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Old Company Name in Catalogs and Other Documents

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	December 27, 1999	No.	TN-SH7-198A/E
THEME	Additions and Modifications of the SH7065 series hardware manual.		
CLASSIFICATION	■ Spec. change ■ Supplement of Documents	□ Limitation on Use	
PRODUCT NAME	HD64F7065S and HD6437065S		
REFERENCE DOCUMENTS	SH7065 series hardware manual No. ADE-602-166(O)	Effective Date: Eternity From: Dec. 9th, 1999	

1. Addition Regarding Software Standby Mode

4.11.1 Transition to Software Standby Mode

When the SH7065 enters software standby mode during bus-released state, /BACK turns to high level from low level. However, state of pins except for /BACK remains in bus-released state.

After /BREQ is driven low during software standby mode, when the SH7065 exits software standby mode while /BREQ remains to be driven low, /BACK becomes high level for 1.5 cycles making conversion of external bus clock (CKE), and then turns to low level.

2. Modification Regarding Clock Pulse Generator (CPG) and Power-Down Modes

4.7 Oscillation Stoppage Detection Function

(Before)

This CPG is provided with a function that automatically places the timer pins in the high-impedance state when it detects clock stoppage to provide for cases where the oscillator halts due to a system error of some kind. If the CPG detects that EXTAL or CKIO has not changed due to an oscillator fault, stoppage of the external clock, or a transition to the standby state, it places the 12 MMT (motor management timer) pins PD26/D26/PWOB/RXD3, PD25/D25/PVOB/TXD3, PD24/D24/PUOB/SCK3, PD22/D22/PWOA/SCK0, PD21/D21/PVOA/IRQ7, PD20/D20/PUOA/IRQ6, PE23/IRQ7/PWOB, PE22/IRQ6/PVOB, PE21/IRQ5/PUOB, PE19/TRQ3/PWOA, PE18/IRQ2/PVOA, and PE17/IRQ1/PUOA/SCK0 in the high-impedance state. (However, PD26/D26/PWOB/RXD3, PD25/D25/PVOB/TXD3, PD24/D24/PUOB/SCK3, PD22/D22/PWOA/SCK0, PD21/D21/PVOA/IRQ7, and PD20/D20/PUOA/IRQ6 go to the high-impedance state only when set as MMT 6-phase output pins by the PFC.)

When oscillation stops other than in the standby state, however, other chip operations are undefined. Also, when oscillation is restarted after stopping other than in the standby state, chip operations, including those of the above 12 pins, are undefined. A power-on reset must therefore be executed when resuming chip operation.

(After)

This CPG is provided with a function that automatically places the timer pins in the high-impedance state when it detects clock stoppage to provide for cases where the oscillator halts due to a system error of some kind. If the CPG detects that EXTAL or CKIO has not changed due to an oscillator fault, stoppage of the external clock, or a transition to the standby state, it places MMT (motor management timer) 6-phase output pins multiplexed to Port E (*1) and multiplexed to Port D (*2) in the high-impedance state.

However, please note that the MMT 6-phase output pins multiplexed to Port E and multiplexed to Port D turn into different pin states when the SH7065 enters software standby state due to HIZ bit (bit 6 of SBYCR (standby control register)) as follows.

(1) The MMT 6-phase output pins multiplexed to Port E

They turn to high-impedance regardless of HIZ bit or PFC setting.

(2) The MMT 6-phase output pins multiplexed to Port D

When they are set as other than data bus by the PFC and HIZ bit is set to “1”, they turn to high-impedance.

When they are set as other than data bus by the PFC and HIZ bit is set to “0”, they maintain their previous state.

When they are set as data bus by the PFC, they turn to high-impedance.

But when the external clock stops, other chip operations are undefined. Also, chip operations, including those of the above 12 pins are undefined when oscillation is restarted after the external clock stopped. Therefore, please execute a power-on reset when resuming chip operation.

Notes

1. PE23/IRQ7/PWOB,PE22/IRQ6/PVOB,PE21/IRQ5/PUOB,PE19/TRQ3/PWOA,PE18/IRQ2/PVOA,PE17/IRQ1/PUOA/SCK0
2. .PD26/D26/PWOB/RXD3,PD25/D25/PVOB/TXD3,PD24/D24/PUOB/SCK3,PD22/D22/PWOA/SCK0,PD21/D21/PVOA/IRQ7, PD20/D20/PUOA/IRQ6

3.Addition Regarding Bus State Controller

8.3.7 Bus Arbitration

When the SH7065 enters software standby mode during bus-released state, /BACK turns to high level from low level. However, state of pins except for /BACK remains in bus-released state.

After /BREQ is driven low during software standby mode, when the SH7065 exits software standby mode while /BREQ remains to be driven low, /BACK becomes high level for 1.5 cycles making conversion of external bus clock (CKE), and then turns to low level.

8.5 Usage Notices

1) Even if CAS assert width is set to 2 cycles, CAS assert width becomes 1 cycle after the second access on condition that access width is bigger than bus width (for example, the access of address 4n+1/4n+2/4n+3 when accessing long word for DRAM whose bus width is 8 bit) by TCAS bit of DRAM control register 2 (DCR2)
2) Limitations when using DRAM/EDO DRAM at RAS down mode.
   (a) RAS down mode is not supported, when Mϕ (clock after the division of master clock (CKM)) is slower than the external bus clock (CKE).
   (b) When row address miss is occurred, CS signal which accesses next is asserted in 1 cycle before accessing to external area.
   (c) When row address value of access in CS4 area is different from the previous access in CS5 area, RAS1 signal is negated.
   (d) When bit value equivalent of row address of transfer-destination is different from row address of transfer-source, RAS1 signal is negated; on condition that transfer-source is CS4/CS5, and transfer-destination is CS0/CS1/CS2/CS3 or on-chip peripheral module at DMAC dual address mode.
   (e) When bit value equivalent of row address at source is different from row address in CS4/5 area accessing from CPU, RAS1 is negated; on condition that DMAC starts up at dual address mode right after CS4/5 area accessing from CPU, and also transfer-source is CS0/CS1/CS2/CS2 or on-chip peripheral module. This phenomenon occurs only the time for transfer right after starting up of DMAC. It does not occur after the second transfer with DMAC at burst mode.
   (f) When bit value equivalent of row address in CS area is different from row address in CS4/5 area accessing from CPU, RAS1 is negated; on condition that DMAC starts up with CS0/CS1/CS2/ CS3 access at single address mode right after CS4/5 area accessing from CPU. This phenomenon occurs only the time for transfer right after starting up of DMAC. It does not occur after the second transfer with DMAC at burst mode.
3) When the SH7065 executes a TAS instruction to on-chip RAM during bus-released state, /BACK is negated once and asserted again after the end of execution.

4. Modification Regarding DC Characteristics (1)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Current dissipation	Nomal operatio	Icc	-	230	260	mA	
	Sleep mode		-	160	240	mA	
	Standby mode		-	5	100	µA	Ta≤ 50℃
			-	-	800	µA	50℃ < Ta
Analog supply current		AIcc	-	0.2	0.25	mA	During A/D conversion
			-	0.1	0.1	µA	Idle

5. Modification Regarding Clock Timing

22.3.1 Clock Timing

(Before)

Item	Symbol	min	Max	Unit	Figure
Operating frequency(master clock)	fop	2	60	MHz	Figure 22.2
Clock cycle time	tcyc	16.7	500	ns	
Clock low-level pulse width	tCL	4.4	-	ns	
Clock high-level pulse width	tCH	4.4	-	ns	
Clock rise time	tcr	-	4	ns	
Clock fall time	tcf	-	4	ns	
EXTAL/CKIO clock input frequency	fEX	2	30	MHz	Figure 22.3
EXTAL/CKIO clock input cycle time	tEXcyc	33.3	500	ns	
EXTAL/CKIO clock input low-level pulse width	tEXL	11.6	-	ns	
EXTAL/CKIO clock input high-level pulse width	tEXH	11.6	-	ns	
EXTAL/CKIO clock input rise time	tEXr	-	5	ns	
EXTAL/CKIO clock input fall time	tEXf	-	5	ns	
Reset oscillation setting time	tOSC1	10	-	ms	Figure 22.4
Standby recovery oscillation setting time	tOSC2	10	-	ms	

(After)

Item	Symbol	min	Max	Unit	Figure
Operating frequency(master clock)	fop	20	60	MHz	Figure 22.2
Clock cycle time	tcyc	16.7	50	ns	
Clock low-level pulse width	tCL	4.4	-	ns	
Clock high-level pulse width	tCH	4.4	-	ns	
Clock rise time	tcr	-	4	ns	
Clock fall time	tcf	-	4	ns	
EXTAL/CKIO clock input frequency	fEX	5	30	MHz	Figure 22.3
EXTAL/CKIO clock input cycle time	tEXcyc	33.3	200	ns	
EXTAL/CKIO clock input low-level pulse width	tEXL	11.6	-	ns	
EXTAL/CKIO clock input high-level pulse width	tEXH	11.6	-	ns	
EXTAL/CKIO clock input rise time	tEXr	-	5	ns	
EXTAL/CKIO clock input fall time	tEXf	-	5	ns	
Reset oscillation setting time	tOSC1	10	-	ms	Figure 22.4
Standby recovery oscillation setting time	tOSC2	10	-	ms	

6. Modification Regarding Pin States
Appendix B Pin State

(Before)

Pin Function		Pin State						
Type	Pin Name	Reset State	Power-Down State			Bus-Released State	Software Standby in Bus-Released State	Hardware Standby in Bus-Released State
			Software Standby	Hardware Standby	Sleep			
Clock	CKIO	I/O/Z*1*2	I/L/Z*1*2	I/L/Z*1*2	I/O/Z*1*2	I/O/Z*1*2	I/L/Z*1*2	I/L/Z*1*2
	EXTAL	I*1	I*1	I*1	I*1	I*1	I*1	I*1
	XTAL	O*1	O*1	O*1	O*1	O*1	O*1	O*1
	CK	O/Z*1*2	L/Z*1*2	L/Z*1*2	O/Z*1*2	O/Z*1*2	L/Z*1*2	L/Z*1*2
	PLLCAP1,2	I/O	I/O	I/O	I/O	I/O	I/O	I/O
System comtrol	/RES	I	I	I	I	I	I	I
	/WDTOVF	H	H	Z	O	O	H	Z
	/BREQ	Z	Z	Z	I	I	Z	Z
	/BACK	Z	Z	Z	O	L	Z	Z
	/HSTBY	I	I	I	I	I	I	I
Operating mode control	MD0 - 5	I	I	I	I	I	I	I
	FWE	I	I	I	I	I	I	I
Interrupt	NMI	I	I	Z	I	I	I	Z
	/IRQ0 - 7	Z	I	Z	I	I	I	Z
	/IRQOUT	Z	H*4	Z	O	O	H*4	Z
Address bus	A0 - 25	O	Z	Z	O	Z	Z	Z
Data bus	D0 - 31	Z	Z	Z	I/O	Z	Z	Z
Bus control	/BS	H*5	Z	Z	O	Z	Z	Z
	/CS0	H*5	Z	Z	O	Z	Z	Z
	/CS1 - /CS5	Z	Z	Z	O	Z	Z	Z
	/RD	H*5	Z	Z	O	Z	Z	Z
	RDWR	Z	Z	Z	O	Z	Z	Z
	/WRLL - /WRHH /WRLL - /WRHH	H*5	Z	Z	O	Z	Z	Z
	/WAIT	Z	Z	Z	I	Z	Z	Z
	/WR	Z	Z	Z	O	Z	Z	Z
	/RAS0 - /RAS1	Z	Z/O*3	Z	O	Z/O*3	Z/O*3	Z
	/CASHH0 - /CASLL0 /CASHH1 - /CASLL1	Z	Z/O*3	Z	O	Z/O*3	Z/O*3	Z
	/OE0,1	Z	Z/O*3	Z	O	Z/O*3	Z/O*3	Z
	/AH	Z	Z	Z	O	Z	Z	Z
DMAC	/DREQ0,1	Z	Z	Z	I	I	Z	Z
	/DRAK0,1	Z	O*4	Z	O	O	O*4	Z
	/DACK0,1	Z	O*4	Z	O	O	O*4	Z
	/TEND0,1	Z	O*4	Z	O	O	O*4	Z
TPU	TCLKA - TCLKD	Z	Z	Z	I	I	Z	Z
	TIOC0A - TIOC0D	Z	K*4	Z	I/O	I/O	K*4	Z
	TIOC1A - TIOC1B	Z	K*4	Z	I/O	I/O	K*4	Z
	TIOC2A - TIOC2B	Z	K*4	Z	I/O	I/O	K*4	Z
	TIOC3A - TIOC3D	Z	K*4	Z	I/O	I/O	K*4	Z
	TIOC4A - TIOC4B	Z	K*4	Z	I/O	I/O	K*4	Z
	TIOC5A - TIOC5B	Z	K*4	Z	I/O	I/O	K*4	Z

Pin Function		Pin State						
Type	Pin Name	Reset State	Power-Down State			Bus-Released State	Software Standby in Bus-Released State	Hardware Standby in Bus-Released State
			Software Standby	Hardware Standby	Sleep			
MMT	PCIO	Z	K*4	Z	I/O	I/O	K*4	Z
	PUOA - PUOB	Z	Z*6	Z*6	O	O	Z*6	Z*6
	PVOA - PVOB	Z	Z*6	Z*6	O	O	Z*6	Z*6
	PWOA - PWOB	Z	Z*6	Z*6	O	O	Z*6	Z*6
	/POE0 - /POE3	Z	Z	Z	I	I	Z	Z
SCI	TxD0 - TxD2	Z	O*4	Z	O	O	O*4	Z
	RxD0 - RxD2	Z	Z	Z	I	I	Z	Z
	SCK0 - SCK2	Z	Z	Z	I/O	I/O	Z	Z
A/D converter	AN0 - AN7	Z	Z	Z	I	I	Z	Z
	/ADTRG	Z	Z	Z	I	I	Z	Z
D/A converter	DA0,1	Z	O*4	Z	O	O	O*4	Z
I/O ports	PAn	Z	K*4	Z	K	I/O	K*4	Z
	PBn	Z	K*4	Z	K	I/O	K*4	Z
	PCn	Z	K*4	Z	K	I/O	K*4	Z
	PDn	Z	K*4	Z	K	I/O	K*4	Z
	PEn	Z	K*4	Z	K	I/O	K*4	Z
	PFn	Z	K*4	Z	K	I/O	K*4	Z
	PGn	Z	K*4	Z	K	I/O	K*4	Z
	PHn	Z	K*4	Z	K	I/O	K*4	Z
	PIn	Z	Z	Z	I	I	Z	Z

I:Input
O:Output
H:High-level output
L:Low-level output
Z:High-impedance state
K:Input pins are in the high-impedance state; output pins maintain their previous state.
Notes 1. Depends on the clock mode.
2. Z or O depending on register setting.
3. Z or O depending on bus control register setting.
4. Z or O depending on standby control register setting.
5. Z in on-chip ROM enabled modes and single-chip mode.
6. Z for all pins when PUOA,PVOA,PWOA,PUOB,PVOB,and PWOB are multiplexed.

(After)

Pin Function		Pin State						
Type System	Pin Name	Reset State	Power-Down State			Bus-Released State	Software Standby in Bus-Released State	Hardware Standby in Bus-Released State
			Software Standby	Hardware Standby	Sleep			
Clock	CKIO	I/O/Z*1*2	I/L/Z*1*2	I/L/Z*1*2	I/O/Z*1*2	I/O/Z*1*2	I/L/Z*1*2	I/L/Z*1*2
	EXTAL	I*1	I*1	I*1	I*1	I*1	I*1	I*1
	XTAL	O*1	O*1	O*1	O*1	O*1	O*1	O*1
	CK	O/Z*1*2	L/Z*1*2	L/Z*1*2	O/Z*1*2	O/Z*1*2	L/Z*1*2	L/Z*1*2
	PLLCAP1,2	I/O	I/O	I/O	I/O	I/O	I/O	I/O
System comtrol	/RES	I	I	I	I	I	I	I
	/WDTOVF	H	H	Z	O	O	H	Z
	/BREQ	Z	Z	Z	I	I	Z	Z
	/BACK	Z	Z	Z	H	L	H	Z
	/HSTBY	I	I	I	I	I	I	I
Operating mode control	MD0 - 5	I	I	I	I	I	I	I
	FWE	I	I	I	I	I	I	I
Interrupt	NMI	I	I	I	I	I	I	I
	/IRQn of PE23 - 21,19 - 17	Z	Z	Z	I	I	Z	Z
	/IRQn of PD21 18,PE20,16 - 12	Z	I	Z	I	I	I	Z
	/IRQOUT	Z	H*4	Z	O	O	H*4	Z
Address bus	A0 - 25	O	Z	Z	O	Z	Z	Z
Data bus	D0 - 31	Z	Z	Z	I/O	Z	Z	Z
Bus control	/BS	H*5	Z	Z	O	Z	Z	Z
	/CS0	H*5	Z	Z	O	Z	Z	Z
	/CS1 -/CS5	Z	Z	Z	O	Z	Z	Z
	/RD	H*5	Z	Z	O	Z	Z	Z
	RDWR	Z	Z	Z	O	Z	Z	Z
	/WRLL - /WRHH /WRLL - /WRHH	H*5	Z	Z	O	Z	Z	Z
	/WAIT	Z	Z	Z	I	Z	Z	Z
	/WR	Z	Z	Z	O	Z	Z	Z
	/RAS0 - /RAS1	Z	Z/O*3	Z	O	Z/O*3	Z/O*3	Z
	/CASHH0 - /CASLL0 /CASHH1 - /CASLL1	Z	Z/O*3	Z	O	Z/O*3	Z/O*3	Z
	/OE0,1	Z	Z/O*3	Z	O	Z/O*3	Z/O*3	Z
	/AH	Z	Z	Z	O	Z	Z	Z
DMAC	/DREQ0,1	Z	Z	Z	I	I	Z	Z
	/DRAK0,1	Z	Z	Z	O	O	Z	Z
	/DACK0,1	Z	O*4	Z	O	O	O*4	Z
	/TEND0,1	Z	O*4	Z	O	O	O*4	Z
TPU	TCLKA - TCLKD	Z	Z	Z	I	I	Z	Z
	TIOC0A - TIOC0D	Z	K*4	Z	I/O	I/O	K*4	Z
	TIOC1A - TIOC1B	Z	K*4	Z	I/O	I/O	K*4	Z
	TIOC2A - TIOC2B	Z	K*4	Z	I/O	I/O	K*4	Z
	TIOC3A - TIOC3D	Z	K*4	Z	I/O	I/O	K*4	Z
	TIOC4A - TIOC4B	Z	K*4	Z	I/O	I/O	K*4	Z
	TIOC5A TIOC5B	Z	K*4	Z	I/O	I/O	K*4	Z

Pin Function		Pin State						
Type	Pin Name	Reset State	Power-Down State			Bus-Released State	Software Standby in Bus-Released State	Hardware Standby in Bus-Released State
			Software Standby	Hardware Standby	Sleep			
MMT	PCIO	Z	K*4	Z	I/O	I/O	K*4	Z
	PUOA(PD20), PUOB(PD24)	Z	O*4	Z	O	O	O*4	Z
	PVOA(PD21), PVOB(PD25)	Z	O*4	Z	O	O	O*4	Z
	PWOA(PD22), PWOB(PD26)	Z	O*4	Z	O	O	O*4	Z
	PUOA(PE17), PUOB(PE21)	Z	Z*6	Z	O	O	Z*6	Z
	PVOA(PE18), PVOB(PE22)	Z	Z*6	Z	O	O	Z*6	Z
	PWOA(PE19), PWOB(PE23)	Z	Z*6	Z	O	O	Z*6	Z
	/POE0 - /POE3	Z	Z	Z	I	I	Z	Z
SCI	TxD0 - TxD2	Z	O*4	Z	O	O	O*4	Z
	RxD0 - RxD2	Z	Z	Z	I	I	Z	Z
	SCK0 - SCK2	Z	Z	Z	I/O	I/O	Z	Z
A/D converter	AN0 - AN7	Z	Z	Z	I	I	Z	Z
	/ADTRG	Z	Z	Z	I	I	Z	Z
D/A converter	DA0,1	Z	Z	Z	O	O	Z	Z
I/O ports	PAn	Z	K*4	Z	K	I/O	K*4	Z
	PBn	Z	K*4	Z	K	I/O	K*4	Z
	PCn	Z	K*4	Z	K	I/O	K*4	Z
	PDn	Z	K*4	Z	K	I/O	K*4	Z
	PE23-21,19-17	Z	Z	Z	K	I/O	Z	Z
	Other PEn	Z	K*4	Z	K	I/O	K*4	Z
	PFn	Z	K*4	Z	K	I/O	K*4	Z
	PGn	Z	K*4	Z	K	I/O	K*4	Z
	PHn	Z	K*4	Z	K	I/O	K*4	Z
	PIn	Z	Z	Z	I	I	Z	Z

I:Input
O:Output
H:High-level output
L:Low-level output
Z:High-impedance state
K:Input pins are in the high-impedance state; output pins maintain their previous state.
Notes 1. Depends on the clock mode.
2. Z or O depending on register setting.
3. Z or O depending on bus control register setting.
4. Z or O depending on standby control register setting.
5. Z in on-chip ROM enabled modes and single-chip mode.
6. Z for all pins when PUOA,PVOA,PWOA,PUOB,PVOB,and PWOB are multiplexed.

HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	26 May 2000	No.	TN- SH7 – 236A/E
THEME	SH7065F change of DC Characteristics value for analog supply current (AIcc)		
CLASSIFICATION	☐ Spec change ☐ Limitation on Use ■ Supplement of Documents		
PRODUCTNAME	HD64F7065SF60/HD64F7065AF60	Lot No.etc.	All
REFERENCE DOCUMENTS	SH7065 Series Hardware Manual	Effective Date	Permanent
		From	Now

The following is the SH7065 change of DC Characteristics value for analog supply current (AIcc).

(1) Change “During A/D conversion” to “During A/D, D/A conversion” in the measurement conditions. And register setting condition is mentioned in Note 1.
(2) Changes “Typ:0.2mA” “Max:0.25mA” to “Typ:2.0mA” “Max:5.0mA” in Alcc during A/D, D/A conversion.

Before the changes:

Item	Symbol	Min	Typ	Max	Unit	Measurement Conditions
Analog supply current	AIcc	-	0.2	0.25	mA	During A/D Conversion
		-	0.1	0.15	mA	Idle

After the changes:

Item	Symbol	Min	Typ	Max	Unit	Measurement Conditions (Note 1)
Analog supply current	AIcc	-	2.0	5.0	mA	During A/D, D/A Conversion
		-	0.1	0.15	mA	Idle

(Note 1) AIcc during the D/A, A/D conversion points out the analog supply current value in the case of the DAE bit in the D/A converter and ADST bit in the A/D are set to 1. Also Idle points out the analog supply current value in the case of the ADST bit in the A/D converter is 0, and DAOE1, DAOE0, DAE bit in the D/A converter are 0.