To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Date: Sep. 28, 2009

RENESAS TECHNICAL UPDATE

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Renesas Technology Corp.

Product Category	MPU/MCU		Document No.	TN-SH7-A739A/E	Rev.	1.00
Title	Additional specs concerning SH7265 electric characteristic tRDH3		Information Category	Technical Notification		
Applicable Product	SH7265 Group	Lot No. All	Reference Document	SH7265 Group Hardware Manual (REJ09B0351-0100)		

This is to notify you of the addition of the bus timing for read data hold time 3 (tRDH3) of electric characteristic of SH7265.

(1) Addition to the Table 36.8 Bus Timing

[The contents before manual correction]

Table 36.8 Bus Timing

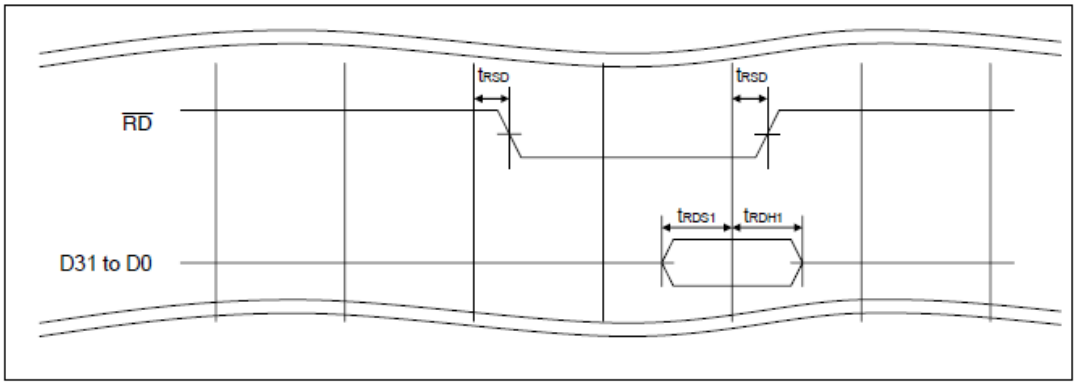
Item	Symbol	Bφ=66.66MHz * Min.	Bφ=66.66MHz * Max.	Unit	Figure
Read data hold time 2 (SDRAM space)	t_{RDH2}	2	-	ns	Figures 36.16, 36.18, 36.20
Read/write mode delay time	t_{RWM}	1	13	ns	Figures 36.11 to 36.15

[The contents after manual correction]

Item	Symbol	Bφ=66.66MHz * Min.	Bφ=66.66MHz * Max.	Unit	Figure
Read data hold time 2 (SDRAM space)	t_{RDH2}	2	-	ns	Figures 36.16, 36.18, 36.20
Read data hold time 3 (external space)	t_{RDH3}	0	-	ns	Figures 36.11 to 36.13, 36.15
Read/write mode delay time	t_{RWM}	1	13	ns	Figures 33.11 to 33.15

(2) Figure 36.11 External Address Space: Basic Bus Timing (Normal Access, Cycle Wait Control, CS Extended Cycle)

[The contents before manual correction]



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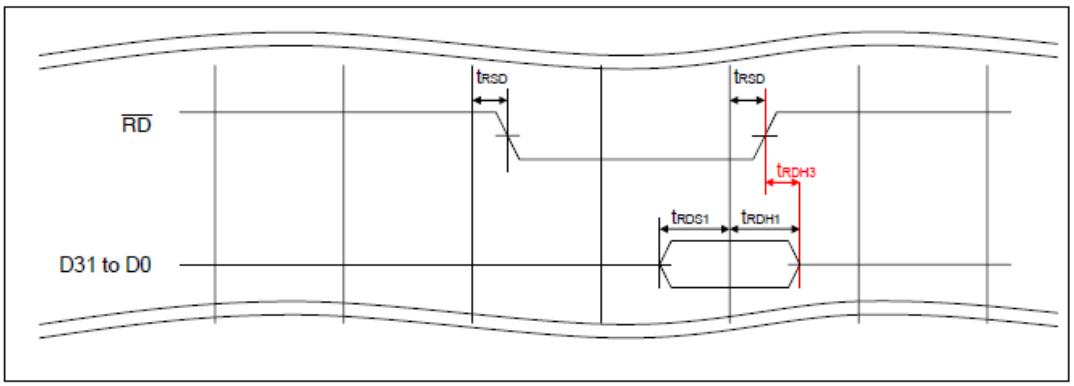
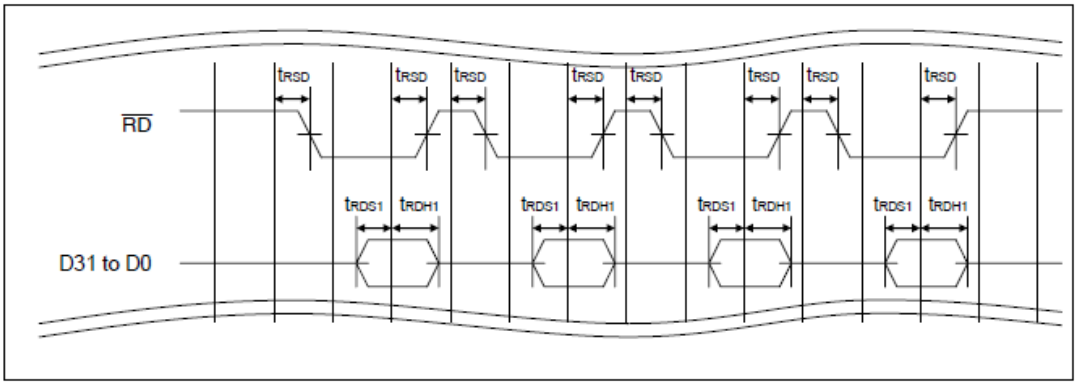


(3) Figure 36.12 External Address Space: Basic Bus Timing (Page Read Access, Normal Access Compatible Mode)

[The contents before manual correction]



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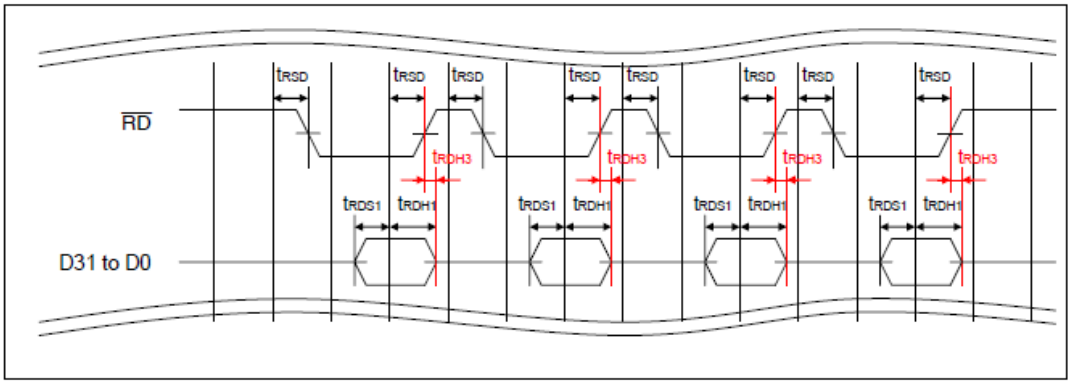

(4) Figure 36.13 External Address Space: Basic Bus Timing (Page Read Access, External Read Data Continuous Assert Mode)

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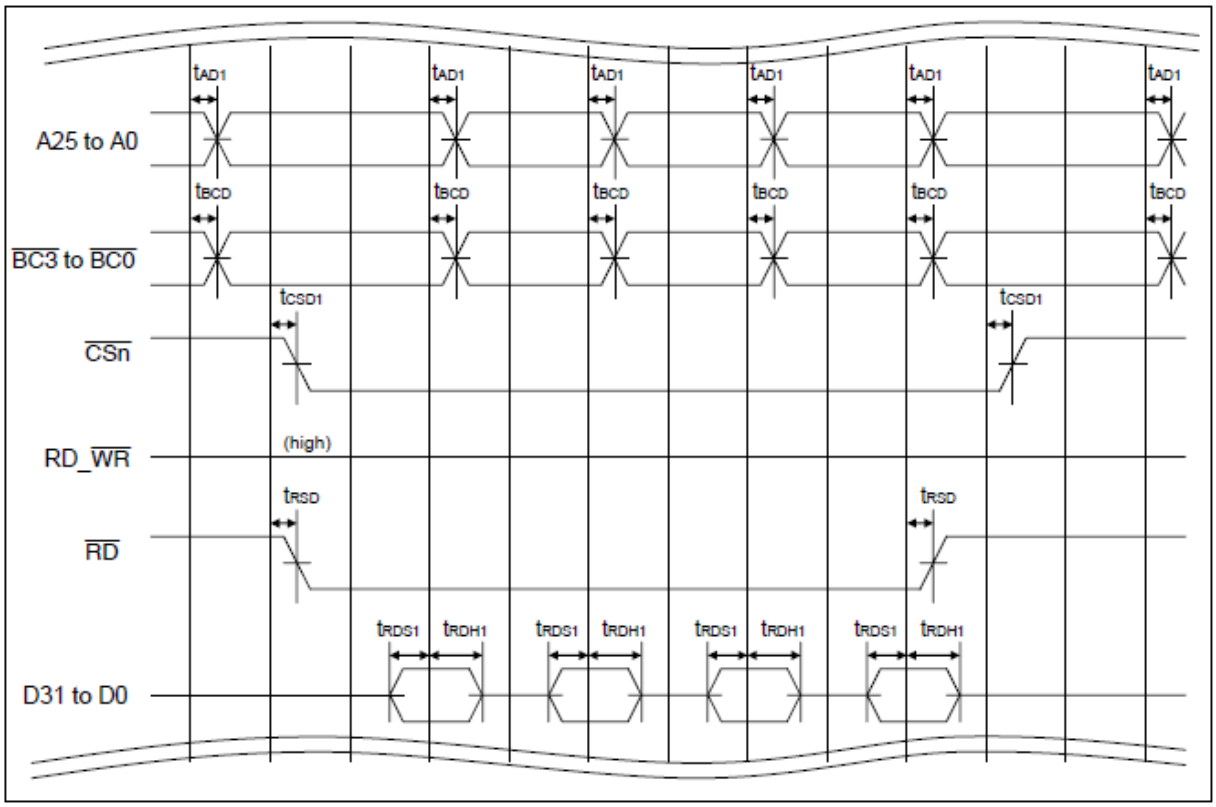

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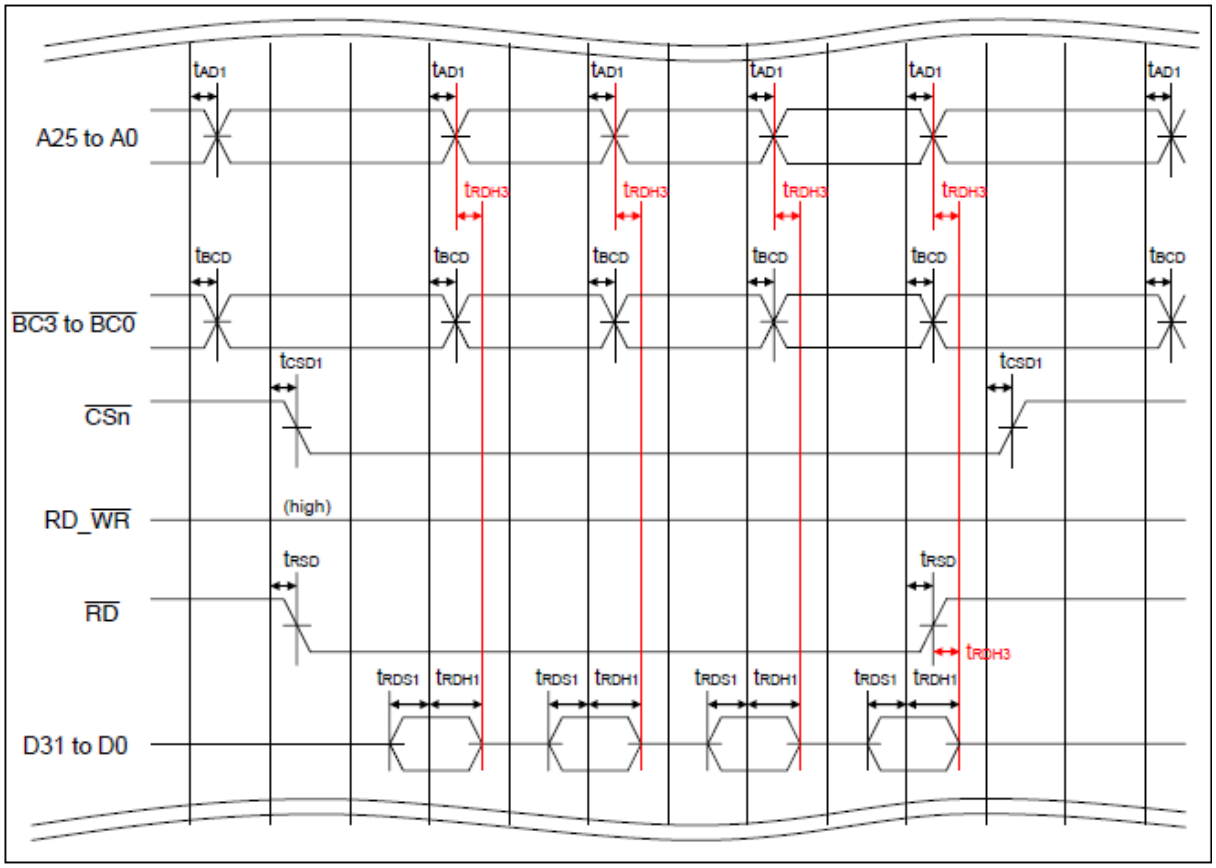
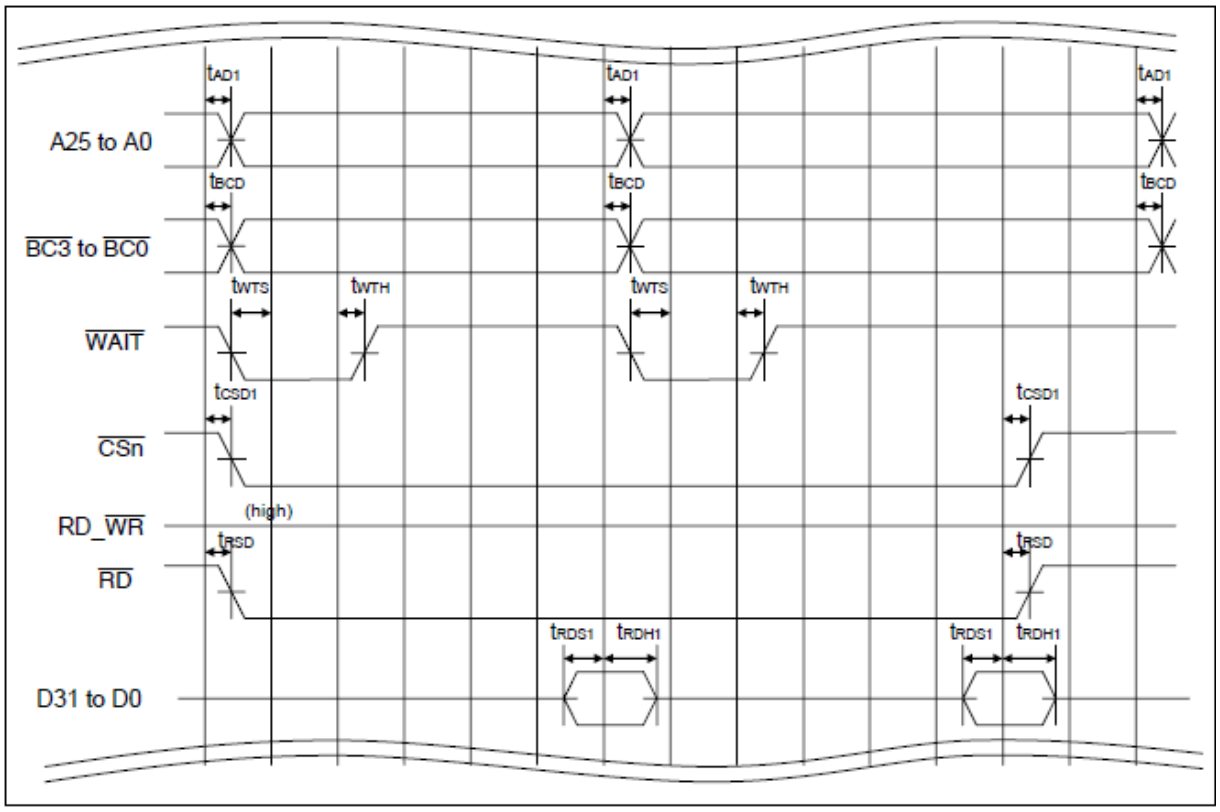


(5) Figure 36.15 External Address Space: Timing with External Wait (Page Read Access to 16-bit Width Channel, External Read Data Continuous Asser Mode)

[The contents before manual correction]



[The contents after manual correction]