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Old Company Name in Catalogs and Other Documents

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	7 August 2001	No.	TN- EML - O71A /E
THEME	Additional Precaution on Using the SH7046 E8000S Emulator		

CLASSIFICATION	☐ Spec. change ☐ Supplement of Documents	☒ Limitation on Use	

PRODUCT NAME	SH7046 E8000S emulator Type number: HS7046EBK81H	Lot No. etc.	Ser. No. 0001 to 0018

REFERENCE DOCUMENT	SH7046 E8000S Emulator User's Manual	Effective Date	Permanent
		From	

In the SH7046 E8000S emulator (type number: HS7046EBK81H), the following malfunction was found in the evaluation chip that has been installed.

[Malfunction]

If two or more access cycles (converted to system clocks) are needed in the stack destination area during hardware exception processing, software break exception processing will be generated instead of the usual exception processing.

[Temporary Countermeasure]

Do not set a stack pointer other than in the internal RAM.

[Precaution]

Exchange the current 'Precautions on Using SH7046 E8000S Emulator' with the updated precaution (HS7046EBK81HE-L (D)) being attached.

Precautions on Using SH7046 E8000S Emulator

Thank you for using the SH7046 E8000S emulator. Note the following when using this E8000S emulator.

1. Operating Mode

When this emulator is used, use the operating mode described in the SH7046 Hardware Manual.

2. Restrictions Resulted from Device

The evaluation chip used in this emulator has the following restrictions.

2.1 AUD/DMAC/DTC Functions

(1) When a break condition is set for the AUD/DMAC/DTC access cycle, and when a break cycle by the STOP button is overlapped with the AUD/DMAC/DTC cycle, the AUD/DMAC/DTC may not correctly transfer the data or display the trace of the bus cycle. For details, refer to the table below.

Malfunction at Contention between the ASE Break Exception Processing and the AUD/DMAC/DTC Bus Cycle Accessing Destination of AUD/DMAC/DTC[1]

Operating Mode	Internal ROM[1]	Internal RAM	Internal I/O	External Memory on User Board	Emulation Memory
MCU expansion mode 0 (invalid ROM mode)	Not used	Normal access Normal trace	Normal access Normal trace	Normal access No bus trace display	Abnormal access[2] No bus trace display
MCU expansion mode 1,2 (valid ROM mode)	Abnormal access[2] No bus trace display	Normal access Normal trace	Normal access Normal trace	Normal access Normal trace	Normal access Normal trace
Single chip mode	Abnormal access[2] No bus trace display	Normal access Normal trace	Normal access Normal trace	Not used	Not used

Notes: 1. Accessing the internal ROM by the AUD is not guaranteed.
2. When the AUD/DMAC/DTC read cycle is contended with the ASE break exception processing, a value before the internal data bus is read. When the AUD/DMAC/DTC write cycle is contended with the ASE break exception processing, the contents in the accessing destination are not rewritten.

(2) If the address error exception processing or interrupt (NMI, user break, H-UDI, IRQ, or internal peripheral module) exception processing and the AUD/DMAC/DTC bus cycle are overlapped, note that the MCU will overrun.

(3) If two or more access cycles (converted to system clocks) are needed in the stack destination area during hardware exception processing, software break exception processing will be generated instead of the usual exception processing.

[Temporary countermeasures by software]

(a) To avoid malfunction (1) above, take the following temporary countermeasures.

• In MCU expansion mode 0, when the external memory is the transfer-source address of the DTC, copy the transfer data on the internal RAM and change the transfer-source address as the internal RAM.

• In MCU expansion mode 1,2, or single chip mode, when the internal ROM is the transfer-source address of the DTC, copy the transfer data on the internal RAM and change the transfer-source address as the internal RAM.

• In MCU expansion mode 0, do not access the external memory by using the AUD.

(b) To avoid malfunction (2) above, take the following temporary countermeasure.

• Do not use the AUD, DMAC, or DTC.

(c) To avoid malfunction (3) above, take the following temporary countermeasure.

• Do not set a stack pointer other than in the internal RAM.

2.2 Others

Restrictions on the device functions or performances also apply to this emulator.

3. Note on Installing the SH7046 E8000S Emulator Software

When this product is installed in the host computer that the SH7046 E8000S emulator software of which version is older than V1.00r1 has been installed, uninstall it before installation. (For uninstallation, refer to section 3.8, Uninstallation, in the user's manual.)

4. Restrictions on Emulator Functions

4.1 Break Function

Do not specify a break in the AUD/DMAC/DTC cycle in the internal break (Break Condition U1 to U4).

4.2 Setting Emulator Operating Conditions

Set the JTAG clock up to 10.0 MHz.