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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A005A/E	Rev.	1.00
Title	Additional precaution about the operation of Flash memory		Information Category	Technical Notification		
Applicable Product	Synergy S3 Series S3A7	Lot No. All lots	Reference Document	S3A7 User's Manual: Microcontrollers, Rev.1.00		

1. Additional information about the operation of Flash memory

• Additional step to set up the flash cache and prepare to rewrite the flash memory in the section 48.4,

Step comparison as follows:

[Before]

48.4 Operation

Use the FCACHEE register to set up and enable flash operation.

To set up the flash cache and prepare to rewrite the flash memory:

1. Disable the flash cache by resetting FCACHEE.FCACHEEN.*1
2. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
3. Check that FCACHEIV.FCACHEIV is 0.
4. Enable the flash cache by setting FCACHEE.FCACHEEN.

Note 1. It is not necessary to disable the flash cache on the first setup after reset

[After]

48.4 Operation

Use the FCACHEE register to set up and enable flash operation.

To set up the flash cache and prepare to rewrite the flash memory:

1. Disable the flash cache by resetting FCACHEE.FCACHEEN.*1
2. Changing the read mode of Flash *2 if necessary.
3. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
4. Check that FCACHEIV.FCACHEIV is 0.
5. Enable the flash cache by setting FCACHEE.FCACHEEN.

Note 1. It is not necessary to disable the flash cache on the first setup after reset

Note 2. Operation of the OPCCR, SOPCCR and MEMWAIT.

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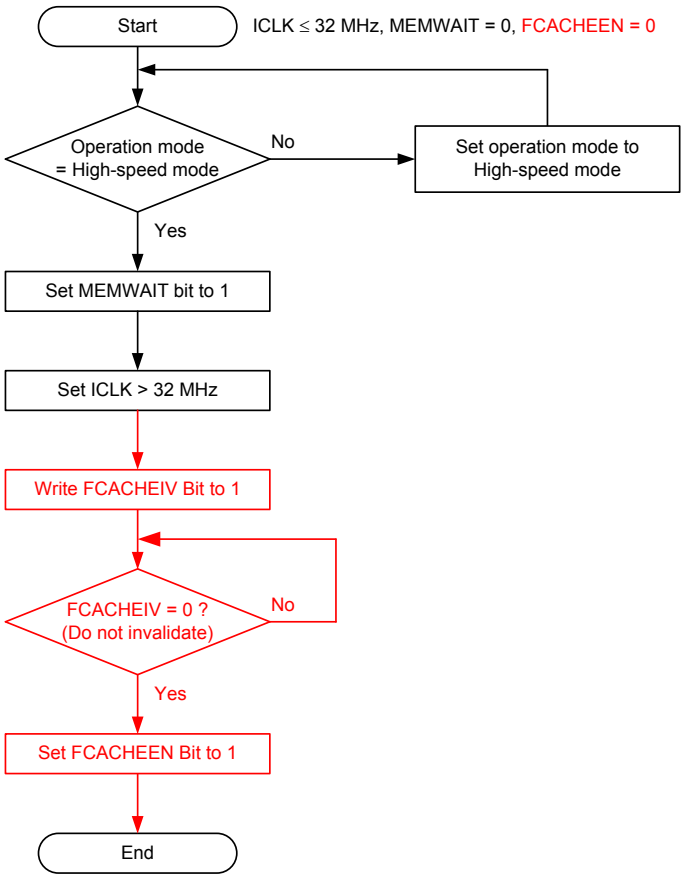
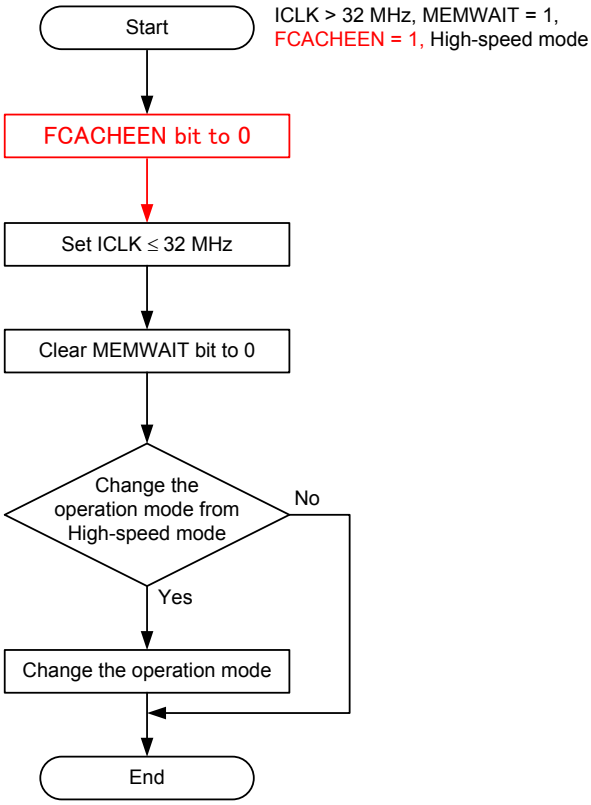
2. Additional information about the section 9.2.6 Memory Wait Cycle Control Register (MEMWAIT)

• Detailed procedure for switching operating Memory wait cycle in case of using the flash cache.

(1) Figure 9.2 When setting the ICLK > 32 MHz



(2) When setting the ICLK ≤ 32 MHz from ICLK > 32 MHz



3. Additional information about the section 11.5.1 Setting Operating Power Control Mode.

• Detailed procedure for switching operating power control modes in case of using the flash cache.

(1) Switching from a higher power mode to a lower power mode

Example 1: From High-speed mode to Low-speed mode:

(Operation in High-speed mode)

1. Disable the flash cache by resetting FCACHEE.FCACHEEN when the flash cache is cacheable in High-speed mode.
2. Change the oscillator to what is used in Low-speed mode. Set the frequency of each clock lower than the maximum operating frequency in Low-speed mode.
3. Turn off the oscillator that is not required in Low-speed mode
4. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed)
5. Set the OPCCR.OPCM bit to 11b (Low-speed mode)
6. Confirm that OPCCR.OPCMTSF flag is 0 (indicates transition completed)

Set the following steps when the flash cache is cacheable in Low-speed mode.

7. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
8. Check that FCACHEIV.FCACHEIV is 0.
9. Enable the flash cache by setting FCACHEE.FCACHEEN.

(Operation in Low-speed mode)

Example 2: From High-speed mode to Subosc-speed mode

(Operation in High-speed mode)

1. Disable the flash cache by resetting FCACHEE.FCACHEEN when the flash cache is cacheable in High-speed mode.
2. Switch the clock source to sub-clock oscillator. Turn off HOCO, MOCO, main oscillator and PLL.
3. Confirm that all clock sources other than the sub-clock oscillator are stopped
4. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed)
5. Set the SOPCCR.SOPCM bit to 1 (Subosc-speed mode)
6. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed)

Set the following steps when the flash cache is cacheable in Subosc-speed mode.

7. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
8. Check that FCACHEIV.FCACHEIV is 0.
9. Enable the flash cache by setting FCACHEE.FCACHEEN.

(Operation in Subosc-speed mode)

(2) Switching from a lower power mode to a higher power mode

Example 1: From Subosc-speed mode to High-speed mode

(Operation in Subosc-speed mode)

1. Disable the flash cache by resetting FCACHEE.FCACHEEN when the flash cache is cacheable in Subosc-speed mode.
2. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed)
3. Set SOPCCR.SOPCM bit to 0 (High-speed mode)
4. Confirm that SOPCCR.SOPCMTSF flag is 0 (indicates transition completed)
5. Turn on the oscillator needed in High-speed mode
6. Set the frequency of each clock to lower than the maximum operating frequency for High-speed mode

Set the following steps when the flash cache is cacheable in High-speed mode.

7. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
8. Check that FCACHEIV.FCACHEIV is 0.
9. Enable the flash cache by setting FCACHEE.FCACHEEN.

(Operation in High-speed mode)

Example 2: From Low-speed mode to High-speed mode

(Operation in Low-speed mode)

1. Disable the flash cache by resetting FCACHEE.FCACHEEN when the flash cache is cacheable in Low-speed mode.
2. Confirm that OPCCR.OPCMTSF flag is 0 (indicates transition completed)
3. Set the OPCCR.OPCM bit to 00b (High-speed mode)
4. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed)
5. Turn on any oscillator needed in High-speed mode
6. Set the frequency of each clock to lower than the maximum operating frequency for High-speed mode

Set the following steps when the flash cache is cacheable in High-speed mode.

7. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
8. Check that FCACHEIV.FCACHEIV is 0.
9. Enable the flash cache by setting FCACHEE.FCACHEEN.

(Operation in High-speed mode)