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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A022A/E	Rev.	1.00
Title	Additional explanation for TCR register of SYS/Audio-DMAC of RZ/G Series		Information Category	Technical Notification		
Applicable Product	RZ/G Series, RZ/G1H, M, N and E	Lot No. All lots	Reference Document	RZ/G Series User's Manual: Hardware Rev.1.00 (R01UH0543EJ0100)		

There is a following additional explanation about the RZ/G series products.

[Summary]

Additional explanation for TCR register of SYS/Audio-DMAC

[Products]

RZ/G1H, M, N and E

[Additional Explanation]

(Following gray highlighted parts (abcd) are newly added. Gray highlighted and cancelation line parts (~~efgh~~) are deleted.)

Section 16. Direct Memory Access Controller for System (SYS-DMAC) for RZ/G1H, M, N and E

Section 16.3.13 DMA Transfer Count Registers 0 to 29 (DMATCR_0 to DMATCR_29)

Section 35. Direct Memory Access Controller for Audio (Audio-DMAC) for RZ/G1H, M, N and E

Section 35.3.13 DMA Transfer Count Registers 0 to 25 (DMATCR_0 to DMATCR_25)

DMATCR is a 32-bit readable/writable register that specifies the number of rounds of DMA transfer. The number of rounds of DMA transfer is 1 when the setting is H'00000001, 16,777,215 when the setting is H'00FFFFFF, and 16,777,216 (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining number of rounds of transfer.

The SYS-DMAC includes independent data buffers for reading and writing. Therefore, the read transfer counter and write transfer counter have different values. This register indicates the counter value used in reading.

The eight higher-order bits of DMATCR are always read as 0, and the write value should always be 0.

The value of this register should be set before DMA transfer starting.

Section 16. Direct Memory Access Controller for System (SYS-DMAC) for RZ/G1H, M, N and E

Section 16.3.17 DMA Channel Control Registers 0 to 29 (DMACHCR_0 to DMACHCR_29)

Section 35. Direct Memory Access Controller for Audio (Audio-DMAC) for RZ/G1H, M, N and E

Section 35.3.17 DMA Channel Control Registers 0 to 25 (DMACHCR_0 to DMACHCR_25)

Bit	Bit Name	Initial Value	R/W	Descriptions
1	TE	0	R/(W)*	Transfer End Flag When the descriptor memory is not in use, the TE bit is set to 1 when DMATCR and DMATSR becomes 0 on completion of the DMA transfer. When the descriptor memory is in use, the TE bit is set to 1 on completion of all transfers set up in the descriptor memory. The TE bit is not set to 1 in the following cases. • DMA transfer ends due to a DMA address error before DMATCR and DMATSR becomes 0. • DMA transfer is aborted by clearing the DE and DME bits in DMAOR. To clear the TE bit, start by reading it as 1, and then write 0 to it. When the TE bit is set to 1, transfer is not possible even if the DE bit is set to 1. 0: DMA transfer is in progress or was aborted [Clearing condition] Writing of 0 after reading of 1 1: DMA transfer ended on the specified count (TCR = 0 and TSR = 0)

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