Date: Feb. 28, 2017

# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-RZ*-A023A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Additional explanation for EthernetAVB of RZ/G Series | | Information Category | Technical Notification | | |
| Applicable Product | RZ/G Series<br>RZ/G1H, M, N and E | Lot No.<br>All lots | Reference Document | RZ/G Series User's Manual: Hardware Rev.1.00 (R01UH0543EJ0100) | | |

There is a following additional explanation about the RZ/G series products.

[Summary]

RZ/G Series User's manual: hardware correction for EthernetAVB.

Since some registers and bits used in the sample driver are not disclosed in the user's manual, add those information to the manual additionally.

[Products]

RZ/G1H, M, N and E

[Note]

There is no specification change (Definition is cleared).

[Additional Explanation]

(Following gray highlighted parts (abcd) are corrected or newly added.)

Section 37A EthernetAVB

**37A.2 Register Descriptions**

- Table 37A.4 Configuration of E-MAC-related Registers

Current (from):

| | | | | | | RZ/G Series Products | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | **Abbreviation** | **R/W** | **Address** | **Initial Value** | **Access Size** | **RZ/G1H** | **RZ/G1M** | **RZ/G1N** | **RZ/G1E** |
| E-MAC mode register | ECMR | R/W | H'E680 0500 | H'0000 0000 | 32 | √ | √ | √ | √ |
| Receive frame length register | RFLR | R/W | H'E680 0508 | H'0000 0000 | 32 | √ | √ | √ | √ |
| E-MAC status register | ECSR | R/W | H'E680 0510 | H'0000 0000 | 32 | √ | √ | √ | √ |
| E-MAC interrupt permission register | ECSIPR | R/W | H'E680 0518 | H'0000 0000 | 32 | √ | √ | √ | √ |
| PHY interface register | PIR | R/W | H'E680 0520 | H'0000 0000 | 32 | √ | √ | √ | √ |
| PHY Status Register | PSR | R | H'E680 0528 | H'0000 0000 | 32 | √ | √ | √ | √ |
| PHY_INT Polarity Register | PIPR | R/W | H'E680 052C | H'0000 0000 | 32 | √ | √ | √ | √ |
| Manual PAUSE frame register | MPR | R/W | H'E680 0558 | H'0000 0000 | 32 | √ | √ | √ | √ |
| PAUSE frame transmit counter | PFTCR | R | H'E680 055C | H'0000 0000 | 32 | √ | √ | √ | √ |
| PAUSE frame receive counter | PFRCR | R | H'E680 0560 | H'0000 0000 | 32 | √ | √ | √ | √ |
| EthernetAVB Mode Register | GECMR | R/W | H'E680 05B0 | H'0000 0000 | 32 | √ | √ | √ | √ |
| E-MAC address high register | MAHR | R/W | H'E680 05C0 | H'0000 0000 | 32 | √ | √ | √ | √ |
| E-MAC address low register | MALR | R/W | H'E680 05C8 | H'0000 0000 | 32 | √ | √ | √ | √ |
| CRC error frame receive counter register | CEFCR | R/W | H'E680 0740 | H'0000 0000 | 32 | √ | √ | √ | √ |
| Frame receive error counter register | FRECR | R/W | H'E680 0748 | H'0000 0000 | 32 | √ | √ | √ | √ |
| Too-short frame receive counter register | TSFRCR | R/W | H'E680 0750 | H'0000 0000 | 32 | √ | √ | √ | √ |
| Too-long frame receive counter register | TLFRCR | R/W | H'E680 0758 | H'0000 0000 | 32 | √ | √ | √ | √ |
| Residual-bit frame receive counter register | RFCR | R/W | H'E680 0760 | H'0000 0000 | 32 | √ | √ | √ | √ |
| Multicast address frame receive counter register | MAFCR | R/W | H'E680 0778 | H'0000 0000 | 32 | √ | √ | √ | √ |

Correction (to):

| | | | | | | RZ/G Series Products | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | **Abbreviation** | **R/W** | **Address** | **Initial Value** | **Access Size** | **RZ/G1H** | **RZ/G1M** | **RZ/G1N** | **RZ/G1E** |
| E-MAC mode register | ECMR | R/W | H'E680 0500 | H'0000 0000 | 32 | √ | √ | √ | √ |
| Receive frame length register | RFLR | R/W | H'E680 0508 | H'0000 0000 | 32 | √ | √ | √ | √ |
| E-MAC status register | ECSR | R/W | H'E680 0510 | H'0000 0000 | 32 | √ | √ | √ | √ |
| E-MAC interrupt permission register | ECSIPR | R/W | H'E680 0518 | H'0000 0000 | 32 | √ | √ | √ | √ |
| PHY interface register | PIR | R/W | H'E680 0520 | H'0000 0000 | 32 | √ | √ | √ | √ |
| PHY Status Register | PSR | R | H'E680 0528 | H'0000 0000 | 32 | √ | √ | √ | √ |

| Name | Abbreviation | R/W | Address | Initial Value | Access Size | RZ/G Series Products RZ/G1H | RZ/G1M | RZ/G1N | RZ/G1E |
|---|---|---|---|---|---|---|---|---|---|
| PHY_INT Polarity Register | PIPR | R/W | H'E680 052C | H'0000 0000 | 32 | √ | √ | √ | √ |
| Manual PAUSE frame register | MPR | R/W | H'E680 0558 | H'0000 0000 | 32 | √ | √ | √ | √ |
| PAUSE frame transmit counter | PFTCR | R | H'E680 055C | H'0000 0000 | 32 | √ | √ | √ | √ |
| PAUSE frame receive counter | PFRCR | R | H'E680 0560 | H'0000 0000 | 32 | √ | √ | √ | √ |
| EthernetAVB Mode Register | GECMR | R/W | H'E680 05B0 | H'0000 0000 | 32 | √ | √ | √ | √ |
| E-MAC address high register | MAHR | R/W | H'E680 05C0 | H'0000 0000 | 32 | √ | √ | √ | √ |
| E-MAC address low register | MALR | R/W | H'E680 05C8 | H'0000 0000 | 32 | √ | √ | √ | √ |
| Transmit retry over counter register | TROCR | R/W | H'E680 0700 | H'0000 0000 | 32 | √ | √ | √ | √ |
| CRC error frame receive counter register | CEFCR | R/W | H'E680 0740 | H'0000 0000 | 32 | √ | √ | √ | √ |
| Frame receive error counter register | FRECR | R/W | H'E680 0748 | H'0000 0000 | 32 | √ | √ | √ | √ |
| Too-short frame receive counter register | TSFRCR | R/W | H'E680 0750 | H'0000 0000 | 32 | √ | √ | √ | √ |
| Too-long frame receive counter register | TLFRCR | R/W | H'E680 0758 | H'0000 0000 | 32 | √ | √ | √ | √ |
| Residual-bit frame receive counter register | RFCR | R/W | H'E680 0760 | H'0000 0000 | 32 | √ | √ | √ | √ |
| Multicast address frame receive counter register | MAFCR | R/W | H'E680 0778 | H'0000 0000 | 32 | √ | √ | √ | √ |

**Section number**

Current (from):

37A.2.61 CRC Error Frame Receive Counter Register (CEFCR)

37A.2.62 Frame Receive Error Counter Register (FRECR)

37A.2.63 Too-Short Frame Receive Counter Register (TSFRCR)

37A.2.64 Too-Long Frame Receive Counter Register (TLFRCR)

37A.2.65 Residual-Bit Frame Receive Counter Register (RFCR)

37A.2.66 Multicast Address Frame Receive Counter Register (MAFCR)

Correction (to):

37A.2.61 Transmit retry over counter register (TROCR) -> new chapter; description at end of this document

37A.2.62 CRC Error Frame Receive Counter Register (CEFCR)

37A.2.63 Frame Receive Error Counter Register (FRECR)

37A.2.64 Too-Short Frame Receive Counter Register (TSFRCR)

37A.2.65 Too-Long Frame Receive Counter Register (TLFRCR)

37A.2.66 Residual-Bit Frame Receive Counter Register (RFCR)

37A.2.67 Multicast Address Frame Receive Counter Register (MAFCR)

**Description for updated registers**

37A.2.37 Transmit Interrupt Control Register (TIC)

Current (from):

| Bit: | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | TFWE | TFUE | — | — | — | — | — | — | — | — |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 31 to 10 | — | All 0 | R/W | Reserved<br>These bits are read as 0. The write value should be 0. |
| 9 | TFWE | 0 | R/W | Time Stamp FIFO Warning Interrupt Enable<br>When the time-stamp FIFO reaches the warning level while the interrupt is enabled, the interrupt is issued.<br>0: Disabled<br>1: Enabled |
| 8 | TFUE | 0 | R/W | Time Stamp FIFO Update Interrupt Enable<br>When the time-stamp FIFO is updated while the interrupt is enabled, the interrupt is issued.<br>0: Disabled<br>1: Enabled |
| 7 to 0 | — | All 0 | R/W | Reserved<br>These bits are read as 0. The write value should be 0. |

Correction (to):

| Bit: | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | TFWE | TFUE | — | — | — | — | FTE3 | FTE2 | FTE1 | FTE0 |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 31 to 10 | — | All 0 | R/W | Reserved<br>These bits are read as 0. The write value should be 0. |
| 9 | TFWE | 0 | R/W | Time Stamp FIFO Warning Interrupt Enable<br>When the time-stamp FIFO reaches the warning level while the interrupt is enabled, the interrupt is issued.<br>0: Disabled<br>1: Enabled |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 8 | TFUE | 0 | R/W | Time Stamp FIFO Update Interrupt Enable<br>When the time-stamp FIFO is updated while the interrupt is enabled, the interrupt is issued.<br>0: Disabled<br>1: Enabled |
| 7 to 4 | — | All 0 | R/W | Reserved<br>These bits are read as 0. The write value should be 0. |
| 3 | FTE3 | 0 | R/W | Frame Transmitted interrupt Enable 3<br>While this bit is 1b an interrupt will be generated when **TIS.FTF3** is 1b.<br>0: Disabled<br>1: Enabled |
| 2 | FTE2 | 0 | R/W | Frame Transmitted interrupt Enable 2<br>While this bit is 1b an interrupt will be generated when **TIS.FTF2** is 1b.<br>0: Disabled<br>1: Enabled |
| 1 | FTE1 | 0 | R/W | Frame Transmitted interrupt Enable 1<br>While this bit is 1b an interrupt will be generated when **TIS.FTF1** is 1b.<br>0: Disabled<br>1: Enabled |
| 0 | FTE0 | 0 | R/W | Frame Transmitted interrupt Enable 0<br>While this bit is 1b an interrupt will be generated when **TIS.FTF0** is 1b.<br>0: Disabled<br>1: Enabled |

37A.2.38 Transmit Interrupt Status Register (TIS)

Current (from):

| Bit: | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | TFWF | TFUF | — | — | — | — | — | — | — | — |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 31 to 10 | — | All 0 | R/W | Reserved<br>These bits are read as 0. The write value should be 0. |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 9 | TFWF | 0 | R/W | Time Stamp FIFO Warning Interrupt Status<br>This bit indicates that the transmission time-stamp FIFO has reached the warning level.<br>Only 0 can be written to the bit.<br>[Conditions for Changing]<br>— The bit is set to 0 when the operating mode is not operation mode and when the time stamp FIFO enable bit in the transmit configuration control register (TCCR.TFEN) is 0.<br>— The bit is set to 1 after a frame including DESCR.TSR set has been transmitted and one entry has already been stored in the time-stamp FIFO.<br>0: The interrupt is not pending.<br>1: The time-stamp FIFO has reached the warning level. |
| 8 | TFUF | 0 | R/W | Time Stamp FIFO Update Interrupt Status<br>This bit indicates that the transmission time-stamp FIFO has been updated.<br>Only 0 can be written to the bit.<br>[Conditions for Changing]<br>— The bit is set to 0 when the operating mode is not operation mode, when the time stamp FIFO enable bit in the transmit configuration control register (TCCR.TFEN) is 0, and when 1 is written to the time stamp FIFO release bit in the transmit configuration control register (TCCR.TFR).<br>— The bit is set to 1 when the time stamp FIFO enable bit (TCCR.TFEN) is 1 after a frame including DESCR.TSR set has been transmitted.<br>0: The interrupt is not pending.<br>1: The time-stamp FIFO has been updated. |
| 7 to 0 | — | All 0 | R/W | Reserved<br>These bits are read as 0. The write value should be 0. |

Correction (to):

| Bit: | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | TFWF | TFUF | — | — | — | — | FTF3 | FTF2 | FTF1 | FTF0 |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 31 to 10 | — | All 0 | R/W | Reserved<br>These bits are read as 0. The write value should be 0. |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 9 | TFWF | 0 | R/W | Time Stamp FIFO Warning Interrupt Status<br>This bit indicates that the transmission time-stamp FIFO has reached the warning level.<br>Only 0 can be written to the bit.<br>[Conditions for Changing]<br>— The bit is set to 0 when the operating mode is not operation mode and when the time stamp FIFO enable bit in the transmit configuration control register (TCCR.TFEN) is 0.<br>— The bit is set to 1 after a frame including DESCR.TSR set has been transmitted and one entry has already been stored in the time-stamp FIFO.<br>0: The interrupt is not pending.<br>1: The time-stamp FIFO has reached the warning level. |
| 8 | TFUF | 0 | R/W | Time Stamp FIFO Update Interrupt Status<br>This bit indicates that the transmission time-stamp FIFO has been updated.<br>Only 0 can be written to the bit.<br>[Conditions for Changing]<br>— The bit is set to 0 when the operating mode is not operation mode, when the time stamp FIFO enable bit in the transmit configuration control register (TCCR.TFEN) is 0, and when 1 is written to the time stamp FIFO release bit in the transmit configuration control register (TCCR.TFR).<br>— The bit is set to 1 when the time stamp FIFO enable bit (TCCR.TFEN) is 1 after a frame including DESCR.TSR set has been transmitted.<br>0: The interrupt is not pending.<br>1: The time-stamp FIFO has been updated. |
| 7 to 4 | — | All 0 | R/W | Reserved<br>These bits are read as 0. The write value should be 0. |
| 3 | FTF3 | 0 | R/W | Frame Transmitted Flag 3<br>This bit indicates that from transmit queue a frame is transmitted by E-MAC.<br>Note: This interrupt flag refers to the end of frame transmission by E-MAC whereas the descriptor interrupt (**DIS.DPFi**) refers to the end of processing storage element.<br>The CPU can only write 0b to this bit.<br>[Changing condition]<br>This bit is set to 0b when leaving OPERATION mode.<br>This bit is set to 1b when a frame from transmit queue 3 has been transmitted by the E-MAC.<br>0: No interrupt pending<br>1: Frame transmitted by E-MAC |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 2 | FTF2 | 0 | R/W | Frame Transmitted Flag 2<br>This bit indicates that from transmit queue a frame is transmitted by E-MAC.<br>Note: This interrupt flag refers to the end of frame transmission by E-MAC whereas the descriptor interrupt (**DIS.DPFi**) refers to the end of processing storage element.<br>The CPU can only write 0b to this bit.<br>[Changing condition]<br>This bit is set to 0b when leaving OPERATION mode.<br>This bit is set to 1b when a frame from transmit queue 2 has been transmitted by the E-MAC.<br>0: No interrupt pending<br>1: Frame transmitted by E-MAC |
| 1 | FTF1 | 0 | R/W | Frame Transmitted Flag 1<br>This bit indicates that from transmit queue a frame is transmitted by E-MAC.<br>Note: This interrupt flag refers to the end of frame transmission by E-MAC whereas the descriptor interrupt (**DIS.DPFi**) refers to the end of processing storage element.<br>The CPU can only write 0b to this bit.<br>[Changing condition]<br>This bit is set to 0b when leaving OPERATION mode.<br>This bit is set to 1b when a frame from transmit queue 1 has been transmitted by the E-MAC.<br>0: No interrupt pending<br>1: Frame transmitted by E-MAC |
| 0 | FTF0 | 0 | R/W | Frame Transmitted Flag 0<br>This bit indicates that from transmit queue a frame is transmitted by E-MAC.<br>Note: This interrupt flag refers to the end of frame transmission by E-MAC whereas the descriptor interrupt (**DIS.DPFi**) refers to the end of processing storage element.<br>The CPU can only write 0b to this bit.<br>[Changing condition]<br>This bit is set to 0b when leaving OPERATION mode.<br>This bit is set to 1b when a frame from transmit queue 0 has been transmitted by the E-MAC.<br>0: No interrupt pending<br>1: Frame transmitted by E-MAC |

37A.2.39 Interrupt Summary Status Register (ISS)

Current (from):

| Bit: | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DPS15 | DPS14 | DPS13 | DPS12 | DPS11 | DPS10 | DPS9 | DPS8 | DPS7 | DPS6 | DPS5 | DPS4 | DPS3 | DPS2 | DPS1 | — |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | CGIS | RFWS | — | — | TFWS | TFUS | MS | ES | — | — | — | — | — | — |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 31 | DPS15 | 0 | R/W | Descriptor Interrupt 15 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE15) and descriptor interrupt status flag (DIS.DPF15) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 30 | DPS14 | 0 | R/W | Descriptor Interrupt 14 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE14) and descriptor interrupt status flag (DIS.DPF14) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 29 | DPS13 | 0 | R/W | Descriptor Interrupt 13 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE13) and descriptor interrupt status flag (DIS.DPF13) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 28 | DPS12 | 0 | R/W | Descriptor Interrupt 12 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE12) and descriptor interrupt status flag (DIS.DPF12) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 27 | DPS11 | 0 | R/W | Descriptor Interrupt 11 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE11) and descriptor interrupt status flag (DIS.DPF11) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 26 | DPS10 | 0 | R/W | Descriptor Interrupt 10 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE10) and descriptor interrupt status flag (DIS.DPF10) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 25 | DPS9 | 0 | R/W | Descriptor Interrupt 9 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE9) and descriptor interrupt status flag (DIS.DPF9) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 24 | DPS8 | 0 | R/W | Descriptor Interrupt 8 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE8) and descriptor interrupt status flag (DIS.DPF8) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 23 | DPS7 | 0 | R/W | Descriptor Interrupt 7 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE7) and descriptor interrupt status flag (DIS.DPF7) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 22 | DPS6 | 0 | R/W | Descriptor Interrupt 6 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE6) and descriptor interrupt status flag (DIS.DPF6) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 21 | DPS5 | 0 | R/W | Descriptor Interrupt 5 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE5) and descriptor interrupt status flag (DIS.DPF5) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 20 | DPS4 | 0 | R/W | Descriptor Interrupt 4 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE4) and descriptor interrupt status flag (DIS.DPF4) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 19 | DPS3 | 0 | R/W | Descriptor Interrupt 3 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE3) and descriptor interrupt status flag (DIS.DPF3) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 18 | DPS2 | 0 | R/W | Descriptor Interrupt 2 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE2) and descriptor interrupt status flag (DIS.DPF2) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 17 | DPS1 | 0 | R/W | Descriptor Interrupt 1 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE1) and descriptor interrupt status flag (DIS.DPF1) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 16 to 14 | — | All 0 | R/W | Reserved<br>These bits are read as 0. The write value should be 0. |
| 13 | CGIS | 0 | R/W | gPTP Interrupt Summary<br>This bit is set to 1 when either interrupt-related bit in the two gPTP-related interrupt registers (GIC and GIS) is 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 12 | RFWS | 0 | R/W | Receive FIFO Warning Interrupt Summary<br>This bit is set to 1 when the receive FIFO warning interrupt enable bit (RIC1.RFWE) and receive FIFO warning interrupt status flag (RIS1.RFWF) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 11, 10 | — | All 0 | R/W | Reserved<br>These bits are read as 0. The write value should be 0. |
| 9 | TFWS | 0 | R/W | Time Stamp FIFO Warning Interrupt Summary<br>This bit is set to 1 when the time stamp FIFO warning interrupt enable bit (TIC.TFWE) and time stamp FIFO warning interrupt status flag (TIS.TFWF) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 8 | TFUS | 0 | R/W | Time Stamp FIFO Update Interrupt<br>This bit is set to 1 when the time stamp FIFO update interrupt enable bit (TIC.TFUE) and time stamp FIFO update interrupt status flag (TIS.TFUF) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 7 | MS | 0 | R/W | E-MAC Interrupt Summary<br>This bit is set to 1 when an E-MAC interrupt is issued.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 6 | ES | 0 | R/W | Error Interrupt Summary<br>This bit is set to 1 when an error interrupt is issued (both of a bit in EIS and corresponding to the bit in EIC are 1).<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 5 to 0 | — | All 0 | R/W | Reserved<br>These bits are read as 0. The write value should be 0. |

Correction (to):

| Bit: | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DPS15 | DPS14 | DPS13 | DPS12 | DPS11 | DPS10 | DPS9 | DPS8 | DPS7 | DPS6 | DPS5 | DPS4 | DPS3 | DPS2 | DPS1 | — |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | CGIS | RFWS | — | — | TFWS | TFUS | MS | ES | — | — | — | FTS | — | FRS |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 31 | DPS15 | 0 | R | Descriptor Interrupt 15 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE15) and descriptor interrupt status flag (DIS.DPF15) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 30 | DPS14 | 0 | R | Descriptor Interrupt 14 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE14) and descriptor interrupt status flag (DIS.DPF14) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 29 | DPS13 | 0 | R | Descriptor Interrupt 13 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE13) and descriptor interrupt status flag (DIS.DPF13) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 28 | DPS12 | 0 | R | Descriptor Interrupt 12 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE12) and descriptor interrupt status flag (DIS.DPF12) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 27 | DPS11 | 0 | R | Descriptor Interrupt 11 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE11) and descriptor interrupt status flag (DIS.DPF11) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 26 | DPS10 | 0 | R | Descriptor Interrupt 10 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE10) and descriptor interrupt status flag (DIS.DPF10) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 25 | DPS9 | 0 | R | Descriptor Interrupt 9 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE9) and descriptor interrupt status flag (DIS.DPF9) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 24 | DPS8 | 0 | R | Descriptor Interrupt 8 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE8) and descriptor interrupt status flag (DIS.DPF8) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 23 | DPS7 | 0 | R | Descriptor Interrupt 7 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE7) and descriptor interrupt status flag (DIS.DPF7) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 22 | DPS6 | 0 | R | Descriptor Interrupt 6 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE6) and descriptor interrupt status flag (DIS.DPF6) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 21 | DPS5 | 0 | R | Descriptor Interrupt 5 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE5) and descriptor interrupt status flag (DIS.DPF5) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 20 | DPS4 | 0 | R | Descriptor Interrupt 4 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE4) and descriptor interrupt status flag (DIS.DPF4) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 19 | DPS3 | 0 | R | Descriptor Interrupt 3 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE3) and descriptor interrupt status flag (DIS.DPF3) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 18 | DPS2 | 0 | R | Descriptor Interrupt 2 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE2) and descriptor interrupt status flag (DIS.DPF2) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 17 | DPS1 | 0 | R | Descriptor Interrupt 1 Summary<br>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE1) and descriptor interrupt status flag (DIS.DPF1) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 16 to 14 | — | All 0 | R | Reserved<br>These bits are read as 0. |
| 13 | CGIS | 0 | R | gPTP Interrupt Summary<br>This bit is set to 1 when either interrupt-related bit in the two gPTP-related interrupt registers (GIC and GIS) is 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 12 | RFWS | 0 | R | Receive FIFO Warning Interrupt Summary<br>This bit is set to 1 when the receive FIFO warning interrupt enable bit (RIC1.RFWE) and receive FIFO warning interrupt status flag (RIS1.RFWF) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 11, 10 | — | All 0 | R | Reserved<br>These bits are read as 0. |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 9 | TFWS | 0 | R | Time Stamp FIFO Warning Interrupt Summary<br>This bit is set to 1 when the time stamp FIFO warning interrupt enable bit (TIC.TFWE) and time stamp FIFO warning interrupt status flag (TIS.TFWF) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 8 | TFUS | 0 | R | Time Stamp FIFO Update Interrupt<br>This bit is set to 1 when the time stamp FIFO update interrupt enable bit (TIC.TFUE) and time stamp FIFO update interrupt status flag (TIS.TFUF) are both 1.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 7 | MS | 0 | R | E-MAC Interrupt Summary<br>This bit is set to 1 when an E-MAC interrupt is issued.<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 6 | ES | 0 | R | Error Interrupt Summary<br>This bit is set to 1 when an error interrupt is issued (both of a bit in EIS and corresponding to the bit in EIC are 1).<br>0: The interrupt is not pending.<br>1: The interrupt is pending. |
| 5 to 3 | — | All 0 | R | Reserved<br>These bits are read as 0. |
| 2 | FTS | 0 | R | Frame Transmitted Summary<br>[Changing condition]<br>This bit is set when any matching pair of **TIC.FTEt** enable and **TIS.FTFt** flag are both 1b.<br>0: No interrupt pending<br>1: Frame transmitted interrupt pending |
| 1 | — | 0 | R | Reserved<br>These bits are read as 0. |
| 0 | FRS | 0 | R | Frame Received Summary<br>[Changing condition]<br>This bit is set when any matching pair of **RIC0.FREr** enable and **RIS0.FRFr** flag are both 1b.<br>0: No interrupt pending<br>1: Frame received interrupt pending |

**Description for additional registers**

37A.2.61 Transmit retry over counter register (TROCR)

| RZ/G1H | RZ/G1M | RZ/G1N | RZ/G1E |
|---|---|---|---|
| √ | √ | √ | √ |

The TROCR register is a counter that indicates the number of times frames with time-out were transmit. Counting up stops when the value in this register reaches H'0000 FFFF.

| Bit: | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | FTTOC[15:0] | | | | | | | | | | | | | | | |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 31 to 16 | — | All 0 | R/W | Reserved<br>These bits are read as 0. The write value should be 0. |
| 15 to 0 | FTTOC [15:0] | H'0000 | R/W | Frame transmit time-out counter<br>These bits indicate the number of transmit frames having time-out.<br>The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1.<br>When TRCCM = 0, they are cleared to 0 by the writing of any value to this register. |

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