To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Mar.22.2005

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A549A/E	Rev.	1.0
Title	Addition of connectable SDRAM with SH7616.		Information Category	Technical Notification		
Applicable Product	HD6417616SF HD6417616SFV	Lot No. Show below	Reference Document	SH7616 Hardware Manual (ADE-602-243 Rev.1.0)		

We report newly that 128-Mbit and 256-Mbit Synchronous DRAM are connectable with SH7616.

For the setting method, please refer to the following [After] table of MCR in BSC.

This addition is public presentation of the specification about the portion which was not exhibited before,

and the product itself is not changed.

For the applied lot, please refer to the Product Lot Code in the following [Mass production schedule].

[Before]

Section 7 Bus State Controller(BSC)

7.2.7 Individual Memory Control Resister(MCR)

- For synchronous DRAM interface

Bit7:AMX2	Bit5:AMX1	Bit4:AMX0	Description
0	0	0	16-Mbit DRAM(1M×16bits), 64-Mbit DRAM(2M×32bits) *2
		1	16-Mbit DRAM(2M×8bits) *1
	1	0	16-Mbit DRAM(4M×4bits) *1
		1	4-Mbit DRAM(256k×16bits)
1	0	0	64-Mbit DRAM(4M×16bits)
		1	64-Mbit DRAM(8M×8bits) *1
	1	0	Reserved do not set
		1	2-Mbit DRAM(128k×16bits)

Notes: 1. Reserved. Do not set when SZ bit in MCR is 0 (16-bit bus width).
2. See sction 7.5.11 for the method of connection to a 64-Mbit DRAM with a 2M×32-bi configuration.

[Affter]

Section 7 Bus State Controller(BSC)

7.2.7 Individual Memory Control Resister(MCR)

- For synchronous DRAM interface

Bit7:AMX2	Bit5:AMX1	Bit4:AMX0	Description
0	0	0	16-Mbit DRAM(1M×16bits), 64-Mbit DRAM(2M×32bits) *2
		1	16-Mbit DRAM(2M×8bits) *1
	1	0	16-Mbit DRAM(4M×4bits) *1
		1	4-Mbit DRAM(256k×16bits)
1	0	0	64-Mbit DRAM(4M×16bits), 128-Mbit DRAM(4M×32bits) *3
		1	64-Mbit DRAM(8M×8bits) *1 128-Mbit DRAM(8M×16bits) *1 *4 256-Mbit DRAM(8M×32bits) *1 *4
	1	0	Reserved do not set
		1	2-Mbit DRAM(128k×16bits)

Notes: 1. Reserved. Do not set when SZ bit in MCR is 0 (16-bit bus width).
2. See sction 7.5.11 for the method of connection to a 64-Mbit DRAM with a 2M×32-bit configuration.
3. See Figure1 for the method of connection to a 128-Mbit DRAM with a 4M×32-bit configuration.
4. In the case of a 128-Mbit DRAM(8M×16-bit), connect to two 128M bit DRAMs (8M×16-bit) by 32-bit data width as Figure2.
5. See Figure3 for the method of connection to a 256-Mbit DRAM with a 8M×32-bit configuration.

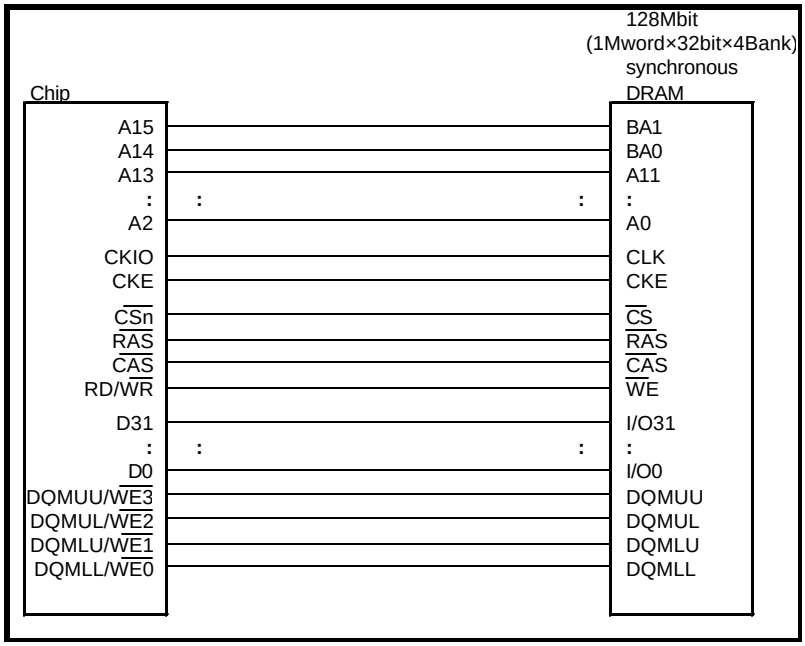

Figure1 128Mbit Synchronous DRAM (4Mword×32bit) Connection Example

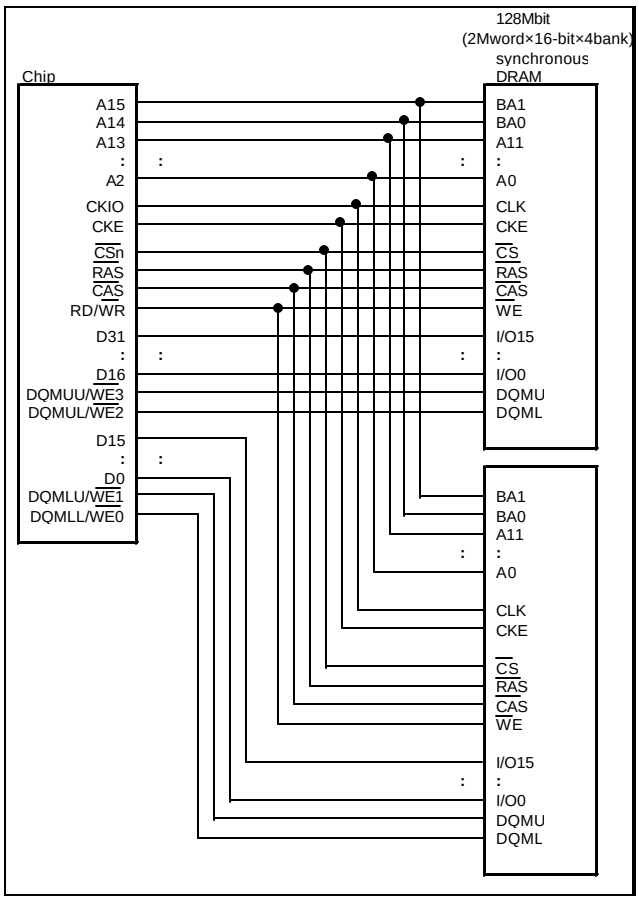

Figure2 128Mbit Synchronous DRAM(8Mword×16bit) Connection Example

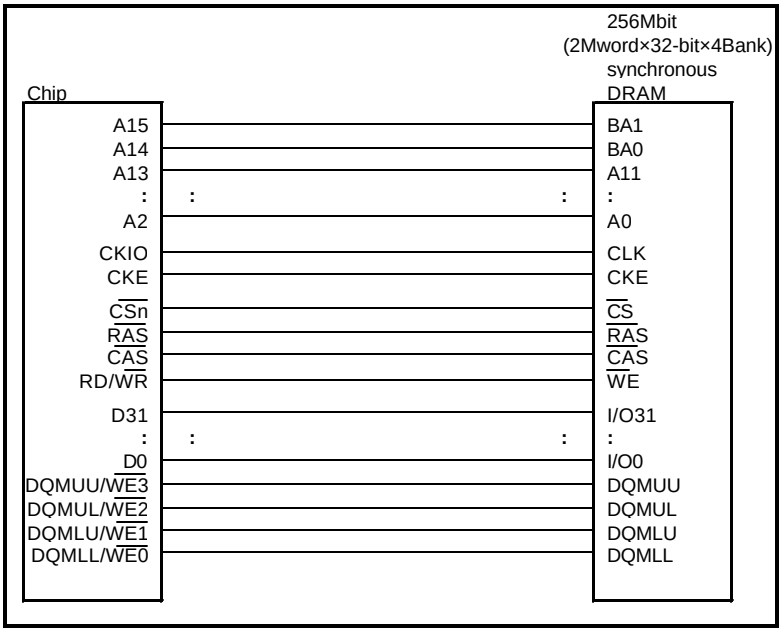

Figure3 256Mbit Synchronous DRAM (8Mword×32bit) Connection Example

[Mass production schedule]

It applies from the following Product Lot Code.

	Product Lot Code
HD6417616SF :	0432
HD6417616SFV :	0432