8-bit Microcontrollers 78K0/Fx2 Release of Specification-Expanded Products	ZBB-BG-06-0097	1/2
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Thank you for your continued support of NEC Electronics products.
This is to inform you of new information concerning the 78K0/Fx2. Please see below for details.

1. Affected products

78K0/Fx2 microcontrollers

78K0/FC2: μPD78F0881, μPD78F0882, μPD78F0883, μPD78F0884, μPD78F0885, μPD78F0886

78K0/FE2: μPD78F0887, μPD78F0888, μPD78F0889, μPD78F0890

78K0/FF2: μPD78F0891, μPD78F0892, μPD78F0893

2. Expanded specifications

Specifications of 78K0/Fx2 microcontroller products will be expanded.

The name of the expanded-specification products will be changed (the letter A will be added to the end of the current product name).

Current name: μPD78F08xx
New name: μPD78F08xxA

See below for an overview of the specification.

The modification and specification expansion described in this document are implemented to the aluminum layer, so there will be no differences in the electrical characteristics and reliability between the current products and new products.

♦ Major changed items

(1) Expansion of flash memory rewritable count and duration period

The rewritable count and duration period of flash memory will be expanded.

See attachment 1 for details.

(2) Improvement of flash memory self-programming interrupt response time

The flash memory self-programming interrupt response time will be improved.

See attachment 2 for details.

(3) Modification of flash memory self-programming processing time

In conjunction with improvement of the interrupt response time, the flash memory self-programming processing time will be modified. See attachment 3 for details.

Caution

Since the internal firmware must be modified in the expanded-specification products, **parameter files**, which are used during flash programming, **must also be modified**. Be sure to use the **newly released parameter files** when performing flash programming to an expanded-specification product.

3. Release schedule

The expanded-specification products will be released according to the schedule shown below. For details, consult an NEC Electronics sales representative.

ES: June 2007

CS: July 2007

MP: September 2007

4. Development tools

The development tools that can be used with the expanded-specification products and their support schedules are as follows.

Development tools	Support Status and Schedule
QB-78K0FX2	Will be supported. But cannot be used with the device files for the current products. Be sure to use the newly released device files
QB-78K0MINI QB-MINI2	Will be supported. But cannot be used with the device files for the current products. Be sure to use the newly released device files
PG-FP4 PG-FPL3	Will be supported, but cannot be used with the parameter files for the current products. Be sure to use the newly released parameter files.

♦ Expansion of flash memory rewritable count and duration period

The rewritable count and duration period of flash memory will be expanded. See below for details.

	Current Products	Expanded-Specification Products ((A) Product)
Normal writing (self-/on-board programming)	100 times (maintained for 15 years)	1,000 times (maintained for 15 years)
EEPROM emulation	100 times (maintained for 15 years)	10,000 times[Notes 1, 2] (maintained for 3 years[Note 3])

Notes 1. Count when a new self-programming library to be released is used

2. Erasure count per block (up to four successive blocks can be written 10,000 times).

3. Three years after the first programming after erasure

♦ Improvement of flash memory self-programming interrupt response time

The interrupt response time during flash memory self-programming will be improved. The specifications of the current products and expanded-specification products are shown below.

Remark The following specifications will be applied to the self programming libraries described in the 78K0/Fx2 Flash Memory Self Programming Library User's Manual (Will be published June 2007).

<Current Products>

Maximum interrupt response time when using high-speed internal oscillation clock [μs] (normal model, RSTS = 1)

Library Name	Entry RAM Is Outside Short-Direct Addressing Range	Entry RAM Is Inside Short-Direct Addressing Range
Block blank check library	933.6	668.6
Block erase library	1026.6	763.6
Word write library	2505.8	1942.8
Block verify library	958.6	693.6
Set information library	476.5	211.5
EEPROM write library	2760.8	2168.8

Remark RSTS is a register that indicates the high-speed internal oscillator status (RSTS = 1: High-speed internal oscillator operation is stable).

Maximum interrupt response time when using high-speed internal oscillation clock [μs] (static model, RSTS = 1)

Library Name	Entry RAM Is Outside Short-Direct Addressing Range	Entry RAM Is Inside Short-Direct Addressing Range
Block blank check library	927.9	662.9
Block erase library	1020.9	757.9
Word write library	2497.8	1934.8
Block verify library	952.9	687.9
Set information library	475.5	210.5
EEPROM write library	2759.5	2167.5

Remark RSTS is a register that indicates the high-speed internal oscillator status (RSTS = 1: High-speed internal oscillator operation is stable).

Maximum interrupt response time when using high-speed system clock [μs] (normal model, RSTOP = 0, RSTS = 1)

Library Name	Entry RAM Is Outside Short-Direct Addressing Range	Entry RAM Is Inside Short-Direct Addressing Range
Block blank check library	179/fcpu + 507	179/fcpu + 407
Block erase library	179/fcpu + 559	179/fcpu + 460
Word write library	333/fcpu + 1589	333/fcpu + 1298
Block verify library	179/fcpu + 518	179/fcpu + 418
Set information library	80/fcpu + 370	80/fcpu + 165
EEPROM write library	29/fcpu + 1759	29/fcpu + 1468
	333/fcpu + 834	333/fcpu + 512

Remarks 1. fcpu is a CPU operating clock frequency. The maximum interrupt response time for the EEPROM write library varies depending on the clock frequency. Assign the frequency to be used, calculate the time, and take the largest value as its maximum time.

2. RSTOP is a register that sets whether to operate or stop the high-speed internal oscillator (RSTOP = 0: High-speed internal oscillator operates).

3. RSTS is a register that indicates the high-speed internal oscillator status (RSTS = 1: High-speed internal oscillator operation is stable).

Maximum interrupt response time when using high-speed system clock [μs] (normal model, RSTOP = 1)

Library Name	Entry RAM Is Outside Short-Direct Addressing Range	Entry RAM Is Inside Short-Direct Addressing Range
Block blank check library	179/fcpu + 1650	179/fcpu + 714
Block erase library	179/fcpu + 1702	179/fcpu + 767
Word write library	333/fcpu + 2732	333/fcpu + 1605
Block verify library	179/fcpu + 1661	179/fcpu + 725
Set information library	80/fcpu + 1513	80/fcpu + 472
EEPROM write library	29/fcpu + 1759	29/fcpu + 1468
	333/fcpu + 2061	333/fcpu + 873

Remarks 1. fcpu is a CPU operating clock frequency. The maximum interrupt response time for the EEPROM write library varies depending on the clock frequency. Assign the frequency to be used, calculate the time, and take the largest value as its maximum time.

2. RSTOP is a register that sets whether to operate or stop the high-speed internal oscillator (RSTOP = 1: High-speed internal oscillator stops).

Maximum interrupt response time when using high-speed system clock [μs] (static model, RSTOP = 0, RSTS = 1)

Library Name	Entry RAM Is Outside Short-Direct Addressing Range	Entry RAM Is Inside Short-Direct Addressing Range
Block blank check library	136/fcpu + 507	136/fcpu + 407
Block erase library	136/fcpu + 559	136/fcpu + 460
Word write library	272/fcpu + 1589	272/fcpu + 1298
Block verify library	136/fcpu + 518	136/fcpu + 418
Set information library	72/fcpu + 370	72/fcpu + 165
EEPROM write library	19/fcpu + 1759	19/fcpu + 1468
	268/fcpu + 834	268/fcpu + 512

Remarks 1. fcpu is a CPU operating clock frequency. The maximum interrupt response time for the EEPROM write library varies depending on the clock frequency. Assign the frequency to be used, calculate the time, and take the largest value as its maximum time.

2. RSTOP is a register that sets whether to operate or stop the high-speed internal oscillator (RSTOP = 0: High-speed internal oscillator operates).

3. RSTS is a register that indicates the high-speed internal oscillator status (RSTS = 1: High-speed internal oscillator operation is stable).

Maximum interrupt response time when using high-speed system clock [μs] (static model, RSTOP = 1)

Library Name	Entry RAM Is Outside Short-Direct Addressing Range	Entry RAM Is Inside Short-Direct Addressing Range
Block blank check library	136/fcpu + 1650	136/fcpu + 714
Block erase library	136/fcpu + 1702	136/fcpu + 767
Word write library	272/fcpu + 2732	272/fcpu + 1605
Block verify library	136/fcpu + 1661	136/fcpu + 725
Set information library	72/fcpu + 1513	72/fcpu + 472
EEPROM write library	19/fcpu + 1759	19/fcpu + 1468
	268/fcpu + 2061	268/fcpu + 873

Remarks 1. fcpu is a CPU operating clock frequency. The maximum interrupt response time for the EEPROM write library varies depending on the clock frequency. Assign the frequency to be used, calculate the time, and take the largest value as its maximum time.

2. RSTOP is a register that sets whether to operate or stop the high-speed internal oscillator (RSTOP = 1: High-speed internal oscillator stops).

<Expanded-Specification Products>

Maximum interrupt response time when using high-speed internal oscillation clock [μs] (normal model, RSTS = 1)

Library Name	Entry RAM Is Outside Short-Direct Addressing Range	Entry RAM Is Inside Short-Direct Addressing Range
Block blank check library	1100.9	431.9
Block erase library	1452.9	783.9
Word write library	1247.2	579.2
Block verify library	1125.9	455.9
Set information library	906.9	312.0
EEPROM write library	1215.2	547.2

Remark RSTS is a register that indicates the high-speed internal oscillator status (RSTS = 1: High-speed internal oscillator operation is stable).

Maximum interrupt response time when using high-speed internal oscillation clock [μs] (static model, RSTS = 1)

Library Name	Entry RAM Is Outside Short-Direct Addressing Range	Entry RAM Is Inside Short-Direct Addressing Range
Block blank check library	1095.3	426.3
Block erase library	1447.3	778.3
Word write library	1239.2	571.2
Block verify library	1120.3	450.3
Set information library	905.8	311.0
EEPROM write library	1213.9	545.9

Remark RSTS is a register that indicates the high-speed internal oscillator status (RSTS = 1: High-speed internal oscillator operation is stable).

Maximum interrupt response time when using high-speed system clock [μs] (normal model, RSTOP = 0, RSTS = 1)

Library Name	Entry RAM Is Outside Short-Direct Addressing Range	Entry RAM Is Inside Short-Direct Addressing Range
Block blank check library	179/fcpu + 567	179/fcpu + 246
Block erase library	179/fcpu + 780	179/fcpu + 459
Word write library	333/fcpu + 763	333/fcpu + 443
Block verify library	179/fcpu + 580	179/fcpu + 259
Set information library	80/fcpu + 456	80/fcpu + 200
EEPROM write library	29/fcpu + 767	29/fcpu + 447
	333/fcpu + 696	333/fcpu + 376

Remarks 1. fcpu is a CPU operating clock frequency. The maximum interrupt response time for the EEPROM write library varies depending on the clock frequency. Assign the frequency to be used, calculate the time, and take the largest value as its maximum time.

2. RSTOP is a register that sets whether to operate or stop the high-speed internal oscillator (RSTOP = 0: High-speed internal oscillator operates).

3. RSTS is a register that indicates the high-speed internal oscillator status (RSTS = 1: High-speed internal oscillator operation is stable).

Maximum interrupt response time when using high-speed system clock [μs] (normal model, RSTOP = 1)

Library Name	Entry RAM Is Outside Short-Direct Addressing Range	Entry RAM Is Inside Short-Direct Addressing Range
Block blank check library	179/fcpu + 1708	179/fcpu + 569
Block erase library	179/fcpu + 1921	179/fcpu + 782
Word write library	333/fcpu + 1871	333/fcpu + 767
Block verify library	179/fcpu + 1721	179/fcpu + 582
Set information library	80/fcpu + 1598	80/fcpu + 459
EEPROM write library	29/fcpu + 767	29/fcpu + 447
	333/fcpu + 1838	333/fcpu + 700

Remarks 1. fcpu is a CPU operating clock frequency. The maximum interrupt response time for the EEPROM write library varies depending on the clock frequency. Assign the frequency to be used, calculate the time, and take the largest value as its maximum time.

2. RSTOP is a register that sets whether to operate or stop the high-speed internal oscillator (RSTOP = 1: High-speed internal oscillator stops).

Maximum interrupt response time when using high-speed system clock [μs] (static model, RSTOP = 0, RSTS = 1)

Library Name	Entry RAM Is Outside Short-Direct Addressing Range	Entry RAM Is Inside Short-Direct Addressing Range
Block blank check library	136/fcpu + 567	136/fcpu + 246
Block erase library	136/fcpu + 780	136/fcpu + 459
Word write library	272/fcpu + 763	272/fcpu + 443
Block verify library	136/fcpu + 580	136/fcpu + 259
Set information library	72/fcpu + 456	72/fcpu + 200
EEPROM write library	19/fcpu + 767	19/fcpu + 447
	268/fcpu + 696	268/fcpu + 376

Remarks 1. fcpu is a CPU operating clock frequency. The maximum interrupt response time for the EEPROM write library varies depending on the clock frequency. Assign the frequency to be used, calculate the time, and take the largest value as its maximum time.

2. RSTOP is a register that sets whether to operate or stop the high-speed internal oscillator (RSTOP = 0: High-speed internal oscillator operates).

3. RSTS is a register that indicates the high-speed internal oscillator status (RSTS = 1: High-speed internal oscillator operation is stable).

Maximum interrupt response time when using high-speed system clock [μs] (static model, RSTOP = 1)

Library Name	Entry RAM Is Outside Short-Direct Addressing Range	Entry RAM Is Inside Short-Direct Addressing Range
Block blank check library	136/fcpu + 1708	136/fcpu + 569
Block erase library	136/fcpu + 1921	136/fcpu + 782
Word write library	272/fcpu + 1871	272/fcpu + 767
Block verify library	136/fcpu + 1721	136/fcpu + 582
Set information library	72/fcpu + 1598	72/fcpu + 459
EEPROM write library	19/fcpu + 767	19/fcpu + 447
	268/fcpu + 1838	268/fcpu + 700

Remarks 1. fcpu is a CPU operating clock frequency. The maximum interrupt response time for the EEPROM write library varies depending on the clock frequency. Assign the frequency to be used, calculate the time, and take the largest value as its maximum time.

2. RSTOP is a register that sets whether to operate or stop the high-speed internal oscillator (RSTOP = 1: High-speed internal oscillator stops).

♦ Modification of flash memory self-programming processing time

In conjunction with improvement of the flash memory self-programming interrupt response time, the flash memory self-programming processing time will be modified.

Remark The following specifications will be applied to the self programming libraries described in the 78K0/Fx2 Flash Memory Self Programming Library User's Manual (Will be published June 2007).

<Current Products>

Processing time when using high-speed internal oscillation clock
(When entry RAM is outside short-direct addressing range)

Library Name	Processing Time (μs)			
	Normal Model		Static Model	
	Min.	Max.	Min.	Max.
Self-programming start library	4.25			
Initialize library	977.75			
Mode check library	753.875		753.125	
Block blank check library	12770.875		12765.875	
Block erase library	36909.5	356318	36904.5	356296.25
Word write library	1214 (1214.375)	2409 (2409.375)	1207 (1207.375)	2402 (2402.375)
Block verify library	25618.875		25613.875	
Self-programming end library	4.25			
Get information library (optional value: 03H)	871.25 (871.375)		866 (866.125)	
Get information library (optional value: 04H)	863.375 (863.5)		858.125 (858.25)	
Get information library (optional value: 05H)	1024.75 (1043.625)		1037.5 (1038.375)	
Set information library	105524.75	790809.375	105523.75	790808.375
EEPROM write library	1496.5 (1496.875)	2691.5 (2691.875)	1489.5 (1489.875)	2684.5 (2684.875)

Remark Figures in parentheses indicate values when the write start address structure is allocated to an area other than high-speed internal RAM.

Processing time when using high-speed internal oscillation clock
(When entry RAM is inside short-direct addressing range)

Library Name	Processing Time (μs)			
	Normal Model		Static Model	
	Min.	Max.	Min.	Max.
Self-programming start library	4.25			
Initialize library	443.5			
Mode check library	219.625		218.875	
Block blank check library	12236.625		12231.625	
Block erase library	36363.25	355771.75	36358.25	355750
Word write library	679.75 (680.125)	1874.75 (1875.125)	672.75 (673.125)	1867.75 (1868.125)
Block verify library	25072.625		25067.625	
Self-programming end library	4.25			
Get information library (optional value: 03H)	337 (337.125)		331.75 (331.875)	
Get information library (optional value: 04H)	329.125 (239.25)		323.875 (324)	
Get information library (optional value: 05H)	502.25 (503.125)		497 (497.875)	
Set information library	104978.5	541143.125	104977.5	541142.125
EEPROM write library	962.25 (962.625)	2157.25 (2157.625)	955.25 (955.625)	2150.25 (2150.625)

Remark Figures in parentheses indicate values when the write start address structure is allocated to an area other than high-speed internal RAM.

Processing time when using high-speed system clock (When entry RAM is outside short-direct addressing range)

Library Name	Processing Time (μs)			
	Normal Model		Static Model	
	Min.	Max.	Min.	Max.
Self-programming start library	34/fcpu			
Initialize library	49/fcpu + 485.8125			
Mode check library	35/fcpu + 374.75		29/fcpu + 374.75	
Block blank check library	174/fcpu + 6382.0625		134/fcpu + 6382.0625	
Block erase library	174/fcpu + 31093.875	174/fcpu + 298948.125	134/fcpu + 31093.875	134/fcpu + 298948.125
Word write library	318 (321)/fcpu + 644.125	318 (321)/fcpu + 1491.625	262 (265)/fcpu + 644.125	262 (265)/fcpu + 1491.625
Block verify library	174/fcpu + 13448.5625		134/fcpu +13448.5625	
Self-programming end library	34/fcpu			
Get information library (optional value: 03H)	171 (172)/fcpu + 432.4375		129 (130)/fcpu + 432.4375	
Get information library (optional value: 04H)	181 (182)/fcpu + 427.875		139 (140)/fcpu + 427.875	
Get information library (optional value: 05H)	404 (411)/fcpu + 496.125		362 (369)/fcpu + 496.125	
Set information library	75/fcpu + 79157.6875	75/fcpu + 652400	67/fcpu + 79157.6875	67/fcpu + 652400
EEPROM write library	318 (321)/fcpu + 799.875	318 (321)/fcpu + 1647.375	262 (265)/fcpu + 799.875	262 (265)/fcpu + 1647.375

Remarks 1. Figures in parentheses indicate values when the write start address structure is allocated to an area other than high-speed internal RAM.

2. fcpu: CPU operating clock frequency

Processing time when using high-speed system clock (When entry RAM is inside short-direct addressing range)

Library Name	Processing Time (μs)			
	Normal Model		Static Model	
	Min.	Max.	Min.	Max.
Self-programming start library	34/fcpu			
Initialize library	49/fcpu + 224.6875			
Mode check library	35/fcpu +113.625		29/fcpu +113.625	
Block blank check library	174/fcpu + 6120.9375		134/fcpu + 6120.9375	
Block erase library	174/fcpu + 30820.75	174/fcpu + 298675	134/fcpu + 30820.75	134/fcpu + 298675
Word write library	318 (321)/fcpu + 383	318 (321)/fcpu + 1230.5	262 (265)/fcpu + 383	262 (265)/fcpu +1230.5
Block verify library	174/fcpu + 13175.4375		134/fcpu + 13175.4375	
Self-programming end library	34/fcpu			
Get information library (optional value: 03H)	171 (172)/fcpu + 171.3125		129 (130)/fcpu + 171.3125	
Get information library (optional value: 04H)	181 (182)/fcpu + 166.75		139 (140)/fcpu + 166.75	
Get information library (optional value: 05H)	404 (411)/fcpu + 231.875		362 (369)/fcpu + 231.875	
Set information library	75/fcpu + 78884.5625	75/fcpu + 527566.875	67/fcpu + 78884.5625	67/fcpu + 527566.875
EEPROM write library	318 (321)/fcpu + 538.75	318 (321)/fcpu + 1386.25	262 (265)/fcpu + 538.75	262 (265)/fcpu + 1386.25

Remarks 1. Figures in parentheses indicate values when the write start address structure is allocated to an area other than high-speed internal RAM.

2. fcpu: CPU operating clock frequency

<Expanded-Specification Products>

Processing time when using high-speed internal oscillation clock

(When entry RAM is outside short-direct addressing range, RSTS = 1)

Library Name	Processing Time (μs)			
	Normal Model		Static Model	
	Min.	Max.	Min.	Max.
Self-programming start library	4.0	4.5	4.0	4.5
Initialize library	1105.9	1106.6	1105.9	1106.6
Mode check library	905.7	906.1	904.9	905.3
Block blank check library	12776.1	12778.3	12770.9	12772.6
Block erase library	26050.4	349971.3	26045.3	349965.6
Word write library	1180.1 + 203 * W	1184.3 + 2241 * W	1172.9 + 203 * W	1176.3 + 2241 * W
Block verify library	25337.9	25340.2	25332.8	25334.5
Self-programming end library	4.0	4.5	4.0	4.5
Get information library (optional value: 03H)	1072.9	1075.2	1067.5	1069.1
Get information library (optional value: 04H)	1060.2	1062.6	1054.8	1056.6
Get information library (optional value: 05H)	1023.8	1028.2	1018.3	1022.1
Set information library	70265.9	759995.0	70264.9	759994.0
EEPROM write library	1316.8 + 347 * W	1320.9 + 2385 * W	1309.0 + 347 * W	1312.4 + 2385 * W

Remarks **1.** RSTS is a register that indicates the high-speed internal oscillator status (RSTS = 1: High-speed internal oscillator operation is stable).

2. The above figures indicate values when the write start address structure is allocated to an area other than high-speed internal RAM.

3. W refers to the number of write data blocks.

Processing time when using high-speed internal oscillation clock
(When entry RAM is inside short-direct addressing range, RSTS = 1)

Library Name	Processing Time (μs)			
	Normal Model		Static Model	
	Min.	Max.	Min.	Max.
Self-programming start library	4.0	4.5	4.0	4.5
Initialize library	449.5	450.2	449.5	450.2
Mode check library	249.3	249.7	248.6	248.9
Block blank check library	12119.7	12121.9	12114.6	12116.3
Block erase library	25344.7	349266.4	25339.6	349260.8
Word write library	445.8 + 203 * W	449.9 + 2241 * W	438.5 + 203 * W	441.9 + 2241 * W
Block verify library	24682.7	24684.9	24677.6	24679.3
Self-programming end library	4.0	4.5	4.0	4.5
Get information library (optional value: 03H)	417.6	419.8	412.1	413.8
Get information library (optional value: 04H)	405.0	407.4	399.5	401.3
Get information library (optional value: 05H)	367.4	371.8	361.9	365.8
Set information library	69569.3	759297.3	69568.3	759296.2
EEPROM write library	795.1 + 347 * W	799.3 + 2385 * W	787.4 + 347 * W	790.8 + 2385 * W

Remarks **1.** RSTS is a register that indicates the high-speed internal oscillator status (RSTS = 1: High-speed internal oscillator operation is stable).

2. The above figures indicate values when the write start address structure is allocated to an area other than high-speed internal RAM.

3. W refers to the number of write data blocks.

Processing time when using high-speed system clock

(When entry RAM is outside short-direct addressing range, RSTS = 1)

Library Name	Processing Time (μs)			
	Normal Model		Static Model	
	Min.	Max.	Min.	Max.
Self-programming start library	34/fcpu			
Initialize library	55/fcpu + 594	55/fcpu + 594	55/fcpu + 594	55/fcpu + 594
Mode check library	36/fcpu + 495	36/fcpu + 495	30/fcpu + 495	30/fcpu + 495
Block blank check library	179/fcpu + 6429	179/fcpu + 6429	136/fcpu + 6429	136/fcpu + 6429
Block erase library	179/fcpu + 19713	179/fcpu + 268079	136/fcpu + 19713	136/fcpu + 268079
Word write library	333/fcpu + 647 + 136 * W	333/fcpu + 647 + 1647 * W	272/fcpu + 647 + 136 * W	272/fcpu + 647 + 1647 * W
Block verify library	179/fcpu + 13284	179/fcpu + 13284	136/fcpu + 13284	136/fcpu + 13284
Self-programming end library	34/fcpu			
Get information library (optional value: 03H)	180/fcpu + 581	180/fcpu + 581	134/fcpu + 581	134/fcpu + 581
Get information library (optional value: 04H)	190/fcpu + 574	190/fcpu + 574	144/fcpu + 574	144/fcpu + 574
Get information library (optional value: 05H)	350/fcpu + 535	350/fcpu + 535	304/fcpu + 535	304/fcpu + 535
Set information library	80/fcpu + 43181	80/fcpu + 572934	72/fcpu + 43181	72/fcpu + 572934
EEPROM write library	333/fcpu + 729 + 209 * W	333/fcpu + 729 + 1722 * W	268/fcpu + 729 + 209 * W	268/fcpu + 729 + 1722 * W

Remarks 1. fcpu: CPU operating clock frequency

2. RSTS is a register that indicates the high-speed internal oscillator status (RSTS = 1: High-speed internal oscillator operation is stable).

3. The above figures indicate values when the write start address structure is allocated to an area other than high-speed internal RAM.

4. W refers to the number of write data blocks.

Processing time when using high-speed system clock

(When entry RAM is inside short-direct addressing range, RSTS = 1)

Library Name	Processing Time (μs)			
	Normal Model		Static Model	
	Min.	Max.	Min.	Max.
Self-programming start library	34/fcpu			
Initialize library	55/fcpu + 272	55/fcpu + 272	55/fcpu + 272	55/fcpu + 272
Mode check library	36/fcpu + 173	36/fcpu + 173	30/fcpu + 173	30/fcpu + 173
Block blank check library	179/fcpu + 6108	179/fcpu + 6108	136/fcpu + 6108	136/fcpu + 6108
Block erase library	179/fcpu + 19371	179/fcpu + 267738	136/fcpu + 19371	136/fcpu + 267738
Word write library	333/fcpu + 247 + 136 * W	333/fcpu + 247 + 1647 * W	272/fcpu + 247 + 136 * W	272/fcpu + 247 + 1647 * W
Block verify library	179/fcpu + 12964	179/fcpu + 12964	136/fcpu + 12964	136/fcpu + 12964
Self-programming end library	34/fcpu			
Get information library (optional value: 03H)	180/fcpu + 261	180/fcpu + 261	134/fcpu + 261	134/fcpu + 261
Get information library (optional value: 04H)	190/fcpu + 254	190/fcpu + 254	144/fcpu + 254	144/fcpu + 254
Get information library (optional value: 05H)	350/fcpu + 213	350/fcpu + 213	304/fcpu + 213	304/fcpu + 213
Set information library	80/fcpu + 42839	80/fcpu + 572592	72/fcpu + 42839	72/fcpu + 572592
EEPROM write library	333/fcpu + 516 + 209 * W	333/fcpu + 516 + 1722 * W	268/fcpu + 516 + 209 * W	268/fcpu + 516 + 1722 * W

Remarks 1. fcpu: CPU operating clock frequency

2. RSTS is a register that indicates the high-speed internal oscillator status (RSTS = 1: High-speed internal oscillator operation is stable).

3. The above figures indicate values when the write start address structure is allocated to an area other than high-speed internal RAM.

4. W refers to the number of write data blocks.