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Technical Notification</td><td>Document No.</td><td colspan="2">ZBG-CC-07-0021</td><td>1/8</td></tr>
<tr><td>Date issued</td><td colspan="3">October 1, 2007</td></tr>
<tr><td rowspan="2">Related documents
78K0R/KE3 User's Manual: U17854EJ6V0UD00 (6th edition)
78K0R/KF3 User's Manual: U17893EJ5V0UD00 (5th edition)
78K0R/KG3 User's Manual: U17894EJ6V0UD00 (6th edition)
78K0R/KH3 User's Manual: U18432EJ2V0UD00 (2nd edition)
78K0R/KJ3 User's Manual: U18417EJ2V0UD00 (2nd edition)</td><td>Issued by</td><td colspan="3">1st Product Solution Group
Multipurpose Microcomputer Systems Division
Microcomputer Operations Unit
NEC Electronics Corporation</td></tr>
<tr><td rowspan="4">Notification classification</td><td>√</td><td colspan="2">Usage restriction</td></tr>
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1. Affected products

All 78K0R/Kx3 microcontroller products

78K0R/KE3: μPD78F1142, μPD78F1143, μPD78F1144, μPD78F1145, μPD78F1146

78K0R/KF3: μPD78F1152, μPD78F1153, μPD78F1154, μPD78F1155, μPD78F1156

78K0R/KG3: μPD78F1162, μPD78F1163, μPD78F1164, μPD78F1165, μPD78F1166, μPD78F1167, μPD78F1168

78K0R/KH3: μPD78F1174, μPD78F1175, μPD78F1176, μPD78F1177, μPD78F1178

78K0R/KJ3: μPD78F1184, μPD78F1185, μPD78F1186, μPD78F1187, μPD78F1188

2. Notification

There are restrictions and erroneous descriptions in the user's manual for 78K0R/Kx3 microcontrollers.

Overview of restrictions and erroneous descriptions:

♦ Restriction on clock output/buzzer output controller

Description:

The level of the clock output/buzzer output may be kept high if a frequency-divided clock other than the original oscillation clock (f_{MAIN}, f_{SUB}) is selected for the output clock in the CKS register (by setting bits CSELn, CCSn2, CCSn1 and CCSn0) and the clock output and buzzer output are disabled (by clearing the PCLOEn bit).

Temporary workaround:

Select the original oscillation clock (f_{MAIN}, f_{SUB}) in the CKS register after disabling the clock output and the buzzer output (by clearing the PCLOEn bit) by the software.

Parmanent workaround:

This issue is planned for correction. The product name after the correction will be μPD78F11xxA.

♦ Restriction on real-time counter 1

Description:

When a constant-period interrupt and alarm interrupt are generated at the same time, the alarm detection status flag (WAFG) is set about 30.52 μs after the occurrence of the constant-period interrupt status flag (RIFG).

Temporary workaround:

Check the WAFG flag after about 30.52 μs or more have elapsed since the occurrence of the INTRTC interrupt, by using the software.

Parmanent workaround:

This issue is planned for correction. The product name after the correction will be μPD78F11xxA.

♦ Restriction on real-time counter 2

Description:

If the real-time counter (RTC) is stopped (RTCE bit of RTCC0 register is cleared) when the count value of the sub-count register (RSUBC) reaches 7FFDH[Note] or 7FFEH[Note], the count-up of the second, minute, hour, day, week, month, and year count registers may not stop.

Note 7FFDH ±correction value or 7FFEH ±correction value when watch error correction is performed

Temporary workaround:

Set the wait control before stopping the real-time counter.

Parmanent workaround:

This issue is planned for correction. The product name after the correction will be μPD78F11xxA.

♦ Erroneous descriptions in Cautions on writing to the RTCC1 register

Description:

There is an erroneous description in Caution for real-time counter control register 1 (RTCC1). For details, refer to attachment 6.

3. Document revision history

78K0R/Kx3 Microcontrollers Technical Notification

Document Number	Issued on	Description
ZBG-CC-07-0021	October 1, 2007	1st edition (this notification)

List of 78K0R/Kx3 Microcontroller Usage Restrictions

1. Usage Restriction History

No.	Description	KE3: μPD78 F1142, F1143, F1144, F1145, F1146 KF3: μPD78F1152, F1153, F1154, F1155, F1156 KG3: μPD78F1162, F1163, F1164, F1165, F1166, F1167, F1168 KH3: μPD78F1174, F1175, F1176, F1177, F1178 KJ3: μPD78F1184, F1185, F1186, F1187, F1188	KE3 μPD78F1142A, F1143A, F1144A, F1145A, F1146A KF3: μPD78F1152A, F1153A, F1154A, F1155A, F1156A KG3: μPD78F1162A, F1163A, F1164A, F1165A, F1166A, F1167A, F1168A KH3: μPD78F1174A, F1175A, F1176A, F1177A, F1178A KJ3: μPD78F1184A, F1185A, F1186A, F1187A, F1188A
1	Restriction on output level when the clock output and buzzer output controller is stopped	×	○
2	Real-time counter (RTC)		
2-1	Restriction on simultaneous use of constant-period interrupt and alarm interrupt of real-time counter	×	○
2-2	Restriction on year, month, week, day, hour, minute and second count registers after real-time counter operation is stopped	×	○

Remark The meaning of each symbol is as follows.

×: Restriction applicable

○: Restriction not applicable (correction is planned)

2. Restriction Details

Item 1: See attachment 3 for details.

Item 2-1: See attachment 4 for details.

Item 2-2: See attachment 5 for details.

3. Supplement

For a detailed schedule of products in which the restrictions are corrected (μPD78F11xxA), contact an NEC Electronics sales representative.

List of Corrections to 78K0R/Kx3 Microcontroller User's Manual

1. Correction and Addition to Specification Update

No.	Description / Edition	78K0R/KE3		78K0R/KF3		78K0R/KG3		78K0R/KH3		78K0R/KJ3	
		6th or Earlier	7th	5th or Earlier	6th	6th or Earlier	7th	2nd or Earlier	3rd	2nd or Earlier	3rd
1	Erroneous description concerning writing to RTCC1 register of real-time counter	×	○	×	○	×	○	×	○	×	○

Remark The meaning of each symbol is as follows.

×: Error

○: Corrected (correction is planned)

2. Modification Details

Item 1: See attachment 6 for details.

Item 1 – Usage restriction: Restriction on output level when the clock output and buzzer output controller is stopped

[Description]

Usage affected by this restriction:

The usage affected by this restriction is the case where a frequency-divided clock other than the original oscillation clock (f_{MAIN}, f_{SUB}) is selected in the CKS register (by setting bits CSELn, CCSn2, CCSn1 and CCSn0), and the clock output and buzzer output are disabled (by clearing the PCLOEn bit).

Phenomenon

The level of the clock output/buzzer output must be low when the output is disabled, but in the usage mentioned above, the output stops at the level (high or low) for which the output was disabled.

[Temporary workaround (restriction)]

The output level will become low by selecting the original oscillation clock (f_{MAIN}, f_{SUB}) in the CKS register after the clock output and the buzzer output are disabled (by clearing the PCLOEn bit). Note that the output level will be low after a high pulse with a different width from the original one has been output.

[Permanent workaround]

Devices will be corrected so that the output is stopped at the low level even under the above-mentioned usage. Refer to the *List of 78K0R/Kx3 Microcontroller Usage Restrictions* in attachment 1 for the products subject to correction.

Remark n = 0, 1

Item 2-1 - Usage restriction: Restriction on simultaneous use of constant-period interrupt and alarm interrupt of real-time counter

[Description]

Usage affected by this restriction:

The usage affected by this restriction is the case where constant-period interrupts are enabled (CT2, CT1 and CT0 bits of RTCC0 register are not set to “0, 0, 0”), alarm interrupts are enabled (WALE and WALIE bits of RTCC1 register = 1), and a constant-period interrupt and an alarm interrupt are generated at the same time.

The cases where either constant-period interrupts or alarm interrupts are enabled, or both interrupts are enabled but are not generated concurrently, are not affected.

Phenomenon:

When an INTRTC interrupt occurs under the above-mentioned condition, the RIFG flag of the RTCC1 register is set at the same time. The WAFG flag is set one subsystem clock (about 30.52 μs) after the occurrence of the INTRTC interrupt. Consequently, the WAFG flag may be read during INTRTC interrupt servicing without being set yet.

[Temporary workaround (usage restriction)]

If an INTRTC interrupt occurs under the above-mentioned condition, first check the interrupt status flag RIFG. If RIFG = 1 (a constant-period interrupt has occurred), check the WAFG flag after one subsystem clock (about 30.52 μs) has elapsed since the occurrence of the INTRTC interrupt. If RIFG = 0 (no constant-period interrupts have occurred), it does not need to wait for one subsystem clock before reading the WAFG flag.

[Permanent workaround]

Devices will be corrected so that the WAFG and RIFG flags are set at the same time as the above-mentioned INTRTC interrupt occurrence. Refer to the *List of 78K0R/Kx3 Microcontroller Usage Restrictions* in attachment 1 for the products subject to correction.

Item 2-2 - Usage restriction: Restriction on year, month, week, day, hour, minute and second count registers after real-time counter operation is stopped

[Description]

Usage affected by this restriction:

The usage affected by this restriction is the case where the real-time counter (RTC) is stopped (RTCE bit of RTCC0 register is cleared) when the count value of the sub-count register (RSUBC) reaches 7FFDH**Note** or 7FFEH**Note**.

Phenomenon:

The RTCE bit is cleared to “0” under the above-mentioned condition, but the second count register (SEC) may not stop and continues to count up at the f_{SUB} cycles. In such a case, the minute, hour, day, week, month, and year count registers will also continue to count up.

[Temporary workaround (usage restriction)]

Before stopping the RTC (clearing the RTCE bit), first set the RWAIT bit of the RTCC1 register, and then confirm that the RWST flag is set to “1”. Before resuming the RTC operation, set the RTCE bit and then clear the RWAIT bit. This procedure stops RTC when the RTCE bit is cleared and thus prevents the SEC register from counting up.

[Permanent workaround]

Devices will be corrected so that the second count register (SEC) is stopped under the above-mentioned usage. Refer to the *List of 78K0R/Kx3 Microcontroller Usage Restrictions* in attachment 1 for the products subject to correction.

Note 7FFDH ±correction value or 7FFEH ±correction value when watch error correction is performed

Item 1 – Correction: Erroneous description concerning writing to RTCC1 register of real-time counter

There is an erroneous description on Caution for real-time counter control register 1 (RTCC1) in the chapter pertaining to real-time counter in the user's manual.

[Description]

The user's manual states that an 8-bit manipulation instruction, instead of a 1-bit manipulation instruction, should be used to write to the WAFG or RIFG flag, but other bits of this register must be written with an 8-bit manipulation instruction, in addition to the WAFG and RIFG flags.

Incorrect:

Caution If writing is performed to the WAFG flag with a 1-bit manipulation instruction[Note], the RIFG flag may be cleared. Therefore, to perform writing to the WAFG flag, be sure to use an 8-bit manipulation instruction, and at this time, set 1 to the RIFG flag to invalidate writing. In the same way, to perform writing to the RIFG flag, use an 8-bit manipulation instruction and set 1 the WAFR flag.

Correct:

Caution If writing is performed to the RTCC1 register with a 1-bit manipulation instruction, the RIFG and WAFG flags may be cleared. Therefore, to perform writing to the RTCC1 register, be sure to use an 8-bit manipulation instruction. To prevent the RIFG and WAFG flags from being cleared upon write, set these bits to 1 so as to make writing to these bits invalid. A 1-bit manipulation instruction can still be used to write to this register, as long as the RIFG and WAFG flags are not used and, therefore, changes in these flag values do not cause any problem.

Note Refer to the *78K0R Microcontrollers Instruction User's Manual* (U17792EJ4V0UM00) for details on the 1-bit manipulation instruction.

[Modification schedule]

The user's manual will be corrected with the next revision.