78K0/Kx2 Microcontrollers Document Modification	Document No.	ZBG-CC-08-0013	1/1
	Date issued	July 14, 2008	
	Issued by	Product Solution Group Multipurpose Microcomputer Systems Division Microcomputer Operations Unit NEC Electronics Corporation	
Related documents 78K0/Kx2 User's Manual: U18598EJ1V0UD00 (1st edition)	Notification classification		Usage restriction
			Upgrade
		√	Document modification
			Other notification

1. Affected products

78K0/Kx2 microcontroller products:

78K0/KB2 : μPD78F0500A, μPD78F0501A, μPD78F0502A, μPD78F0503A, μPD78F0503DA

78K0/KC2 : μPD78F0511A, μPD78F0512A, μPD78F0513A, μPD78F0514A, μPD78F0515A, μPD78F0513DA, μPD78F0515DA

78K0/KD2 : μPD78F0521A, μPD78F0522A, μPD78F0523A, μPD78F0524A, μPD78F0525A, μPD78F0526A, μPD78F0527A, μPD78F0527DA

78K0/KE2 : μPD78F0531A, μPD78F0532A, μPD78F0533A, μPD78F0534A, μPD78F0535A, μPD78F0536A, μPD78F0537A, μPD78F0537DA

78K0/KF2 : μPD78F0544A, μPD78F0545A, μPD78F0546A, μPD78F0547A, μPD78F0547DA

Note. this notification affect users manual of specification-expansion products(μPD78F05xxA), not affect users manual of conventional-specification products(μPD78F05xx).

2. Notification

There are erroneous descriptions in the user's manual for the 78K0/Kx2 microcontrollers.

Summary:

There are erroneous descriptions in chapters for A/D converter, Serial interface IIC0, Interrupt function and Standby function. See the attachment for details.

3. Document revision history

78K0/Kx2 Microcontrollers Document Modification

Document Number	Date Issued	Description
ZBG-CC-08-0013	July 14, 2008	Corrections to 78K0/Kx2 user's manual (This notification)

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List of Corrections to 78K0/Kx2 Microcontroller User's Manual (U18598EJ1V0UD00)

[Details of Correction]

Page	Part	Content	
p.402	CHAPTER 13 A/D CONVERTER	Modification of **Table 13-2. A/D Conversion Time Selection**	<1>
p.565	CHAPTER 18 SERIAL INTERFACE IIC0	Modification of **Table 18-4. Extension Code Bit Definitions** and addition of Remark	<2>
pp.602 to 607		Modification of **Figure 18-27. Example of Master to Slave Communication** and **Figure 18-28. Example of Slave to Master Communication**	<3>
p.659	CHAPTER 22 STANDBY FUNCTION	Modification of Note 1 in **Figure 22-3. HALT Mode Release by Interrupt Request Generation**	<4>
p.663		Addition of Caution to **Table 22-3. Operating Statuses in STOP Mode**	<5>
pp.664 to 666		Modification of Note 2 in **Figure 22-5. Operating Timing When STOP Mode Is Released (When Unmasked Interrupt Request Is Generated),** and Note **Figure 22-6. STOP Mode Release by Interrupt Request Generation**	<6>

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<1> Modification of **Table 13-2. A/D Conversion Time Selection** (p.402)

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Table 13-2. A/D Conversion Time Selection

(1) 2.7 V ≤ AV_{REF} ≤ 5.5 V (LV0 = 0)

A/D Converter Mode Register (ADM)					Conversion Time Selection					Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz Note	
0	0	0	0	0	264/f_{PRS}	Setting prohibited	52.8 μs	26.4 μs	13.2 μs Note	f_{PRS}/12
0	0	1	0	0	176/f_{PRS}		35.2 μs	17.6 μs	8.8 μs Note	f_{PRS}/8
0	1	0	0	0	132/f_{PRS}	66.0 μs	26.4 μs	13.2 μs	6.6 μs Note	f_{PRS}/6
0	1	1	0	0	88/f_{PRS}	44.0 μs	17.6 μs	8.8 μs Note	Setting prohibited	f_{PRS}/4
1	0	0	0	0	66/f_{PRS}	33.0 μs	13.2 μs	6.6 μs Note		f_{PRS}/3
1	0	1	0	0	44/f_{PRS}	22.0 μs	8.8 μs Note	Setting prohibited		f_{PRS}/2
Other than above					Setting prohibited					

Note This can be set only when 4.0 V ≤ AV_{REF} ≤ 5.5 V.

(2) 2.3 V ≤ AV_{REF} < 5.5 V (LV0 = 1)

A/D Converter Mode Register (ADM)					Conversion Time Selection					Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz Note 2	f_{PRS} = 20 MHz Note 1	
0	0	0	0	1	480/f_{PRS}	Setting prohibited	Setting prohibited	48.0 μs Note 2	24.0 μs Note 1	f_{PRS}/12
0	0	1	0	1	320/f_{PRS}		64.0 μs	32.0 μs Note 2	16.0 μs Note 1	f_{PRS}/8
0	1	0	0	1	240/f_{PRS}		48.0 μs	24.0 μs Note 2	12.0 μs Note 1	f_{PRS}/6
0	1	1	0	1	160/f_{PRS}		32.0 μs	16.0 μs Note 2	8.0 μs Note 1	f_{PRS}/4
1	0	0	0	1	120/f_{PRS}	60.0 μs	24.0 μs Note 2	12.0 μs Note 2	Setting prohibited	f_{PRS}/3
1	0	1	0	1	80/f_{PRS}	40.0 μs	16.0 μs Note 2	8.0 μs Note 1		f_{PRS}/2
Other than above					Setting prohibited					

Notes 1. This can be set only when 4.0 V ≤ AV_{REF} ≤ 5.5 V.

2. This can be set only when 2.7 V ≤ AV_{REF} ≤ 5.5 V.

Cautions 1. Set the conversion times with the following conditions.

(1) 2.7 V ≤ AV_{REF} ≤ 5.5 V (LV0 = 0)

- **4.0 V ≤ AV_{REF} ≤ 5.5 V: f_{AD} = 0.33 to 3.61 MHz**
- **2.7 V ≤ AV_{REF} < 4.0 V: f_{AD} = 0.33 to 1.8 MHz**

(2) 2.3 V ≤ AV_{REF} ≤ 5.5 V (LV0 = 1)

- **4.0 V ≤ AV_{REF} ≤ 5.5 V: f_{AD} = 0.6 to 6.56 MHz**
- **2.7 V ≤ AV_{REF} < 4.0 V: f_{AD} = 0.6 to 3.28 MHz**
- **2.3 V ≤ AV_{REF} < 2.7 V: f_{AD} = 0.6 to 1.48 MHz**

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<Correct>

Table 13-2. A/D Conversion Time Selection

(1) 2.7 V ≤ AV_{REF} ≤ 5.5 V (LV0 = 0)

A/D Converter Mode Register (ADM)					Conversion Time Selection					Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz	
0	0	0	0	0	264/f_{PRS}	Setting prohibited	52.8 μs	26.4 μs	13.2 μs	f_{PRS}/12
0	0	1	0	0	176/f_{PRS}		35.2 μs	17.6 μs	8.8 μs Note	f_{PRS}/8
0	1	0	0	0	132/f_{PRS}	66.0 μs	26.4 μs	13.2 μs	6.6 μs Note	f_{PRS}/6
0	1	1	0	0	88/f_{PRS}	44.0 μs	17.6 μs	8.8 μs Note	Setting prohibited	f_{PRS}/4
1	0	0	0	0	66/f_{PRS}	33.0 μs	13.2 μs	6.6 μs Note		f_{PRS}/3
1	0	1	0	0	44/f_{PRS}	22.0 μs	8.8 μs Note	Setting prohibited		f_{PRS}/2
Other than above					Setting prohibited					

Note This can be set only when 4.0 V ≤ AV_{REF} ≤ 5.5 V.

(2) 2.3 V ≤ AV_{REF} < 5.5 V (LV0 = 1)

A/D Converter Mode Register (ADM)					Conversion Time Selection					Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz Note 2	f_{PRS} = 20 MHz Note 2	
0	0	0	0	1	480/f_{PRS}	Setting prohibited	Setting prohibited	48.0 μs Note 2	24.0 μs Note 2	f_{PRS}/12
0	0	1	0	1	320/f_{PRS}		64.0 μs	32.0 μs Note 2	16.0 μs Note 1	f_{PRS}/8
0	1	0	0	1	240/f_{PRS}		48.0 μs	24.0 μs Note 2	12.0 μs Note 1	f_{PRS}/6
0	1	1	0	1	160/f_{PRS}		32.0 μs	16.0 μs Note 1	Setting prohibited	f_{PRS}/4
1	0	0	0	1	120/f_{PRS}	60.0 μs	24.0 μs Note 2	12.0 μs Note 1		f_{PRS}/3
1	0	1	0	1	80/f_{PRS}	40.0 μs	16.0 μs Note 1	Setting prohibited		f_{PRS}/2
Other than above					Setting prohibited					

Notes 1. This can be set only when 4.0 V ≤ AV_{REF} ≤ 5.5 V.

2. This can be set only when 2.7 V ≤ AV_{REF} ≤ 5.5 V.

Cautions 1. Set the conversion times with the following conditions.

(1) 2.7 V ≤ AV_{REF} ≤ 5.5 V (LV0 = 0)

- **4.0 V ≤ AV_{REF} ≤ 5.5 V: f_{AD} = 0.33 to 3.6 MHz**
- **2.7 V ≤ AV_{REF} < 4.0 V: f_{AD} = 0.33 to 1.8 MHz**

(2) 2.3 V ≤ AV_{REF} ≤ 5.5 V (LV0 = 1)

- **4.0 V ≤ AV_{REF} ≤ 5.5 V: f_{AD} = 0.6 to 3.6 MHz**
- **2.7 V ≤ AV_{REF} < 4.0 V: f_{AD} = 0.6 to 1.8 MHz**
- **2.3 V ≤ AV_{REF} < 2.7 V: f_{AD} = 0.6 to 1.48 MHz**

<2> **Table 18-4. Extension Code Bit Definitions** and addition of Remark (p.565)

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Table 18-4. Extension Code Bit Definitions

Slave Address	R/W Bit	Description
0 0 0 0 0 0 0	0	General call address
0 0 0 0 0 0 0	1	Start byte
0 0 0 0 0 0 1	×	C-BUS address
0 0 0 0 0 1 0	×	Address that is reserved for different bus format
1 1 1 1 0 X X	×	10-bit slave address specification

<Correct>

Table 18-4. Bit Definitions of Main Extension Codes

Slave Address	R/W Bit	Description
0 0 0 0 0 0 0	0	General call address
1 1 1 1 0 X X	0	10-bit slave address specification (for address authentication)
1 1 1 1 0 X X	1	10-bit slave address specification (for read command issuance after address match)

Remark For extension codes other than the above, refer to THE I^2C-BUS SPECIFICATION published by NXP

<3> Modification of **Figure 18-27. Example of Master to Slave Communication** and **Figure 18-28. Example of Slave to Master Communication** (pp.602 to 607)

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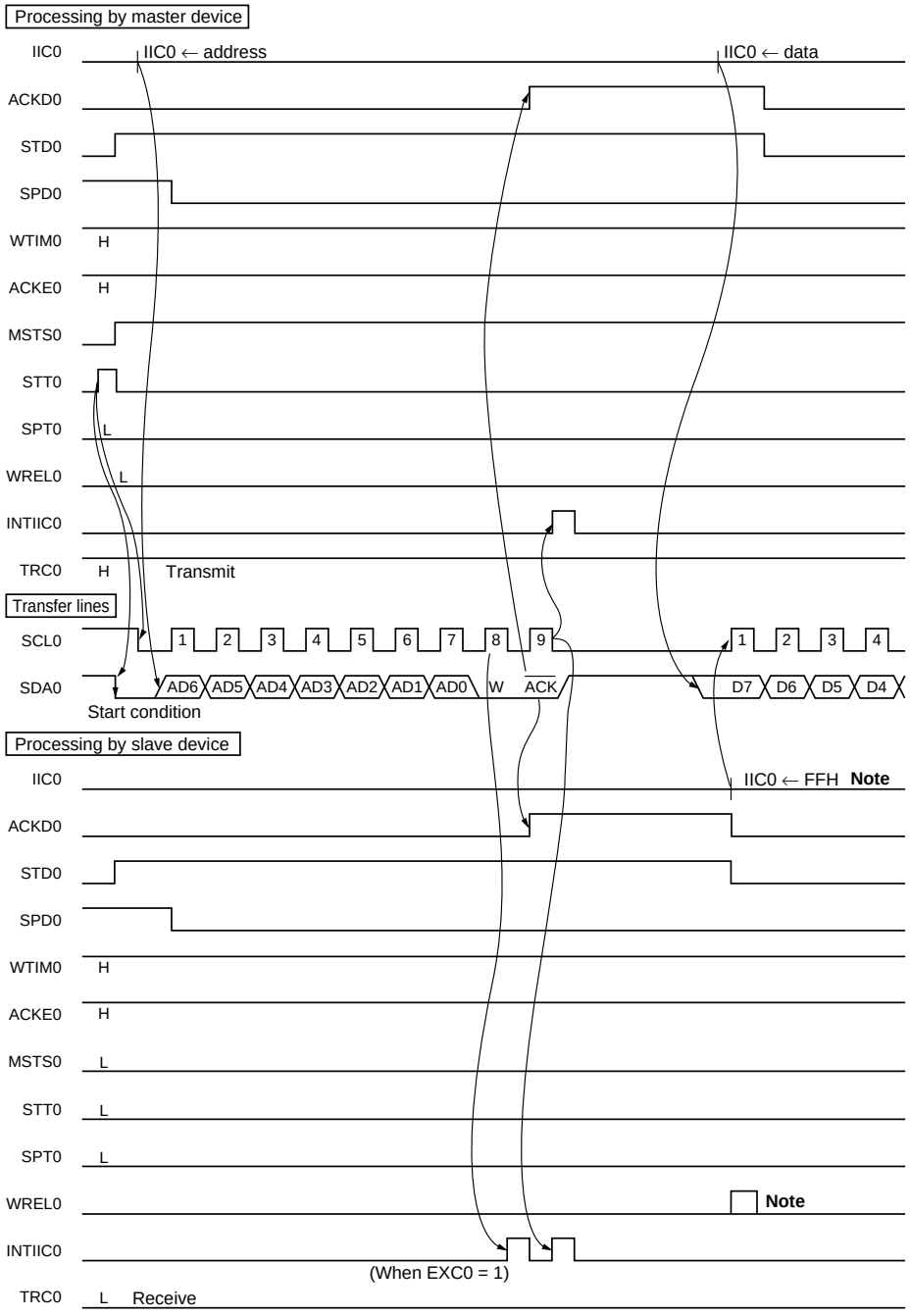
Figure 18-27. Example of Master to Slave Communication
(When 9-Clock Wait Is Selected for Both Master and Slave) (1/3)

(1) Start condition ~ address

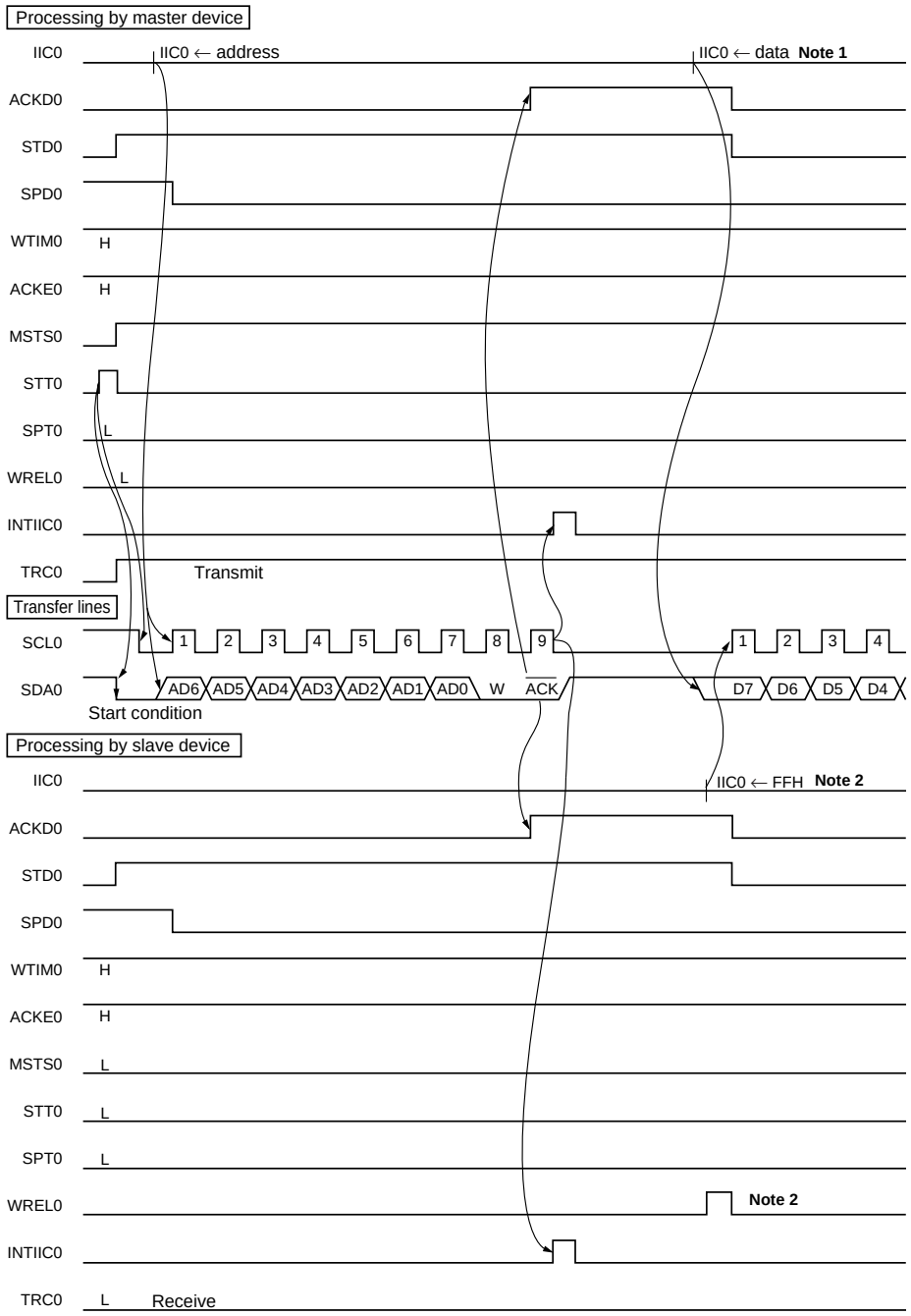


Note To cancel slave wait, write “FFH” to IIC0 or set WREL0.

<Correct>

Figure 18-27. Example of Master to Slave Communication
(When 9-Clock Wait Is Selected for Both Master and Slave) (1/3)

(1) Start condition ~ address



Notes 1. Write data to IIC0, not setting WREL0, in order to cancel a wait state during master transmission.

2. To cancel slave wait, write “FFH” to IIC0 or set WREL0.

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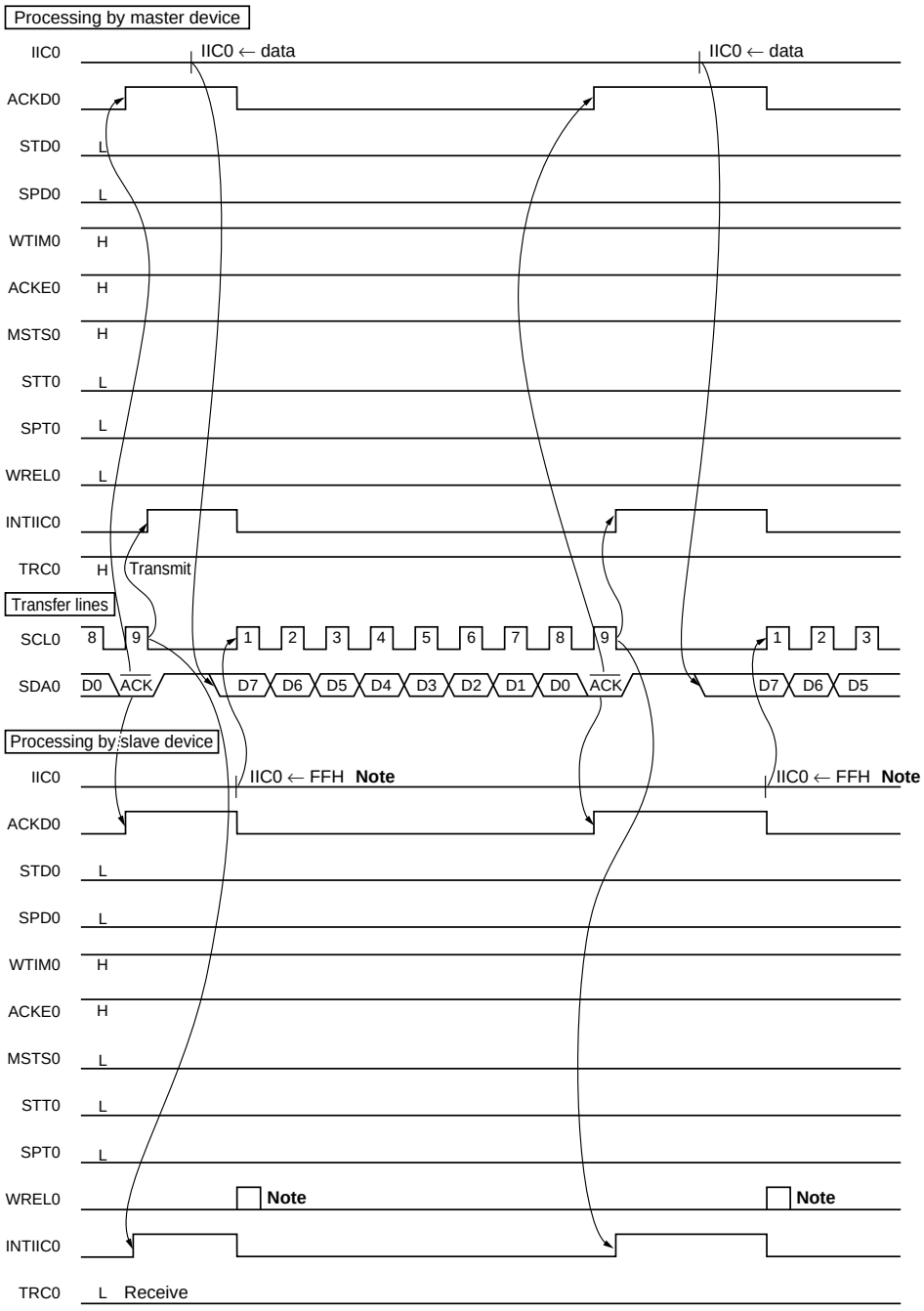
Figure 18-27. Example of Master to Slave Communication
(When 9-Clock Wait Is Selected for Both Master and Slave) (2/3)

(2) Data

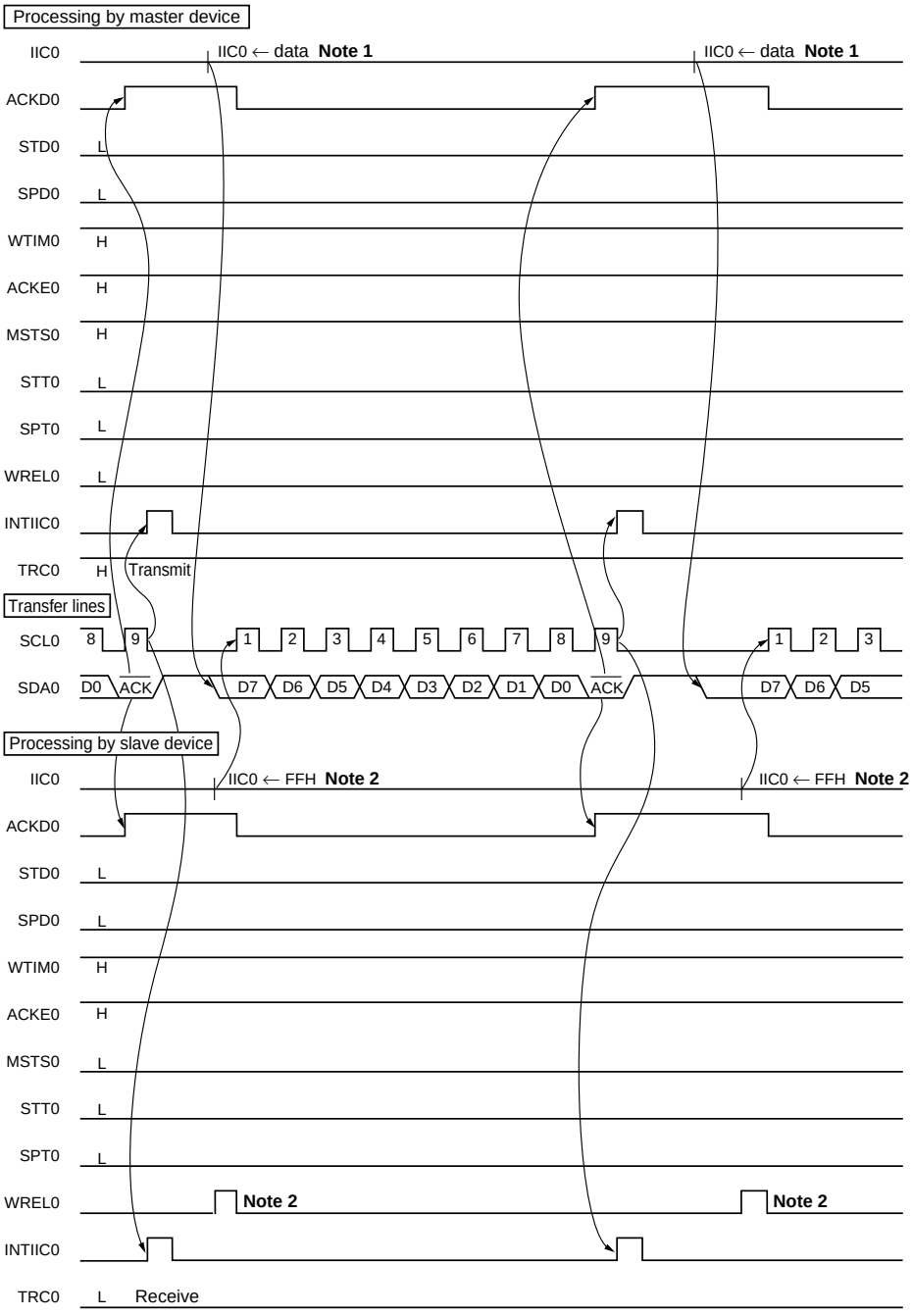


Note To cancel slave wait, write “FFH” to IIC0 or set WREL0.

<Correct>

Figure 18-27. Example of Master to Slave Communication
(When 9-Clock Wait Is Selected for Both Master and Slave) (2/3)

(2) Data



Notes 1. Write data to IIC0, not setting WREL0, in order to cancel a wait state during master transmission.

2. To cancel slave wait, write “FFH” to IIC0 or set WREL0.

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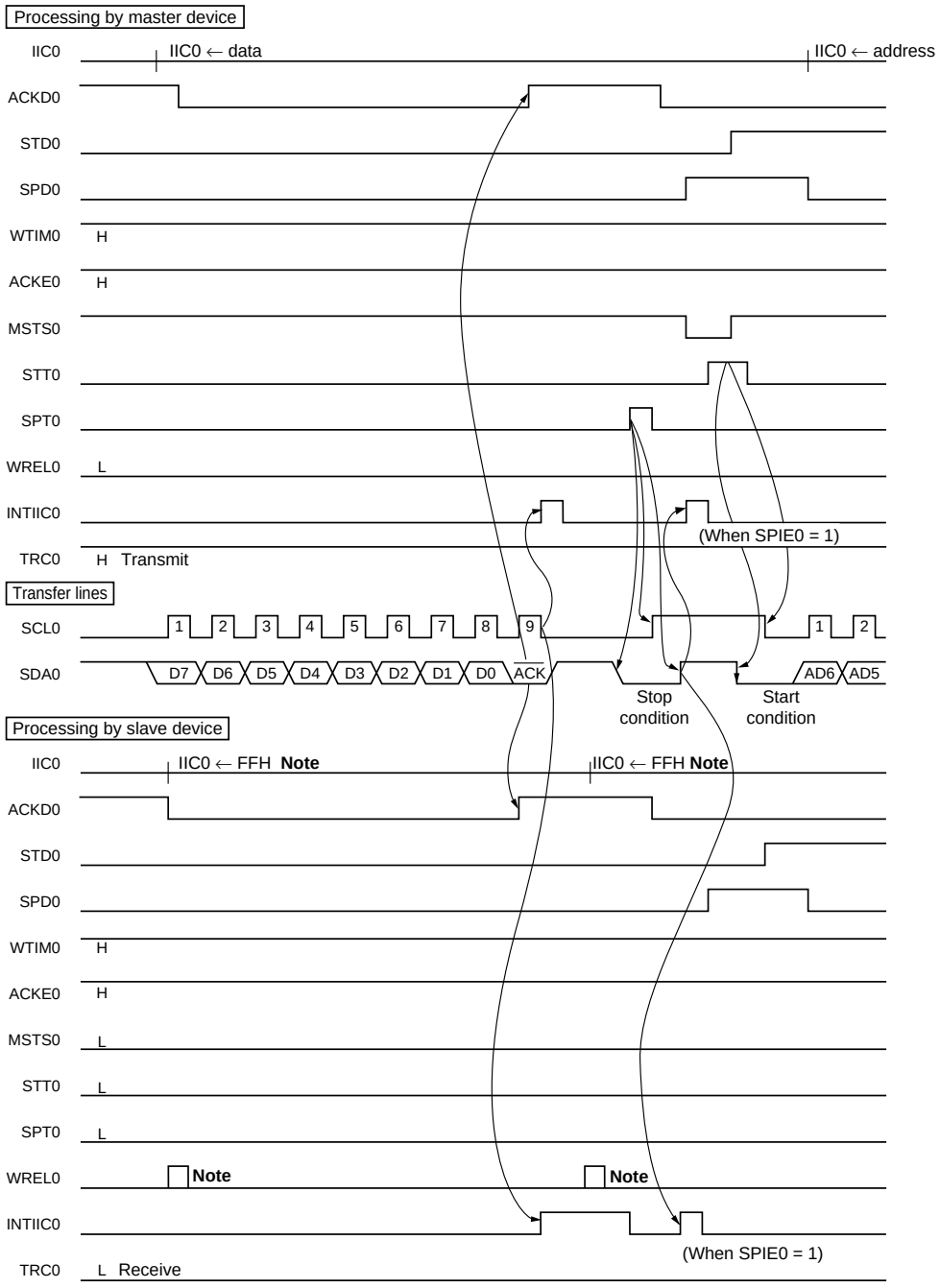
Figure 18-27. Example of Master to Slave Communication
(When 9-Clock Wait Is Selected for Both Master and Slave) (3/3)

(3) Stop condition

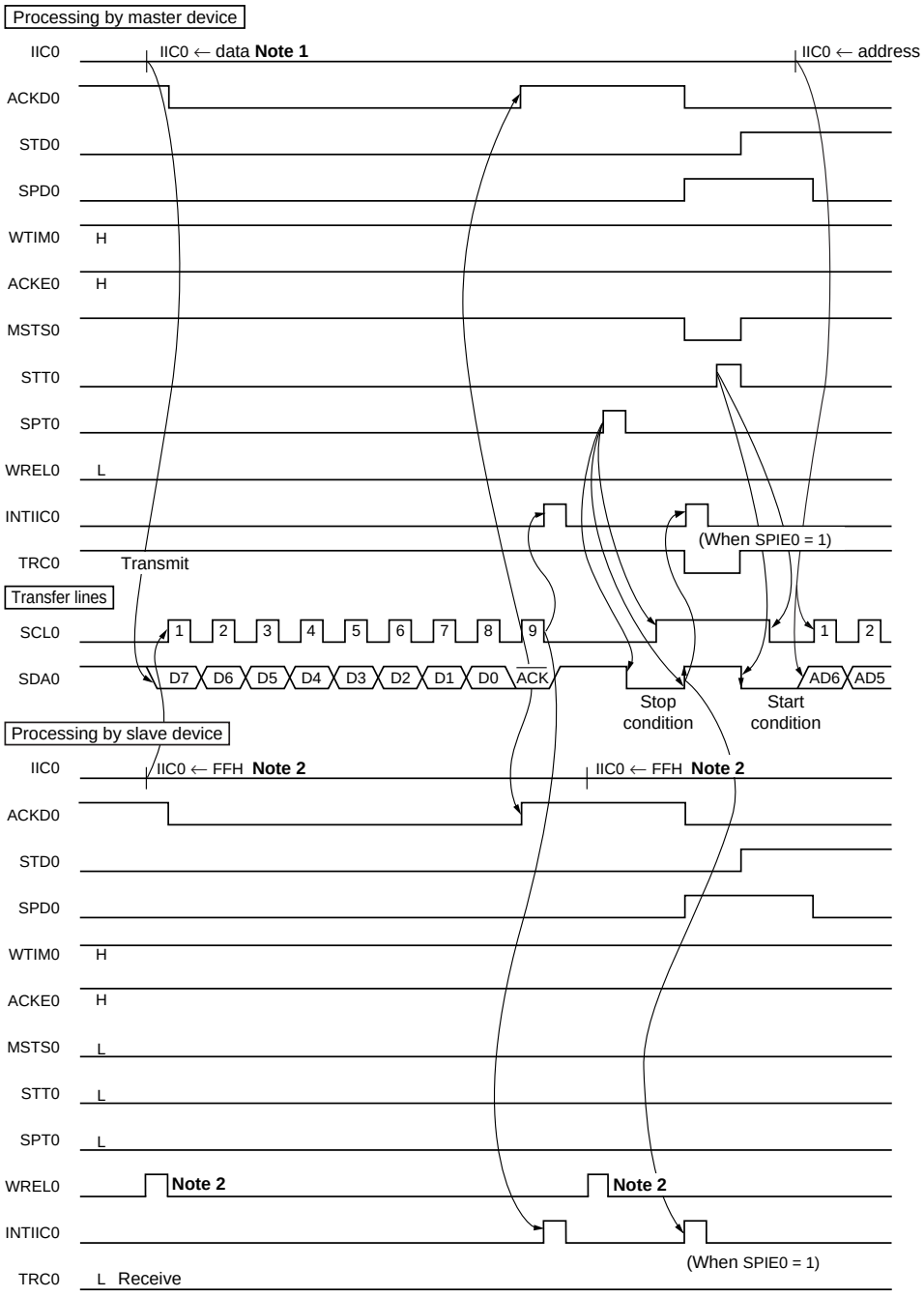


Note To cancel slave wait, write “FFH” to IIC0 or set WREL0.

<Correct>

Figure 18-27. Example of Master to Slave Communication
(When 9-Clock Wait Is Selected for Both Master and Slave) (3/3)

(3) Stop condition



Notes 1. Write data to IIC0, not setting WREL0, in order to cancel a wait state during master transmission.

2. To cancel slave wait, write “FFH” to IIC0 or set WREL0.

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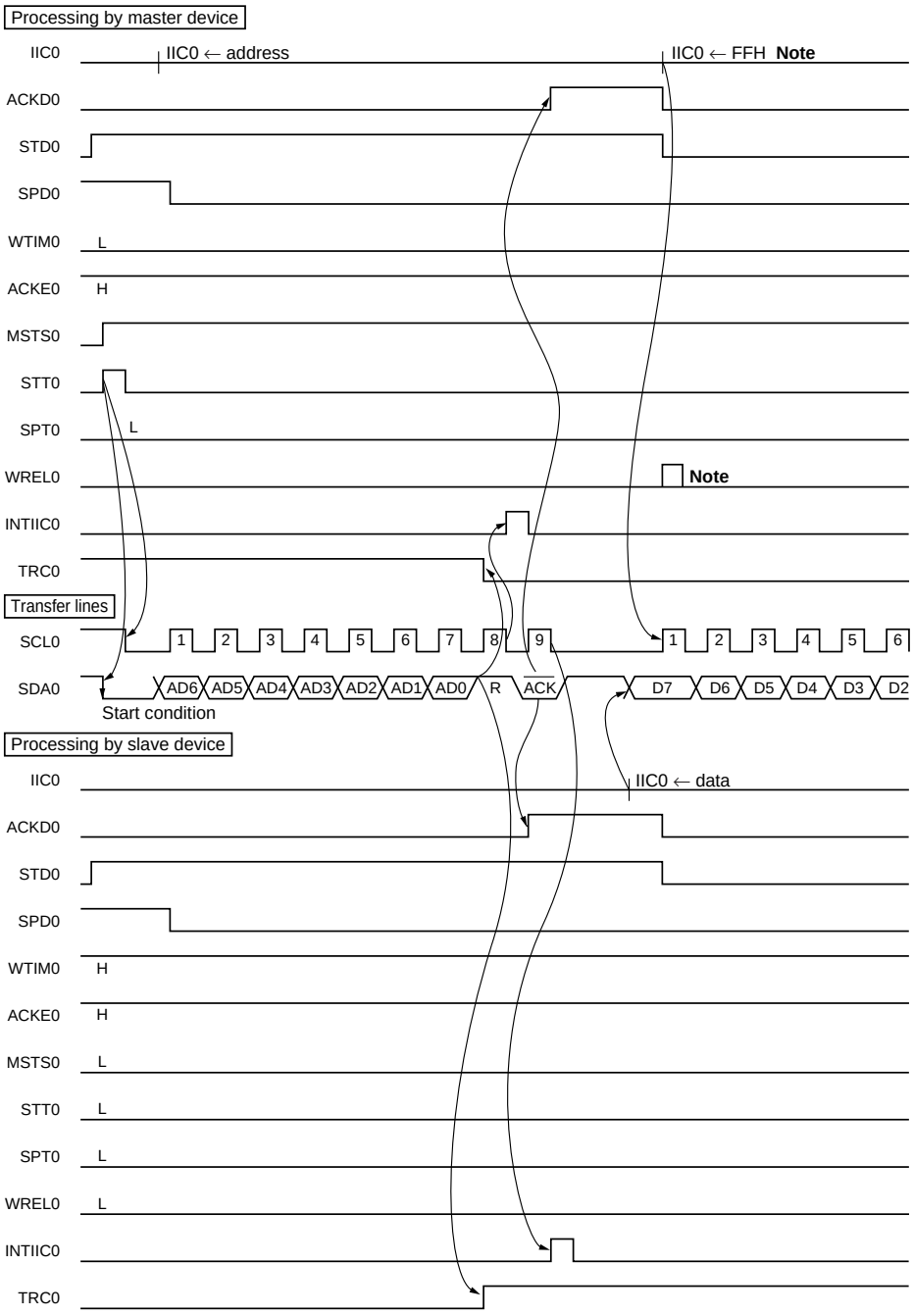
Figure 18-28. Example of Slave to Master Communication
(When 8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/3)

(1) Start condition ~ address



Note To cancel master wait, write “FFH” to IIC0 or set WREL0.

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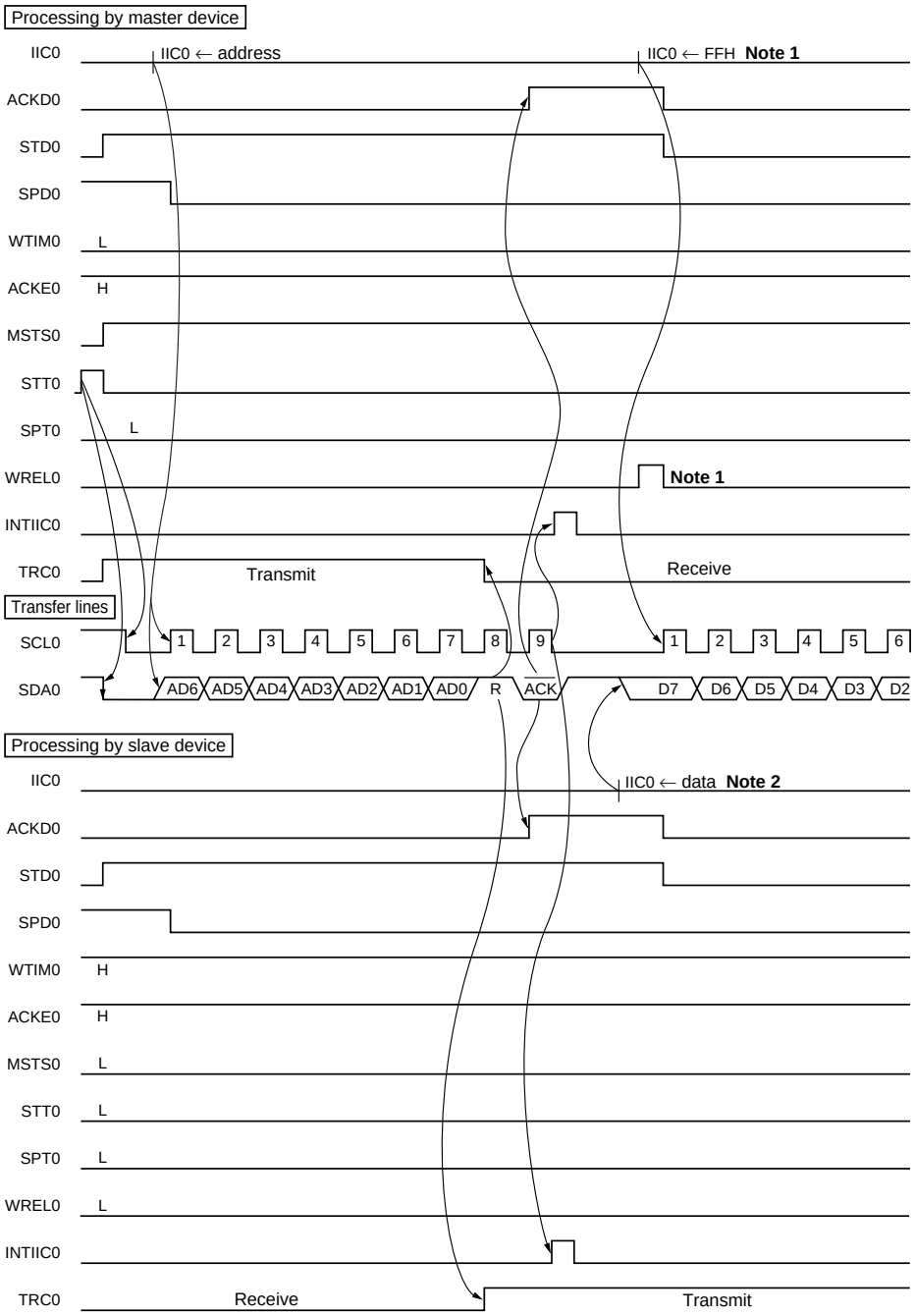
Figure 18-28. Example of Slave to Master Communication
(When 8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/3)

(1) Start condition ~ address



Notes 1. To cancel master wait, write “FFH” to IIC0 or set WREL0.

2. Write data to IIC0, not setting WREL0, in order to cancel a wait state during slave transmission.

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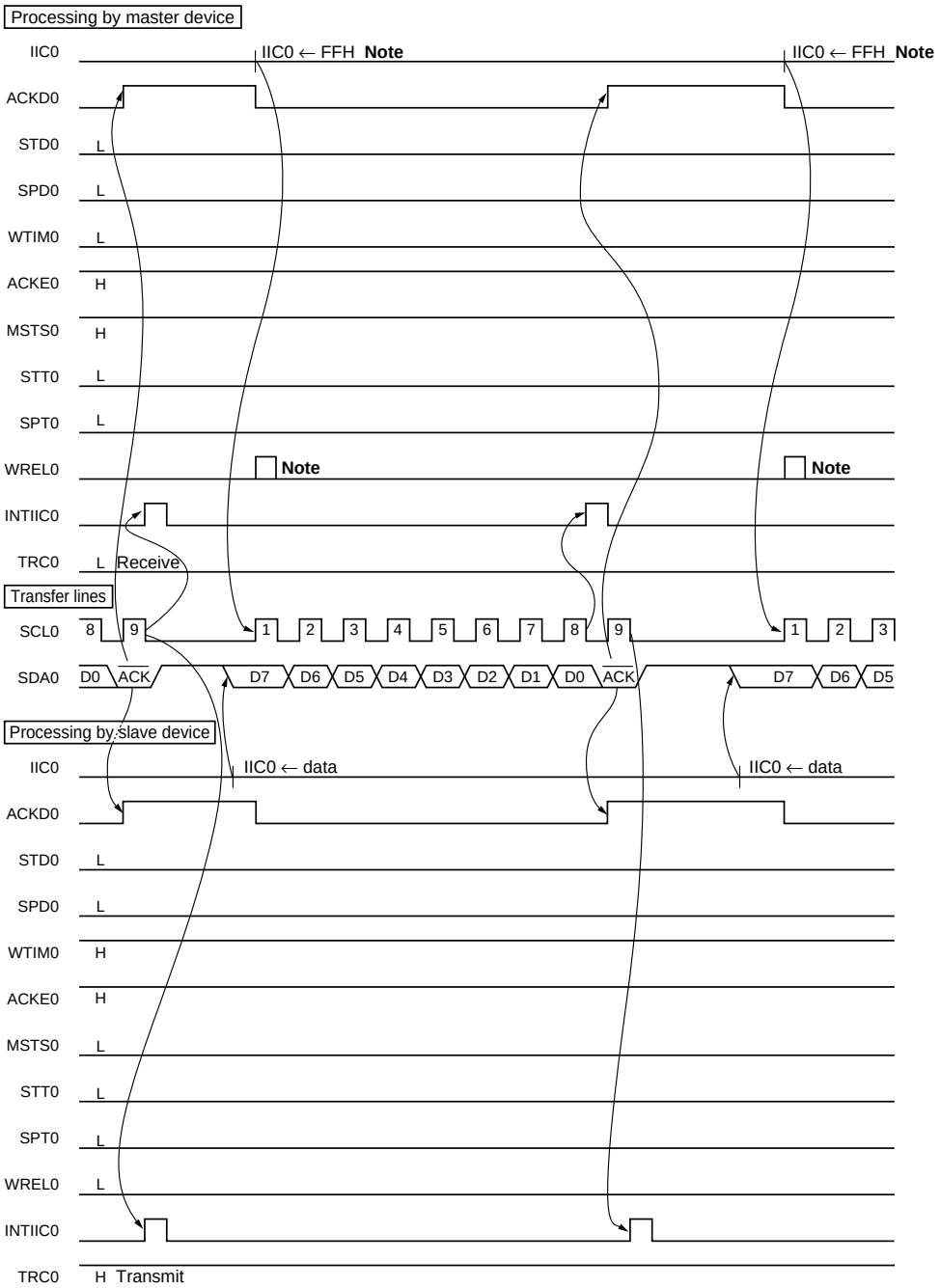
Figure 18-28. Example of Slave to Master Communication
(When 8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (2/3)

(2) Data

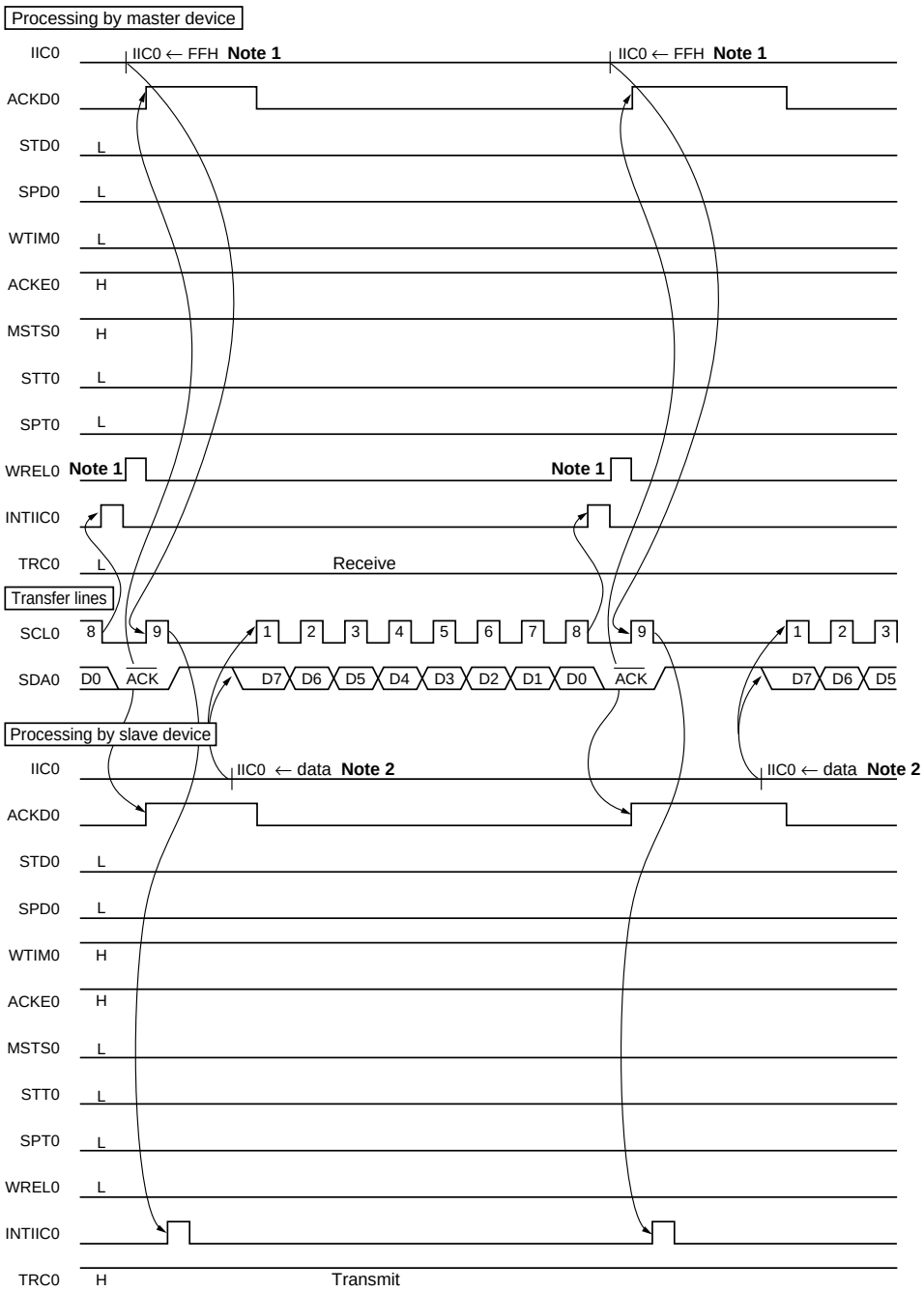


Note To cancel master wait, write “FFH” to IIC0 or set WREL0.

<Correct>

Figure 18-28. Example of Slave to Master Communication
(When 8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (2/3)

(2) Data



Notes 1. To cancel master wait, write “FFH” to IIC0 or set WREL0.

2. Write data to IIC0, not setting WREL0, in order to cancel a wait state during slave transmission.

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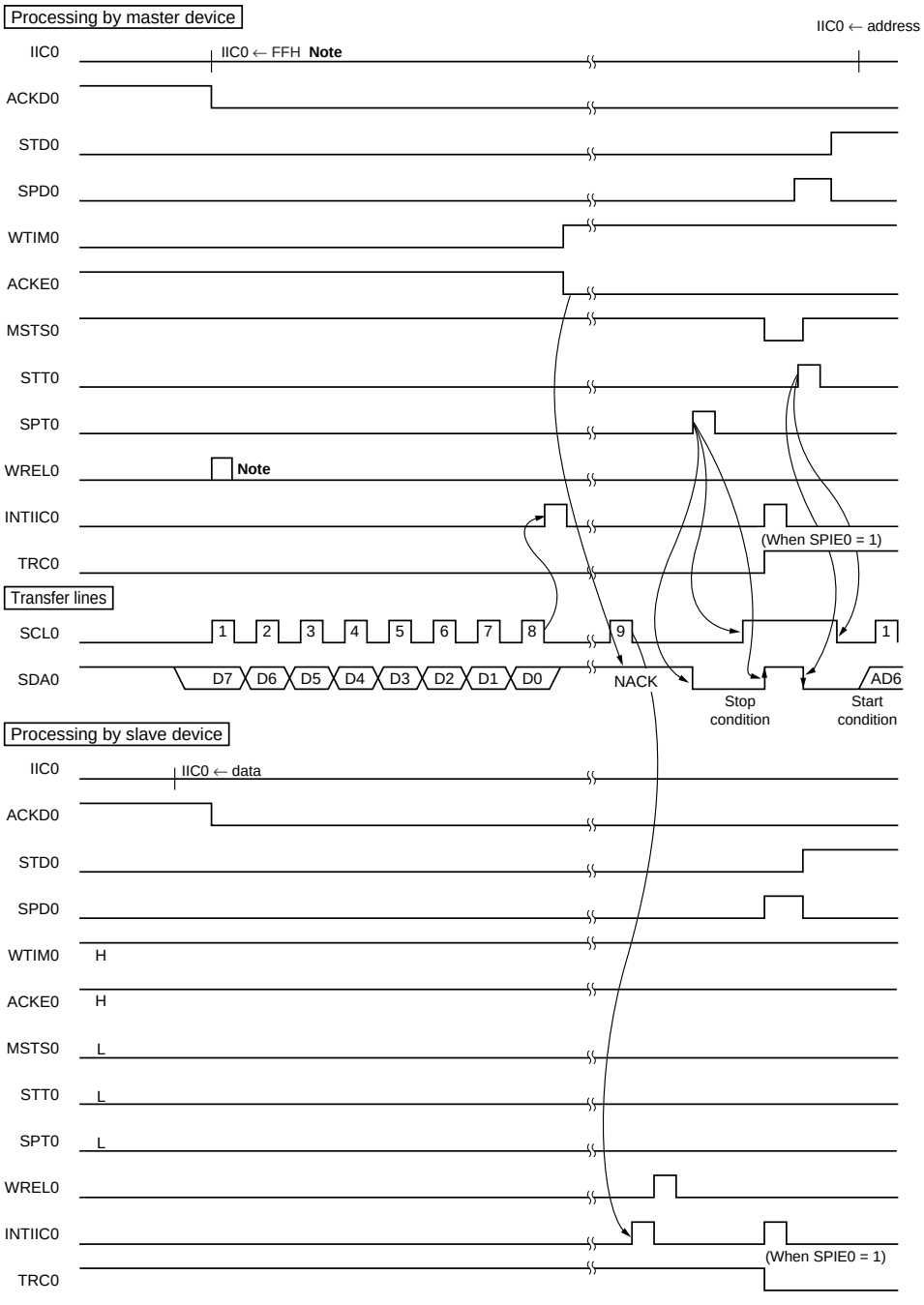
Figure 18-28. Example of Slave to Master Communication

(When 8-Clock and 9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (3/3)

(3) Stop condition

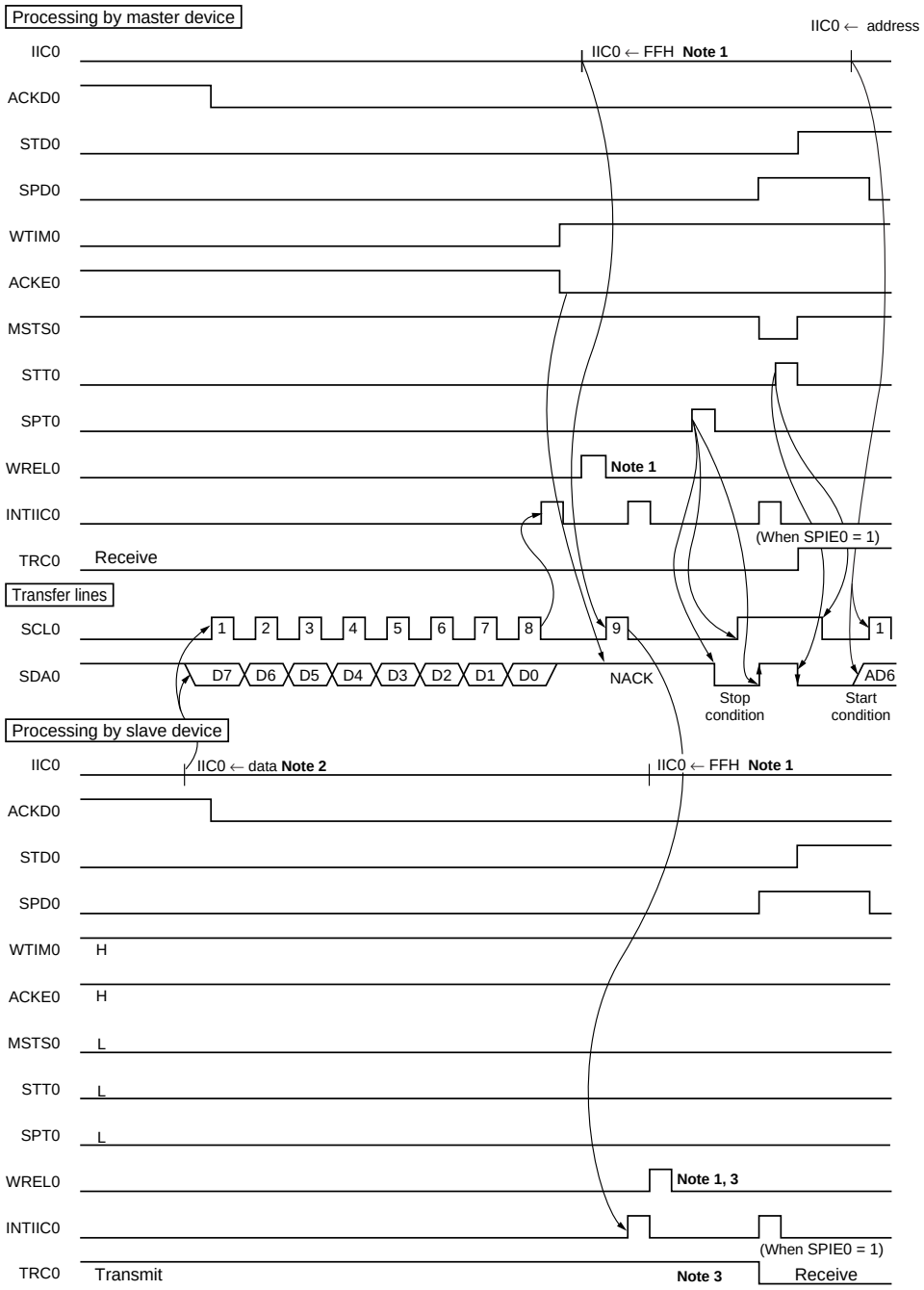


Note To cancel master wait, write “FFH” to IIC0 or set WREL0.

<Correct>

Figure 18-28. Example of Slave to Master Communication
(When 8-Clock and 9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (3/3)

(3) Stop condition



Notes 1. To cancel wait, write “FFH” to IIC0 or set WREL0.

2. Write data to IIC0, not setting WREL0, in order to cancel a wait state during slave transmission.

3. If a wait state during slave transmission is canceled by setting WREL0, TRC0 will be cleared.

<4> Modification of Note 1 in **Figure 22-3. HALT Mode Release by Interrupt Request Generation** (p.659)

<Error>

Note 1. The wait time is as follows:

- When vectored interrupt servicing is carried out: 8 or 9 clocks
- When vectored interrupt servicing is not carried out: 2 or 3 clocks

<Correct>

Note 1. The wait time is as follows:

- When vectored interrupt servicing is carried out: 11 or 12 clocks
- When vectored interrupt servicing is not carried out: 4 or 5 clocks

<5> Addition of Caution to **Table 22-3. Operating Statuses in STOP Mode** (p.663)

Caution Execute the STOP instruction after having confirmed that the internal high-speed oscillator is operating stably (RSTS = 1).

<6> Modification of Note 2 in **Figure 22-5. Operating Timing When STOP Mode Is Released (When Unmasked Interrupt Request Is Generated),** and Note **Figure 22-6. STOP Mode Release by Interrupt Request Generation** (pp.664 to 666)

Note The wait time is as follows:

- When vectored interrupt servicing is carried out: 8 or 9 clocks
- When vectored interrupt servicing is not carried out: 2 or 3 clocks

<Correct>

Note The wait time is as follows:

- When vectored interrupt servicing is carried out: 17 or 18 clocks
- When vectored interrupt servicing is not carried out: 11 or 12 clocks