NEC

Customer Notification

78K0/Kx2

8-Bit Single-Chip Microcontrollers

Operating Precautions

78K0/KB2
78K0/KC2
78K0/KD2
78K0/KE2
78K0/KF2

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78K0/Kx2

(A) Related Products

List of related products:

78K0/KB2:
μPD78F0500, μPD78F0501, μPD78F0502, μPD78F0503, μPD78F0503D
μPD78F0500(A), μPD78F0501(A), μPD78F0502(A), μPD78F0503(A)
μPD78F0500(A2), μPD78F0501(A2), μPD78F0502(A2), μPD78F0503(A2)

78K0/KC2:
μPD78F0511, μPD78F0512, μPD78F0513, μPD78F0514, μ78F0515, μ78F0513D, μ78F0515D
μPD78F0511(A), μPD78F0512(A), μPD78F0513(A), μPD78F0514(A), μPD78F0515(A)
μPD78F0511(A2), μPD78F0512(A2), μPD78F0513(A2), μPD78F0514(A2), μPD78F0515(A2)

78K0/KD2:
μPD78F0521, μPD78F0522, μPD78F0523, μPD78F0524, μ78F0525,
μPD78F0526, μPD78F0527, μPD78F0527D
μPD78F0521(A), μPD78F0522(A), μPD78F0523(A), μPD78F0524(A), μPD78F0525(A),
μPD78F0526(A), μPD78F0527(A)
μPD78F0521(A2), μPD78F0522(A2), μPD78F0523(A2), μPD78F0524(A2), μPD78F0525(A2),
μPD78F0526(A2), μPD78F0527(A2)

78K0/KE2:
μPD78F0531, μPD78F0532, μPD78F0533, μPD78F0534, μ78F0535,
μPD78F0536, μPD78F0537, μPD78F0537D
μPD78F0531(A), μPD78F0532(A), μPD78F0533(A), μPD78F0534(A), μPD78F0535(A),
μPD78F0536(A), μPD78F0537(A)
μPD78F0531(A2), μPD78F0532(A2), μPD78F0533(A2), μPD78F0534(A2), μPD78F0535(A2),
μPD78F0536(A2), μPD78F0537(A2)

78K0/KF2:
μPD78F0544, μ78F0545, μPD78F0546, μPD78F0547, μPD78F0547D
μPD78F0544(A), μPD78F0545(A), μPD78F0546(A), μPD78F0547(A)
μPD78F0544(A2), μPD78F0545(A2), μPD78F0546(A2), μPD78F0547(A2)

(B) Table of Operating Precautions

Product Group 1:

No.	Outline		**µPD78F050x (x = 0, 1, 2, 3) µPD78F051x (x = 1, 2, 3) µPD78F052x (x = 1, 2, 3) µPD78F053x (x = 1, 2, 3)**			
		Rev.	ES	CS, MP		
		Rank[Note]	I	K		
1	Clock generator STOP instruction execution (Direction of Use)		×	×		
2	Flash memory Flash memory programming (Direction of Use)		×	×		
3	Low-Voltage Detector Reset function and writing to CRC00 (Direction of Use)		×	×		

Product Group 2:

No.	Outline		**µPD78F051x (x = 4, 5) µPD78F052x (x = 4, 5, 6, 7) µPD78F053x (x = 4, 5, 6, 7) µPD78F054x (x = 4, 5, 6, 7) µPD78F0503D, µPD78F0513D, µPD78F0515D, µPD78F0527D, µPD78F0537D, µPD78F0547D**			
		Rev.	ES	CS, MP		
		Rank[Note]	I	K, E, X		
1	Clock generator STOP instruction execution (Direction of Use)		×	×		
2	Flash memory Flash memory programming (Direction of Use)		×	×		

✓: Not applicable
× applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

(C) Description of Operating Precautions

No. 1	Clock generator STOP instruction execution (Direction of Use)

Details

If the microcontroller is using the internal high-speed oscillator (fRH) as the CPU clock, then when a STOP instruction is executed, under certain circumstances the device will enter a state of undefined operation and it will not exit from STOP mode by interrupt. There are certain timing conditions between the execution of the STOP instruction and the internal high speed oscillator which cause this situation and they are listed below.

The instruction is executed 888-889 clock cycles after the internal high speed oscillator is enabled (RSTOP set to 0).
The instruction is executed 888-889 clock cycles after the device exits from STOP mode, and the CPU was operating from the high speed internal oscillator prior to entering STOP mode and continues to operate from the same clock source when it exits STOP mode.
The instruction is executed 408-701 clock cycles after the device finishes initializing after a non-POC (power up) Reset; i.e. WDT, LVI, external reset.

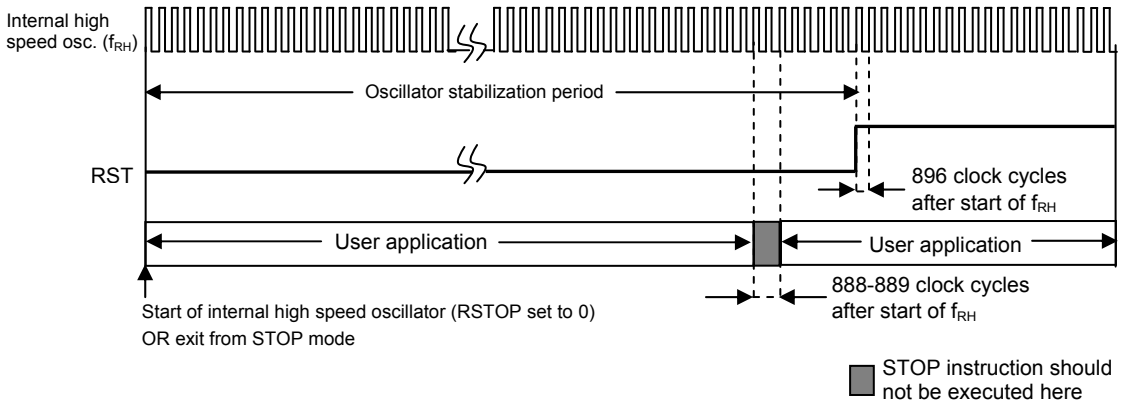


Fig. 1－1 Operation of internal high-speed oscillator after initial starting or after exit from STOP mode

NOTE: Figure is not drawn to scale.

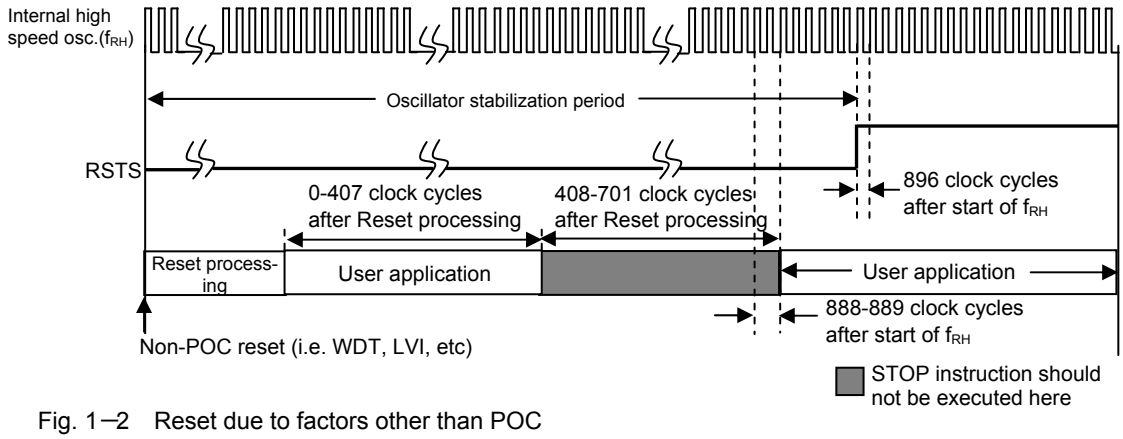


Fig. 1－2 Reset due to factors other than POC

NOTE: Figure is not drawn to scale

When one of the described situations occurs, the device abnormally enters into STOP mode. As a result, the following conditions occur-

- The device will not exit STOP mode when an interrupt occurs
- The internal high speed oscillator does not stop. Hence the current consumption is greater than what is specified for STOP mode; approximately 150-400uA.

If the watchdog timer is enabled (WDTON=1) and it is configured to operate in STOP mode (Option Byte->LSROSC=1), then it can Reset the device once the counter overflows and release the device from STOP mode.

Workaround

This condition can be avoided using a software modification. There are two different modifications which can be utilized.

1) Postpone the execution of the STOP instruction until a check is performed on the RSTS bit and it is verified that it is 1.
2) A delay is implemented in the software such that it can be insured that the STOP instruction will not be executed until after the previously mentioned conditions have passed.

It is suggested to use modification (1) if the STOP instruction will be executed during interrupt processing.

Following is a table of application conditions and which modifications will work for each.

Application condition	Modification	
	(1)	(2)
STOP instruction will be executed shortly after the internal high speed oscillator starts operation	✓	✓
STOP instruction will be executed shortly after exiting STOP mode	✓	✓
STOP instruction will be executed shortly after a non-POC reset	✓	✓
The time from which the internal high speed oscillator starts to when the STOP instruction will be executed can not be defined	✓	✗

✓: modification will work

✗ : modification will not work

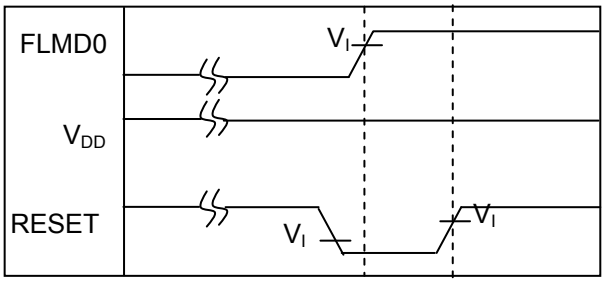
No. 2	Flash memory Flash memory programming (Direction of Use)

Details

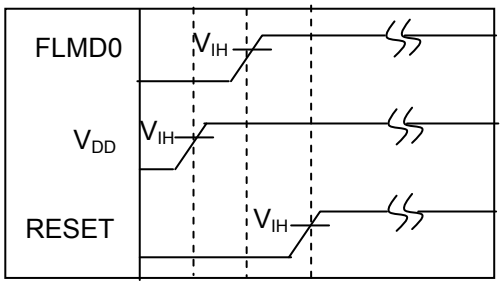
There is an issue with the device not entering into flash programming mode. There are two situations in which the microcontroller may not enter into the programming mode and they are listed below.

- When the Run After Disconnect function is used during programming with the flash memory programmer (PG-FP5) or MINICUBE2.
- When the programming environment has been configured based on the Application Note (Programmer) (U17739EJ2V0AN00) and when entering into flash programming mode during user program operation (Figure 2-1 (1))

Even if either of the above situations exists, the device may still correctly enter into programming mode and the flash can be successfully programmed. If the verify indicates correct programming, then the flash programming worked correctly.
This issue is not applicable for the circumstances listed below.
• When entering into the programming mode at the same time as power-on
• When performing self programming
• When performing EEPROM emulation



① Entering into flash programming mode during user program operation



② Entering into flash programming mode at the same time as power-on

Figure 2-1 Methods of entering flash memory programming mode

If the duration of the reset signal applied to the external RESET pin is shorter than 1,950 ms when entering the flash programming mode during user program operation without dropping the power supply voltage to the level of the POC detection voltage (VPOC = 1.59 V ±0.15 V), the following phenomenon may occur.
• A POC reset occurs upon reset release and the flash memory programming mode is not entered normally. Consequently, the user program is executed without performing programming processing.

Workaround

Secure a reset period for 1,950 ms or longer by controlling the external RESET pin when entering the flash memory programming mode.

For those configuring the programming environment based on the Application Note (Programmer) (U17739EJ2V0AN00). Please apply and use the workaround.
For 3rd party programmers please contact directly the manufacturer of your programmer.

No. 3	Low-Voltage Detector Reset function and writing to CRC00 (Direction of Use)

Details

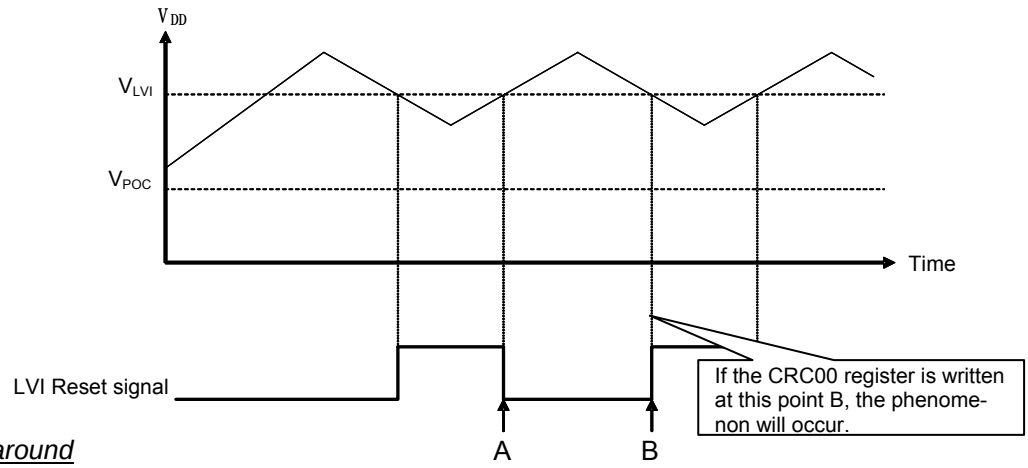
If a reset is generated from the Low Voltage Detection (LVI) function at the same time that the CRC00 register is being written, then one or more bits of the LVIM register can be changed to High (1).

- Low voltage detect pin will be changed to “EXLVI” pin.

If a Reset is generated from any other source besides LVI, this phenomenon does not occur.

When VDD falls below V_{LVI} a Reset from the LVI is generated. If data is written to the CRC00 register at the same time that the reset signal is generated, then incorrect data can be written to the LVIM register

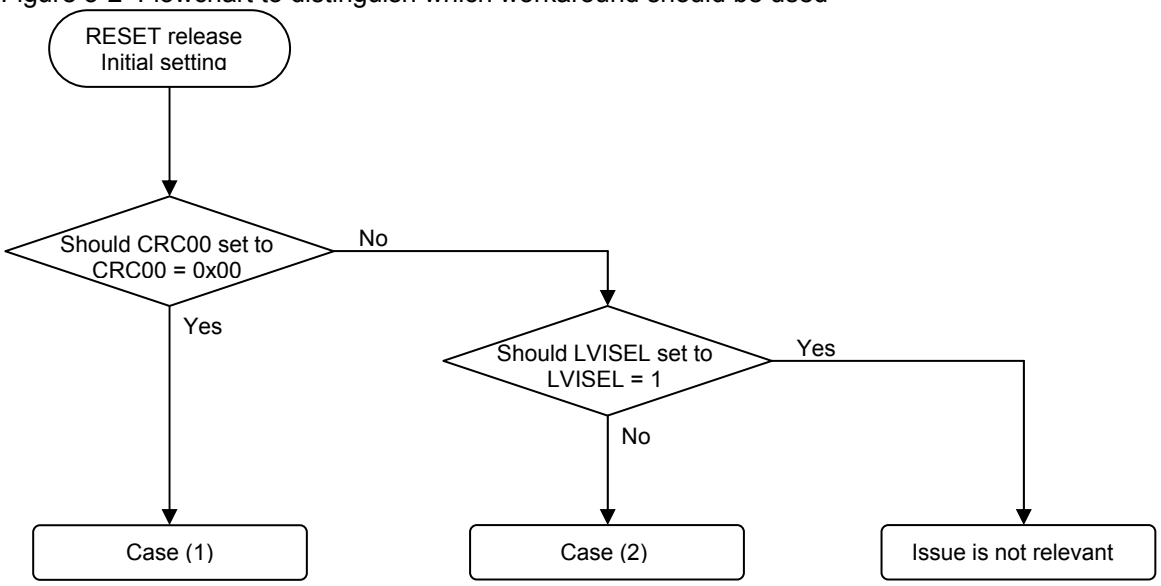
Figure 3-1 Example of Phenomenon



Workaround

As a workaround, at first distinguish the following cases:

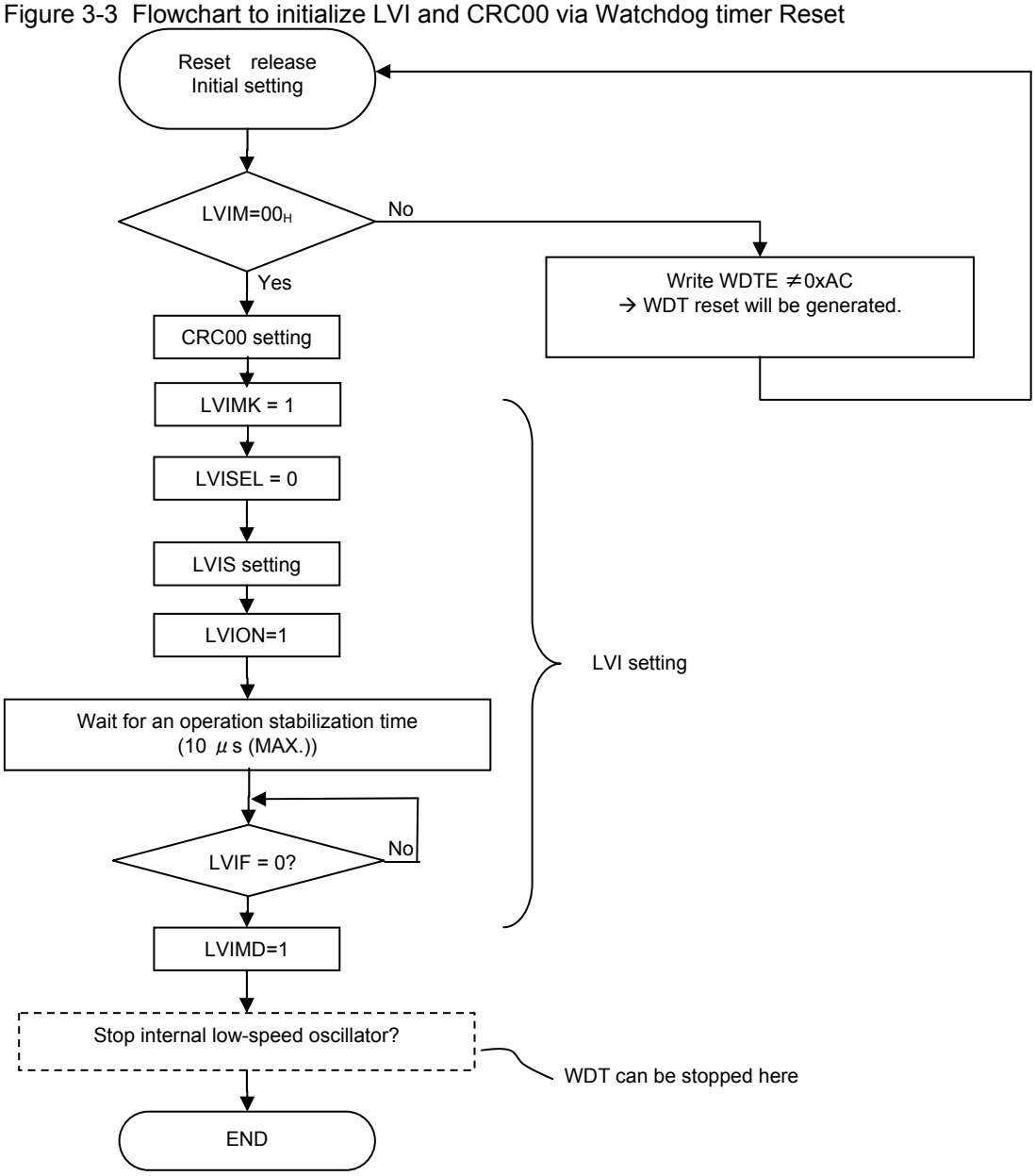
Figure 3-2 Flowchart to distinguish which workaround should be used



Case (1):
Method of configuring CRC00 = 00_H
After any Reset, the value of CRC00 becomes always 00_H, therefore it is not necessary to write to this register. The issue will be avoided because the competition with LVI reset will not occur when not writing to CRC00

Case (2):
Method of configuring CRC00 ≠ 00_H
In case LVIM ≠ 00_H after a Reset release, please initialize the LVI registers and CRC00 register again after the occurrence of another Reset generated by the Watchdog Timer.
The correct sequence for the LVI and CRC00 initialization is described in Figure 3-3.

Figure 3-3 Flowchart to initialize LVI and CRC00 via Watchdog timer Reset



To enable the Watchdog timer operation, please set the WDTON - bit in the option byte (address 0080h) to “1”.
In case, the internal Watchdog timer should not be used in the user application, please clear the LSROSC - bit in the option byte (address 0080h) to “0” and stop the Low-speed oscillator by software (LSRSTOP = 1)

(D) Valid Specification

Item	Date published	Document No.	Document Title
1	July 2007	U17328EJ5V0UD00 or later	User's Manual 78K0/KB2
2	February 2007	U17336EJ5V0UD00 or later	User's Manual 78K0/KC2
3	November 2007	U17312EJ5V0UD00 or later	User's Manual 78K0/KD2
4	October 2007	U17260EJ6VUD00 or later	User's Manual 78K0/KE2
5	October 2007	U17397EJ5V0UD00 or later	User's Manual 78K0/KF2

(E) Revision History

Item	Date published	Document No.	Comment
1	July 23, 2008	U18716EE1V0IF00	1st Release