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78K0/Kx1 Microcontrollers Technical Update	Document No.	ZBG-CC-06-0054	1/2
	Date issued	December 5, 2006	
	Issued by	1st Solution Group Multipurpose Microcomputer Systems Division 4th Systems Operations Unit NEC Electronics Corporation	
Related documents 78K0/KB1 User's Manual: U15836EJ5V0UD00 78K0/KC1 User's Manual: U16227EJ3V0UD00 78K0/KD1 User's Manual: U16315EJ3V1UD00 78K0/KE1 User's Manual: U16228EJ3V1UD00 78K0/KF1 User's Manual: U15947EJ3V1UD00	Notification classification	√	Usage condition
			Upgrade
			Document modification
			Other notification

1. Affected products

78K0/KB1: μPD780101, μPD780102, μPD780103, μPD78F0103

78K0/KC1: μPD780111, μPD780112, μPD780113, μPD780114, μPD78F0114

78K0/KD1: μPD780121, μPD780122, μPD780123, μPD780124, μPD78F0124

78K0/KE1: μPD780131, μPD780132, μPD780133, μPD780134, μPD780136, μPD780138, μPD78F0134, μPD78F0138

78K0/KF1: μPD780143, μPD780144, μPD780146, μPD780148, μPD78F0148Mx (x = 1 to 6)

2. Notification

The following item has been added. See attachment 11 for details.

When a reset input by the low-voltage detector (LVI) conflicts with write to the low-voltage detection register (LVIM) or low-voltage detection level selection register (LVIS), the write-enabled bits of the register may be set to 1.

3. Workaround

Do not write to the LVIM and LVIS registers after the LVI is set as a reset source. Make sure that bit 7 (LVION) of LVIM is 0 before writing to the LVIM or LVIS register. When setting both, set LVIS first. If LVION is 1, do not set LVIM and LVIS.

4. Modification schedule

Please regard this item as a caution on use.

5. Content listing

See attachment 1.

6. Revision history

78K0/KB1 Technical Update

Document Number	Date Issued	Description
SBG-DT-03-0002-E	January 14, 2003	Newly created.
SBG-DT-03-0159-E	May 28, 2003	Addition of restriction (No. 7)
SBG-DT-04-0024	January 24, 2004	Integration as 78K0/Kx1, addition of restriction (No. 8)
ZBG-CC-04-0016	October 4, 2004	Addition of restriction (No. 9)
ZBG-CC-04-0025	October 26, 2004	Change of document number
ZBG-CC-06-0054	December 5, 2006	Addition of usage condition (No. 10)

78K0/KC1 Technical Update

Document Number	Date Issued	Description
SBG-DT-03-0003-E	January 14, 2003	Newly created.
SBG-DT-03-0160-E	May 28, 2003	Addition of restriction (No. 7)
SBG-DT-04-0024	January 24, 2004	Integration as 78K0/Kx1, addition of restriction (No. 8)
ZBG-CC-04-0016	October 4, 2004	Addition of restriction (No. 9)
ZBG-CC-04-0025	October 26, 2004	Change of document number
ZBG-CC-06-0054	December 5, 2006	Addition of usage condition (No. 10)

78K0/KD1 Technical Update

Document Number	Date Issued	Description
SBG-DT-03-0004-E	January 14, 2003	Newly created.
SBG-DT-03-0161-E	May 28, 2003	Addition of restriction (No. 7)
SBG-DT-04-0024	January 24, 2004	Integration as 78K0/Kx1, addition of restriction (No. 8)
ZBG-CC-04-0016	October 4, 2004	Addition of restriction (No. 9)
ZBG-CC-04-0025	October 26, 2004	Change of document number
ZBG-CC-06-0054	December 5, 2006	Addition of usage condition (No. 10)

78K0/KE1 Technical Update

Document Number	Date Issued	Description
SBG-DT-03-0005-E	January 14, 2003	Newly created.
SBG-DT-03-0162-E	May 28, 2003	Addition of restriction (No. 7)
SBG-DT-04-0024	January 19, 2004	Integration as 78K0/Kx1, addition of restriction (No. 8)
ZBG-CC-04-0016	October 4, 2004	Addition of restriction (No. 9)
ZBG-CC-04-0025	October 26, 2004	Change of document number
ZBG-CC-06-0054	December 5, 2006	Addition of usage condition (No. 10)

78K0/KF1 Technical Update

Document Number	Date Issued	Description
SBG-DT-03-0006-E	January 14, 2003	Newly created.
SBG-DT-03-0163-E	May 28, 2003	Addition of restriction (No. 7)
SBG-DT-04-0024	January 24, 2004	Integration as 78K0/Kx1, addition of restriction (No. 8)
ZBG-CC-04-0016	October 4, 2004	Addition of restriction (No. 9)
ZBG-CC-04-0025	October 26, 2004	Change of document number
ZBG-CC-06-0054	December 5, 2006	Addition of usage condition (No. 10)

Usage Condition Updates in 78K0/Kx1 Microcontrollers

1. Product Version

- μPD780101, μPD780102, μPD780103: Rank K, E
- μPD780111, μPD780112, μPD780113, μPD780114: Rank K, E
- μPD780121, μPD780122, μPD780123, μPD780124: Rank K, E
- μPD780131, μPD780132, μPD780133, μPD780134, μPD780136, μPD780138: Rank K, E
- μPD780143, μPD780144, μPD780146, μPD780148: Rank K, E
- μPD78F0103: Rank I, K
- μPD78F0114: Rank K, E
- μPD78F0124: Rank K, E
- μPD78F0134: Rank K, E
- μPD78F0138: Rank K, E
- μPD78F0148: Rank I, K, E
- (A)- and (A1)-grade products of above products

* The rank is indicated by the letter appearing as the 5th digit from the left in the lot number marked on each product.

2. Product History

Mask ROM version:

	Description	78K0/KB1: μPD780101 μPD780102 μPD780103	78K0/KC1: μPD780111 μPD780112 μPD780113 μPD780114		78K0/KD1: μPD780121 μPD780122 μPD780123 μPD780124		78K0/KE1: μPD780131 μPD780132 μPD780133 μPD780134 μPD780136 μPD780138		78K0/KF1: μPD780143 μPD780144 μPD780146 μPD780148	
	Rank	K	K	E	K	E	K	E	K	E
	Version	–	–	–	–	–	–	–	–	–
1	Restriction on writing to flash memory	–	–	–	–	–	–	–	–	–
2	Restriction on detection voltage in POC and LVI	–	–	–	–	–	–	–	–	–
3	Restriction on POC	–	–	–	–	–	–	–	–	–
4	Restriction on clock monitor	–	–	–	–	–	–	–	–	–
5	Restriction on automatic transfer 3-wire CSI	–	–	–	–	–	–	–	–	–
6	Restriction on SBF transmission using UART6	△	△	△	△	△	△	△	△	△
7	Restriction on 16-bit timer output	△	△	△	△	△	△	△	△	△
8	Restriction on connection when XT1 is not used	–	×Note 3	○	×	○	×	○	×	○
9	Restriction on oscillation stabilization time	△	△	△	△	△	△	△	△	△
10	Low-voltage detector (LVI) function	△	△	△	△	△	△	△	△	△

Flash memory version:

	Description	78K0/KB1: μPD78F0103				78K0/KC1: μPD78F0114		78K0/KD1: μPD78F0124		78K0/KE1: μPD78F0134 μPD78F0138		78K0/KF1: μPD78F0148				
	Rank[Note 1]	I			K	K	E	K	E	K	E	I			K	E
	Version	1.0	1.1-2.1	2.2	–	–	–	–	–	–	–	1.1	2.0	2.1	–	–
1	Restriction on writing to flash memory	×	○	○	○	–	–	–	–	–	–	–	–	–	–	–
2	Restriction on detection voltage in POC and LVI	×	○	○	○	–	–	–	–	–	–	–	–	–	–	–
3	Restriction on POC	×	○	○	○	–	–	–	–	–	–	–	–	–	–	–
4	Restriction on clock monitor	×	×	○	○	–	–	–	–	–	–	–	–	–	–	–
5	Restriction on automatic transfer 3-wire CSI	–	–	–	–	–	–	–	–	–	–	×	×	○	○	○
6	Restriction on SBF transmission using UART6	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△
7	Restriction on 16-bit timer output	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△
8	Restriction on connection when XT1 is not used	–	–	–	–	× [Note 3]	○	○	○	×	○	×	×	×	×	○
9	Restriction on oscillation stabilization time	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△
10	Low-voltage detector (LVI) function	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△

Notes 1. The rank is indicated by the fifth character from the left in the lot number marked on the package.

2. The meaning of each symbol is as follows.

–: No relevant

○: Restriction already corrected

×: Restriction applies (correction is planned)

△: Restriction applies (correction is not planned)

3. Item 8 does not apply to the 78K0/KC1, but the device will be modified. See attachment 9 for details.

2. Update Details

Item 1: See Attachment 2.

Item 2: See Attachment 3.

Item 3: See Attachment 4.

Item 4: See Attachment 5.

Item 5: See Attachment 6.

Item 6: See Attachment 7.

Item 7: See Attachment 8.

Item 8: See attachment 9.

Item 9: See attachment 10.

Item 10: Item added in this edition (see attachment 11).

No. 1 Restriction on writing to flash memory

UART6 cannot be used in flash memory writing communication mode.

[Affected products]

μPD78F0103Mx (x = 1 to 6) Ver. 1.0

[Description]

Writing to the flash memory cannot be performed when UART6 is used in flash memory writing communication mode. Do not use UART6 for flash memory writing; the use 3-wire serial I/O or UART0 instead.

No. 2 Restriction on detection voltage in POC and LVI

The voltage detected by the power-on-clear circuit (POC) and low-voltage detector (LVI) is 0.1 to 0.3 V (TYP.) lower than that of the specification.

[Affected products]

μPD78F0103Mx (x = 1 to 6) Ver. 1.0

[Description]

The voltage detected by the power-on-clear circuit (POC) and low-voltage detector (LVI) is 0.1 to 0.3 V (TYP.) lower than that of the specification.

No. 3 Restriction on POC

Reset using POC may not be possible immediately after power application.

[Affected products]

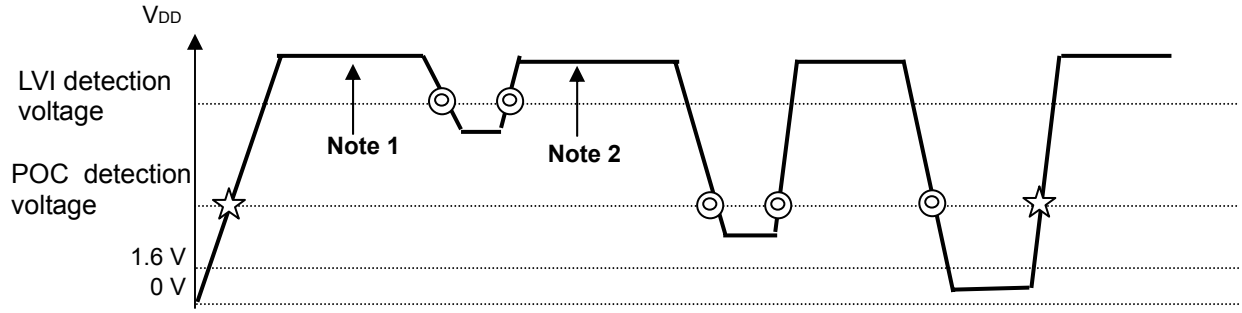
μPD78F0103Mx (x = 1 to 6) Ver. 1.0

[Description]

A reset using POC may not be possible immediately after power application. Therefore, an external reset should be used immediately after power application

A reset using POC at the fall of the power supply and when the voltage is raised from the POC detection voltage > V_{DD} > 1.6 V can be generated normally.

In addition, a reset is also generated normally at the rise/fall of the power supply when using LVI with a voltage higher than the POC detection voltage.



☆: RESET cannot be applied normally. Apply an external RESET.

◎: RESET can be applied normally.

Note 1: LVI is set to RESET by software (LVIMD ← 1)

Note 2: LVI operation stopped or is set to interrupt by software (LVION ← 0 or LVIMD ← 0)

No. 4 Restriction on clock monitor

The operation status of CLM (clock monitor mode register) can be manipulated even after the clock monitor operation is set.

[Affected products]

μPD78F0103Mx (x = 1 to 6) Ver. 1.0
μPD78F0103Mx (x = 1 to 6) Ver. 1.1
μPD78F0103Mx (x = 1 to 6) Ver. 2.0
μPD78F0103Mx (x = 1 to 6) Ver. 2.1

[Description]

Once bit 0 of CLM (clock monitor mode register) is set (1), the clock monitor cannot be cleared using a method other than RESET input or internal reset signal. However, operation of the clock monitor can actually be set by manipulating CLM by a software instruction.

Do not clear bit 0 of the CLM register once it is set (1); otherwise the clock monitor stops.

Bit 0 of CLM Register	Clock Monitor Operation
0	Stops
1	Operates

No. 5 Restriction on transmit data write using 3-wire serial interface with automatic transfer function

[Affected products]

μPD78F0148Mx (x = 1 to 6) Ver. 1.1

μPD78F0148Mx (x = 1 to 6) Ver. 2.0

[Description]

When writing transmit data to the buffer RAM using the 3-wire serial interface with automatic transfer function (CSIA0), data may not be written correctly depending on the instruction executed after the write instruction.

This restriction is not applicable under the following condition.

Condition: CSIA0 input clock (f_{SCKA}) is faster than the CPU operating clock (fcpu) $\times$ 10

$$fcpu \times 10 < f_{SCKA}$$

f_{SCKA}: CSIA0 input clock = fx

This condition is applicable only when fx is selected as the CSIA0 operating clock, and $fx/2^4$ or fxt is selected as the CPU operating clock (when the main clock is oscillating) in the 78K0/KF1.

[Workaround]

Temporary workarounds:

Implement any of the workarounds shown below by software.

Workaround (1): When interrupts are not disabled when writing to the buffer RAM

Write data to the buffer RAM using the 16-bit data transfer instruction only, and then read back the data to compare with the written value. If the data do not match, write the same value again. At this time, it is not necessary to disable interrupts.

When writing an odd number of bytes (if it is needed to write data to the even address), write dummy data to the buffer RAM at the higher address of the last address.

```
Example:  BRAMW1:   MOVW   AX,#0AA55H
                    MOVW   !0FA00H,AX        ; Buffer RAM write instruction
                    MOVW   AX,!0FA00H
                    CMPW   AX,#0AA55H        ; Comparison with expected data
                    BF     PSW.6,$BRAMW1
          ;
          BRAMW2:   MOVW   AX,#5A69H
                    MOVW   !0FA02H,AX        ; Buffer RAM write instruction
                      :
```

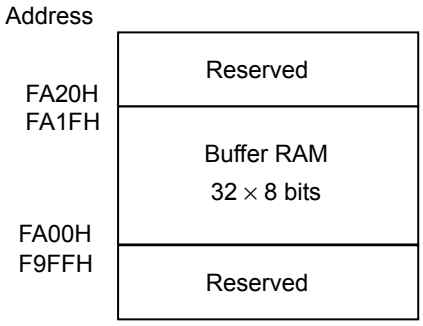


Figure: Buffer RAM Configuration

Workaround (2): When interrupts are disabled when writing to the buffer RAM (using the 16-bit data transfer instruction)

Disable interrupts using the DI instruction and write data to the buffer RAM using the 16-bit data transfer instruction only. In addition, re-write the last 2 bytes of the written data again. Do not execute instructions other than NOP and operation instructions between when data is written to the buffer RAM and when the last 2 bytes are rewritten.

```
Example:    DI                      ; Disables interrupt
            MOVW    AX,#0AA55H
            MOVW    !0FA00H,AX      ; Buffer RAM write instruction
            MOVW    AX,#5A69H
            MOVW    !0FA02H,AX      ; Buffer RAM write instruction
                    :
            MOVW    AX,#1234H
            MOVW    !0FA1EH,AX      ; Buffer RAM write instruction (last address)
            MOVW    !0FA1EH,AX      ; Re-write
            EI                      ; Enables interrupt
```

Workaround (3): When interrupts are disabled when writing to the buffer RAM (using the 8-bit data transfer instruction)

Disable interrupts using the DI instruction and write data to the buffer RAM using the 8-bit data transfer instruction only. In addition, execute a NOP or operation instruction after the last data is written to the buffer RAM.

```
Example:    DI                      ; Disables interrupt
            MOV   A,#0AAH
            MOV   !0FA00H,A         ; Buffer RAM write instruction
            MOV   A,#055H
            MOV   !0FA01H,A         ; Buffer RAM write instruction
                    :
            MOV   A,#12H
            MOV   !0FA1FH,A         ; Buffer RAM write instruction (last address)
            NOP
            EI          ; Enables interrupt
```

No. 6 Restriction on SBF transmission using UART6

[Affected products]

All 78K0/Kx1 microcontrollers

[Description]

If SyncBreakField transmission is performed when LIN operates as the master in UART6 supporting the LIN-bus, the following illegal operation may be performed.

(1) A SyncBreakField field length shorter than the set value is output.

(2) Illegal UART transmission may be performed before SyncBreakField transmission is performed

There is no problem when LIN operates as a slave with which SyncBreakField transmission is not performed and when UART6 is used as a UART function.

[Workaround]

Implement the following workaround by software.

Perform 13- to 20-bit low-level SyncBreakField transmission by adjusting the baud rate value of the normal UART transmit function.

Do not use the SyncBreakField transmission function. Specifically, do not set bit 5 (SBTT6) of asynchronous serial interface control register 6 (ASICL6) to 1.

<How to set>

Set the UART data length to 8 bits, parity to 0 parity or even parity and transmit 00H.

As a result, 10-bit low-level transmission (start bit (1 bit) + data (8 bits) + parity (1 bit)) can be performed. Adjust the baud rate value so that this 10-bit low level matches the target SyncBreakField length.

Example: When conditions of the transmitted LIN are:

UART6 basic clock = 5 MHz ←This value is set by clock select register 6 (CKSR6)

Target baud rate value = 19,200 [bps]

The value set to the baud rate generator control register (BRGC6) to implement the above baud rate value is 130. Therefore, the 13-bit SyncBreakField length is: 0.2 μs $\times$ 130 $\times$ 2 $\times$ 13 = **676 μs**

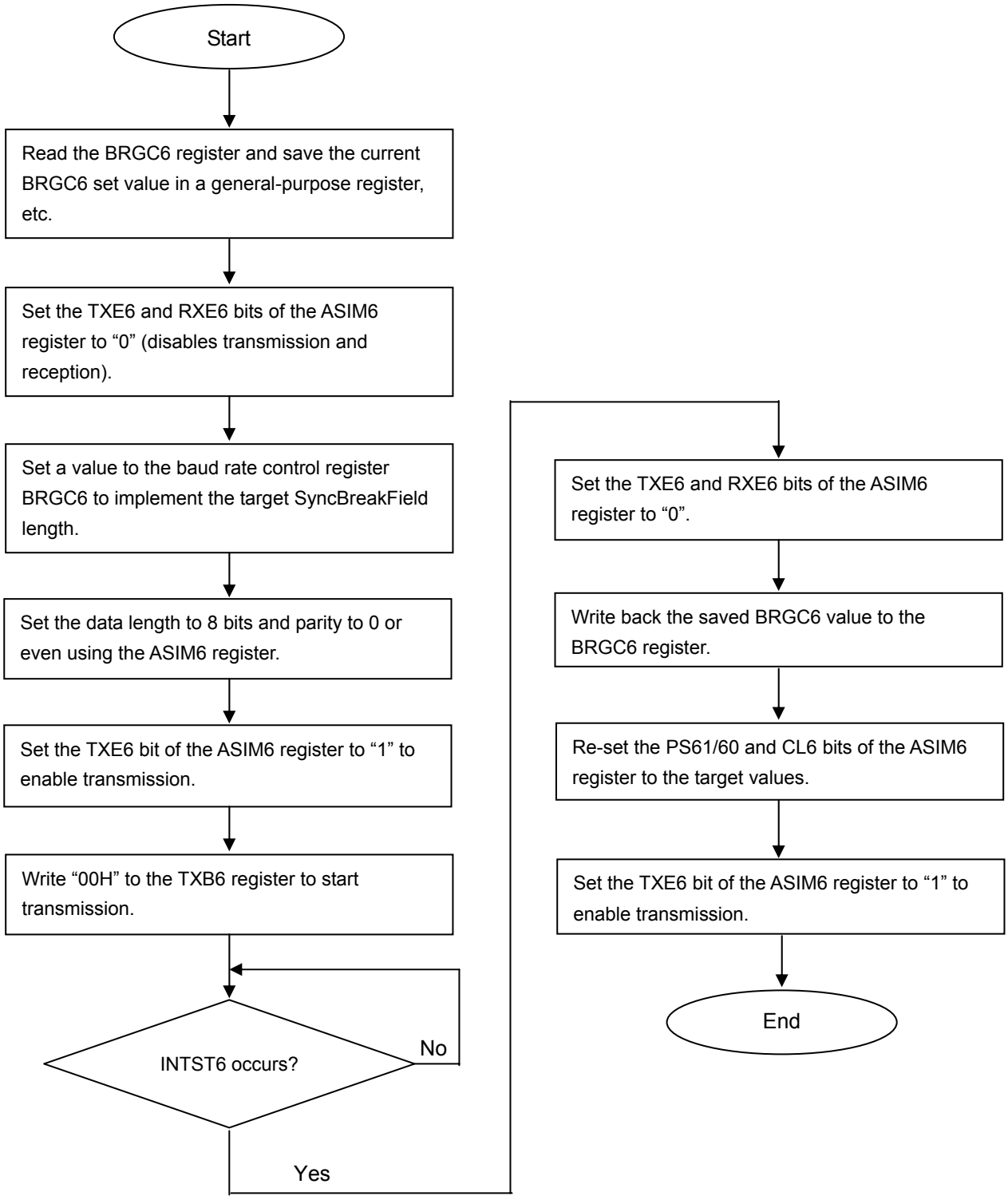
To implement this 13-bit field length in 10 bits, set a value 1.3 times the target baud rate to BRGC6. In this example, set BRGC6 to 169. The 10-bit low-level transmission length is: 0.2 μs $\times$ 169 $\times$ 2 $\times$ 10 = **676 μs**

Consequently, the value matches that of the 13-bit SyncBreakField length.

If the setting to the BRGC6 register is not sufficient for setting the bit, also select the UART6 basic clock.

The following shows the flowchart of the software setting procedure.

<Flowchart of software setting procedure>



[Modification]

Regard this item as a usage restriction. The user's manual and device file will be corrected.

<Details of correction in user's manual and device file>

Description of bits 2 to 5 related to the SyncBreakField transmit function of asynchronous serial interface control register 6 (ASICL6) will be deleted from the chapter of UART6 in the user's manual. In addition, these bits are fixed to the initial values and writing to these bits is disabled.

The correction will be reflected in the device file.

[Before modification]

Address: FF58H After reset: 16H R/W

Note Bit 7 is read-only.

Symbol	<7>	6	5	4	3	2	1	0
ASICL6	SBRF6	SBRT6	SBTT6	SBL62	SBL61	SBL60	DIR6	TXDLV6

[After modification]

Address: FF58H After reset: 16H R/W**Note**

Note Bits 2 to 5 and 7 are read-only.

Symbol	<7>	<6>	5	4	3	2	1	0
ASICL6	SBRF6	SBRT6	0	1	0	1	DIR6	TXDLV6

In line with this correction, SBRT6 will be added to the assembler reserved words, and to the header file (sfrbit.h) in the C compiler.

No. 7 Restriction on 16-bit timer output

[Affected products]

All 78K0/Kx1 microcontrollers

[Description]

When setting the timer output F/F status using 16-bit timer/event counter 00 or 01, the setting may not be performed correctly depending on the TOC0n (timer output control register) setting timing.

If LVS0n is set to 1 before setting TOE0n, the LVS0n settings are invalid and a low level is output. If LVS0n and TOE0n are set to 1 simultaneously, the timer output is undefined.

<16-bit timer output control register format>

Symbol	7	<6>	<5>	4	<3>	<2>	1	<0>
TOC0n	0	OSPT0n	OSPE0n	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n

LVS0n	LVR0n	Setting of timer output F/F
0	0	No change
0	1	Timer output F/F is reset (0)
1	0	Timer output F/F is set (1)
1	1	Setting prohibited

TOE0n	Timer output control
0	Output disabled
1	Output enabled

[Workaround]

When setting LVS0n to 1 to output a high level from the timer, be sure to set TOE0n to 1 first to enable timer output, and then set LVS0n to 1. The following shows a program example.

<Program example>

```
                :
MOV     TOC00,#00000001B        ; 16-bit timer output enabled
MOV     TOC00,#00011011B        ; Other settings and timer output F/F are set to high level
                                  (Timer output level is set to high.)
                :
MOV     TMC00,#00001100B        ; Timer operation started
```

Remark n = 0 or 1

No. 8 Restriction on connection when XT1 is not used

[Affected products]

78K0/KD1, 78K0/KE1, and 78K0/KF1 products of rank I or K

[Description]

When the unused XT1 pin is connected under the following condition, the operating current increases by approx. 5 mA.

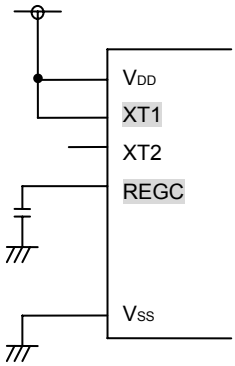
Condition: The regulator is used (the REGC pin is connected to V_{SS} vis a 1 μF capacitor) and the XT1 pin is connected to V_{DD}.

This restriction does not apply if the regulator is not used (the REGC pin is connected to V_{DD}) or if the XT1 and XT2 pins are connected to the subclock.

Table 1. Relationship Between connection of XT1 and REGC Pins and Restriction

	Regulator Is Not Used (REGC Pin Is Connected to V_{DD})	Regulator Is Used (REGC Pin Is Connected to V_{SS} via 1 μF Capacitor)
Subclock is used (A 32.768 kHz resonator is connected to XT1, XT2)	Not affected by restriction.	Not affected by restriction.
Subclock is not used (XT1 is connected to V_{DD} and XT2 is left open)	Not affected by restriction.	The operating current increases by approx. 5 mA.

Figure 1. Connection of REGC and XT1 Pins That Increases Operating Current



[Action]

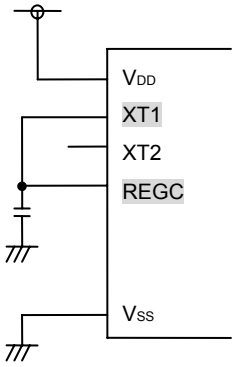
<Temporary workaround>

When the regulator is used and the XT1 pin is not used, implement any of the following temporary workarounds.

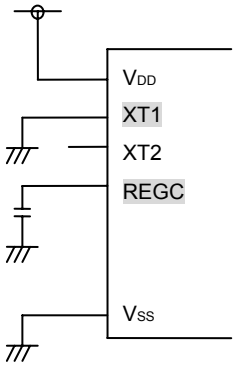
- Connect the XT1 pin to the REGC pin directly.
- Connect the XT1 pin to V_{SS}. With this workaround, however, the operating current increases by several μA.

Figure 2. Circuit Diagram When Temporary Workaround Is Implemented

(1) XT1 pin is connected to REGC pin



(2) XT1 pin is connected to VSS

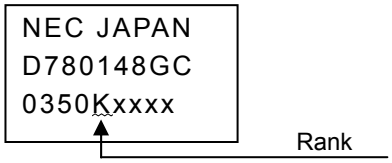


<Permanent workaround>

Connect the XT1 pin to GND when it is not used. In addition, the device will be modified to suppress the several μA current increase.

Cautions on device modification

1. Users are not required to change software in line with this device modification.
2. The electrical specifications will not be affected by this device modification.
3. Users can use the modified device without modifying circuits or software if the regulator is not used or the subclock is connected.
4. This restriction does not apply to the 78K0/KC1, but the device will be modified so that the **XT1 pin can be connected to Vss.**
5. The device name will be changed after modification.
6. After this modification, the rank of the product will be E (products not modified are rank K or I). The rank is indicated by the fifth character from the left in the lot number marked on the third line on the package (see the figure below).



The relationship between the connection of the XT1 pin when it is not used, the temporary workaround, and the permanent workaround is shown in Table 2.

Table 2. Relationship Between Connection of XT1 Pin When It Is Not Used, Temporary Workaround, and Permanent Workaround

Connection of XT1 Pin When It Is Not Used		KD1, KE1, KF1 Before Modification	KD1, KE1, KF1 After Modification	78K0/Kx1+[Note]
Current connection	Connect XT1 pin to V_{DD} (when regulator is not used, REGC pin is connected to V_{DD})	Not affected by restriction.	Not affected by restriction.	Not affected by restriction.
	Connect XT1 pin to V_{DD} (when regulator is used, a 1 μF capacitor is connected to REGC pin)	The operating current increases by approx. 5 mA.	The operating current increases by approx. 5 mA.	Not affected by restriction.
Temporary workaround	Connect XT1 pin to REGC pin (when regulator is used, a 1 μF capacitor is connected to REGC pin)	Not affected by restriction.	Not affected by restriction.	Leave the REGC pin open; otherwise a through current may flow in the XT1 and XT2 pins.
Permanent workaround	Connect XT1 pin to V_{SS} (when regulator is not used, REGC pin is connected to V_{DD})	The operating current increases by several μA.	Not affected by restriction.	Not affected by restriction.
	Connect XT1 pin to V_{SS} (when regulator is used, a 1 μF capacitor is connected to REGC pin)	The operating current increases by several μA.	Not affected by restriction.	Not affected by restriction.

Note The 78K0/Kx1+ is a 78K0/Kx1-compatible microcontroller currently under development.

[Device modification schedule]

Flash memory version: Modification of products will be complete by the shipment of June 2004.

Mask ROM version: Modification of products will be complete for tape-out products by the shipment of May 2004.

The modified devices will be released as they become ready. Separately contact an NEC Electronics sales representative for the detailed schedule.

No. 9 Restriction on oscillation stabilization time

[Affected products]

All 78K0/Kx1 microcontrollers

[Description]

When the OSTS register (oscillation stabilization time select register) is used with a specific setting other than the initial value and the main clock oscillation stabilization time is checked using the OSTC register (oscillation stabilization time counter status register), the correct value may not be read.

<Condition>

OSTC Operating Status	OSTS Value Setting	OSTS Value Change Pattern (OSTS Initial Value = 05H)	Whether or Not This Restriction Is Applicable
Count status after reset or standby release	OSTS value is not set (Initial value is used)	–	Not applicable
	OSTS value is set	05H (101) → 05H (101)	Not applicable
		05H (101) → 04H (100)	Not applicable
		05H (101) → 03H (011)	Applicable
		05H (101) → 02H (010)	Applicable
		05H (101) → 01H (001)	Not applicable
		Consult NEC Electronics in regards to change patterns other than above.	–
Other than above	–	–	Not applicable

[Workaround]

Do not use the OSTS register under the condition to which this restriction applies.

When using the OSTS register under the condition to which this restriction applies, check the oscillation stabilization time using the OSTC register before setting the OSTS register.

No. 10 Low-voltage detector (LVI) function

[Affected products]

All 78K0/Kx1 microcontrollers

[Affected usage]

When the low-voltage detector (LVI) is used as a reset source

(This item does not affect operations when the LVI is not used, or when it is used as an interrupt source.)

[Description]

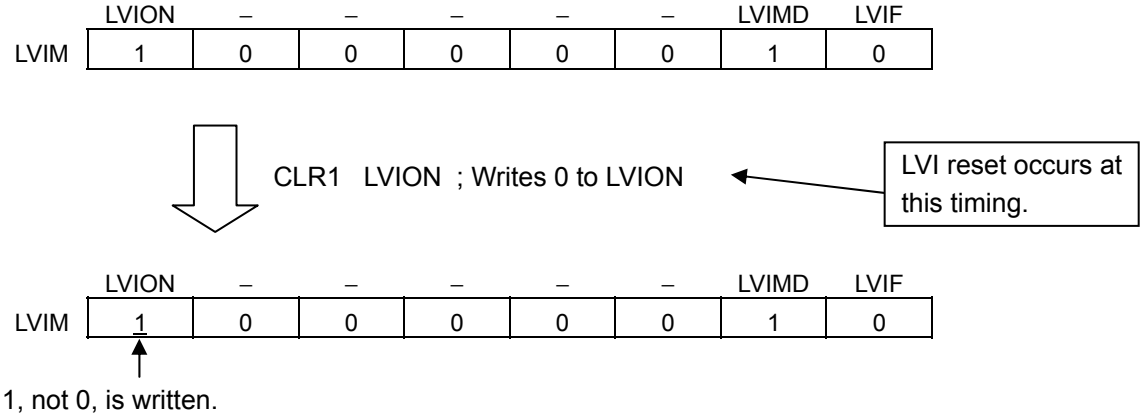
When a reset input by the low-voltage detector (LVI) conflicts with write to a register that sets the LVI operation (LVIM or LVIS), the write-enabled bits of the register may be set to 1. As a result, the following two phenomena occur.

- The reset by the LVI may not stop.
- The voltage detected by the LVI may be lower than the set value or the default value.

These phenomena do not occur in cases other than the LVI reset.

Figure 1 shows an example when these phenomena occur due to manipulation of the LVION flag.

Figure 1 When LVION Flag Value Is Changed from 1 to 0



In the case of LVIS, the default value (4.3 V ±0.2 V) is detected if bit 3 is set to 1.

[Cause]

The bus connected to LVIM and LVIS becomes High (“1”) after reset. In addition, the values of these registers are not cleared by an LVI reset, according to the specifications.

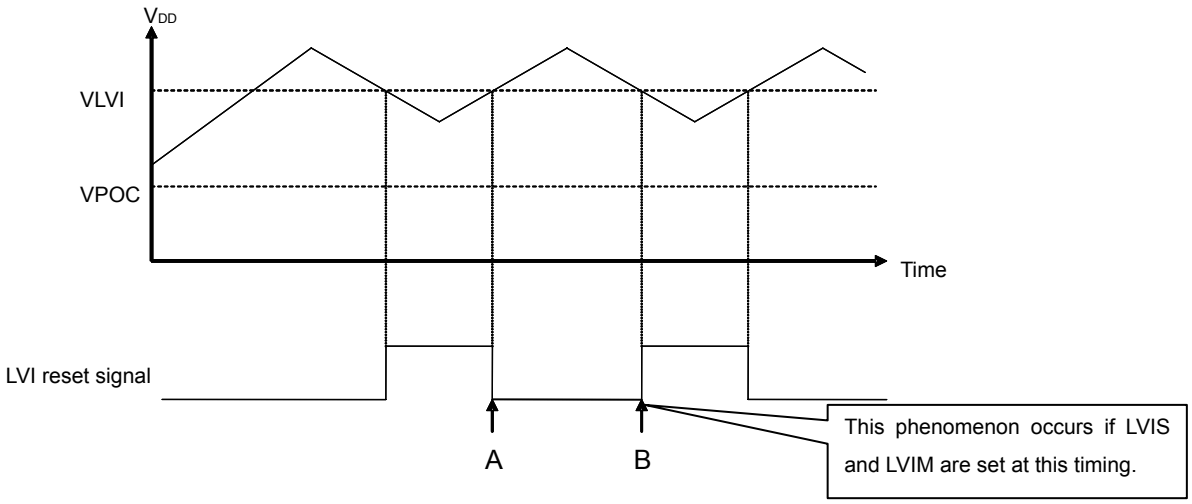
When a value is written to these registers, the CPU first sets the write value to the bus. This value is written to the target register when a write signal occurs. If the register is written when the internal bus is reset by an LVI reset, however, the reset value of the bus (1) may be written. This also applies to 1-bit manipulation instructions.

Registers other than LVIM and LVIS are not affected by this case.

[Occurrence Example]

If the VDD voltage varies around the LVI detection voltage (VLVI), the LVI reset occurs several times. In programs in which LVIM and LVIS are always initialized after reset release, if the period from LVI reset release (A in Figure 2) until a LVI reset occurrence (B in Figure 2) matches the time from reset release until initial setting of LVIM and LVIS, this phenomenon occurs.

Figure 2 Example of Conflict Between LVI Reset and LVIM Register Write



[Workarounds]

Implement the following two software measures.

(1) Do not write to the LVIM and LVIS registers after the LVI is set as a reset source.

(2) Make sure that bit 7 (LVION) of LVIM is 0 before setting the LVIM or LVIS register. If LVION is 1, do not set LVIM and LVIS. By taking this measure, setting of LVIM and LVIS will be performed upon external reset input, POC reset, watchdog timer (WDT) reset or clock monitor (CLM) reset, but will not be performed upon LVI reset.

Because the reset control flag register (RESF) is not cleared by reset input from the LVI, WDT, or CLM according to the specifications, LVIRF, WDTRF and CLMRF may be set to 1. Whether the LVI reset has been input can be judged by checking LVIRF, but an additional instruction is required to judge if LVIM or LVIS has been cleared by WDT or CLM reset. Therefore, use LVION for workarounds of this case.