

<p>78K0/KD1</p> <p>Document Modification</p>		Document No.	SBG-DT-03-0292-E	1/2
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Related documents	78K0/KD1 User's Manual: U16315EJ2V0UD00	Notification classification	<input type="checkbox"/>	Usage restriction
			<input type="checkbox"/>	Upgrade
			<input checked="" type="checkbox"/>	Document modification
			<input type="checkbox"/>	Other notification

1. Affected products

μPD780121, 780122, 780123, 780124

μPD78F0124Mx (x = 1 to 6)

2. Details of correction of erroneous description

(1) Erroneous descriptions have been found in **CHAPTER 5 CLOCK GENERATOR** as shown below.

AC Characteristics on page 419 defines the minimum instruction execution time only for 240 kHz (TYP.) operation when Ring-OSC is selected as the CPU clock, but **Figure 5-2 Format of Processor Clock Control Register (PCC)** on page 103 shows the ratings of the divided Ring-OSC clock frequency.

In the standard products and (A) grade products, the CPU can operate on a Ring-OSC clock divided by up to 2. Dividing the clock frequency in the (A1) grade products (A2) grade products is not possible.

See attachment 3 for details.

(2) Erroneous descriptions have been found in **CHAPTER 10 WATCHDOG TIMER** as shown below.

Caution 3 in **Figure 10-2 Format of Watchdog Timer Mode Register (WDTM)** on page 219 indicates, "After reset is released, WDTM can be written only once by an 8-bit memory manipulation instruction. If writing attempted a second time, an internal reset signal is generated." However, the internal reset signal is not generated while the watchdog timer operation is stopped.

Caution 1 in **Figure 10-3 Format of Watchdog Timer Enable Register (WDTE)** on page 219 indicates, "If a value other than ACH is written to WDTE, an internal reset signal is generated" and **Caution 2** indicates, "If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated." However, the internal reset signal is not generated while the watchdog timer operation is stopped.

See attachment 4 for details.

3. Action

Correction of the erroneous descriptions in this document will be reflected in the next revision of the user's manual.

4. List of erroneous description corrections

The history of erroneous description corrections and detailed information will be described on the following pages.

5. Revision history

78K0/KD1 Document Modification Revision History

Document Number	Date Issued	Description
SBG-DT-03-0004-E	January 14, 2003	Newly created.
SBG-DT-03-0161-E	May 28, 2003	Addition of restriction (No.2)
SBG-DT-03-0212-E	July 18, 2003	Addition of erroneous description correction (No.1)
SBG-DT-03-0292-E	November 14, 2003	Addition of erroneous description corrections (No.2 and No.3)

Correction History of Erroneous Descriptions in 78K0/KD1

1. Product History

No.	Description Edition (Document No.)	78K0/KD1 User's Manual	
		1st Edition (U16315EJ1V0)	2nd Edition (U16315EJ2V0)
1	Erroneous description on REGC pin connection capacitance	×	√
2	Erroneous description on Ring-OSC clock division	×	×
3	Erroneous description on watchdog timer	×	×

Note The meaning of each symbol is as follows.

- : Erroneous description exists
- √: Erroneous description already corrected
- ×: Erroneous description will be corrected

2. Details of Correction of Erroneous Description

Item 1: See attachment 2.

Item 2: The correction added this time (see attachment 3).

Item 3: The correction added this time (see attachment 4).

Erroneous description correction

No.1 Erroneous description on REGC pin connection capacitance

On page 382 in **CHAPTER 23 REGULATOR** in the 78K0/KD1 Preliminary User's Manual, the capacitance of the capacitor for regulator stabilization is described as 0.1 μF , but 1 μF is correct.

Incorrect) 0.1 μF

Correct) 1 μF

In addition, the operating voltage range and instruction cycle (minimum instruction execution time) when the capacitor for regulator stabilization is connected has been corrected as follows.

Incorrect)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock operation	X1 input clock, 0.1 μF is connected to REGC pin	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.238	16	μs
				$2.7\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	0.4	16	μs

Correct)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock operation	X1 input clock, 1 μF is connected to REGC pin	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.238	16	μs
					0.4	16	μs

Details of corrections

The shaded portions are the relevant corrections.

◆ Caution 4 on page 29

Incorrect)

When using the regulator, connect the REGC pin to V_{SS} via 0.1 μF capacitor.

Correct)

When using the regulator, connect the REGC pin to V_{SS} via 1 μF capacitor.

◆ X1 input clock item in table on page 34

Incorrect)

0.1 μF capacitor is connected to REGC pin

Correct)

1 μF capacitor is connected to REGC pin

◆ REGC in table on page 37

Incorrect)

Connect to V_{SS} via a 0.1 μF capacitor.

Correct)

Connect to V_{SS} via a 1 μF capacitor.

◆ 2.2.13 REGC on page 43

Incorrect)

Connect this pin to Vss via a 0.1 μF capacitor.

Correct)

Connect this pin to Vss via a 1 μF capacitor.

◆ 2nd line in **23.1 Outline** on page 382

Incorrect)

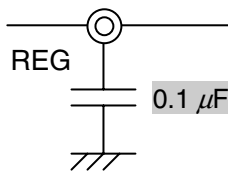
..., connect the REGC pin to Vss via a 0.1 μF capacitor.

Correct)

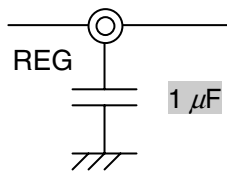
..., connect the REGC pin to Vss via a 1 μF capacitor.

◆ Capacitor capacitance in Figure 23-1 on page 382

Incorrect)



Correct)



◆ 2nd line of **Caution** on pages 388 and 389

Incorrect)

Connect to GND of Flashpro III/Flashpro IV via 0.1 μF capacitor.

Correct)

Connect to GND of Flashpro III/Flashpro IV via 1 μF capacitor.

◆ 2nd line of **Note** on pages 390 to 394

Incorrect)

Connect to GND via 0.1 μF capacitor.

Correct)

Connect to GND via 1 μF capacitor.

◆ X1 Oscillator Characteristics on page 410

Incorrect)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit	
Ceramic resonator		Oscillation frequency (f_{XP}) ^{Note 1}	When a capacitor is connected to the REGC pin ^{Note 2}	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.0		8.38	MHz
				$2.7\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	2.0		5.0	
			When the REGC pin is directly connected to V_{DD}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.0		10	MHz
				$3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	2.0		8.38	
Crystal resonator		Oscillation frequency (f_{XP}) ^{Note 1}	When a capacitor is connected to the REGC pin ^{Note 2}	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.0		8.38	MHz
				$2.7\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	2.0		5.0	
			When the REGC pin is directly connected to V_{DD}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.0		10	MHz
				$3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	2.0		8.38	

Correct)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit	
Ceramic resonator		Oscillation frequency (f_{XP}) ^{Note 1}	When a capacitor is connected to the REGC pin ^{Note 2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.0		8.38	MHz
					2.0		5.0	
			When the REGC pin is directly connected to V_{DD}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.0		10	MHz
				$3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	2.0		8.38	
Crystal resonator		Oscillation frequency (f_{XP}) ^{Note 1}	When a capacitor is connected to the REGC pin ^{Note 2}	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.0		8.38	MHz
				$2.7\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	2.0		5.0	
			When the REGC pin is directly connected to V_{DD}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.0		10	MHz
				$3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	2.0		8.38	

◆ Note 2 in X1 Oscillator Characteristics on page 410

Incorrect)

When the REGC pin is connected to V_{SS} via a $0.1\ \mu\text{F}$ capacitor.

Correct)

When the REGC pin is connected to V_{SS} via a $1\ \mu\text{F}$ capacitor.

◆ Note 8 in DC Characteristics (3/4): $\mu\text{PD78F0124}$ on page 414

Incorrect)

When the REGC pin is connected to V_{SS} via a $0.1\ \mu\text{F}$ capacitor.

Correct)

When the REGC pin is connected to V_{SS} via a $1\ \mu\text{F}$ capacitor.

◆ **Note 8 in DC Characteristics (4/4): Mask ROM version** on page 415

Incorrect)

When the REGC pin is connected to Vss via a 0.1 μF capacitor.

Correct)

When the REGC pin is connected to Vss via a 1 μF capacitor.

◆ **AC Characteristics (1) Basic operation** on page 416

Incorrect)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	T _{cy}	Main system clock operation	X1 input clock	Note 1	3.3 V ≤ V _{DD} ≤ 5.5 V	0.238		16	μs
					2.7 V ≤ V _{DD} ≤ 3.3 V	0.4		16	μs
				Note 2	4.0 V ≤ V _{DD} ≤ 5.5 V	0.2		16	μs
					3.3 V ≤ V _{DD} < 4.0 V	0.238		16	μs
					2.7 V ≤ V _{DD} < 3.3 V	0.4		16	μs
				Ring-OSC clock				4.17	8.33
		Subsystem clock operation				114	122	125	μs

Correct)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	T _{cy}	Main system clock operation	X1 input clock	Note 1	4.0 V ≤ V _{DD} ≤ 5.5 V	0.238		16	μs
						0.4		16	μs
				Note 2	4.0 V ≤ V _{DD} ≤ 5.5 V	0.2		16	μs
					3.3 V ≤ V _{DD} < 4.0 V	0.238		16	μs
					2.7 V ≤ V _{DD} < 3.3 V	0.4		16	μs
				Ring-OSC clock				4.17	8.33
		Subsystem clock operation				114	122	125	μs

◆ **Note 1 in AC Characteristics (1) Basic operation** on page 416

Incorrect)

When the REGC pin is connected to Vss via a 0.1 μF capacitor.

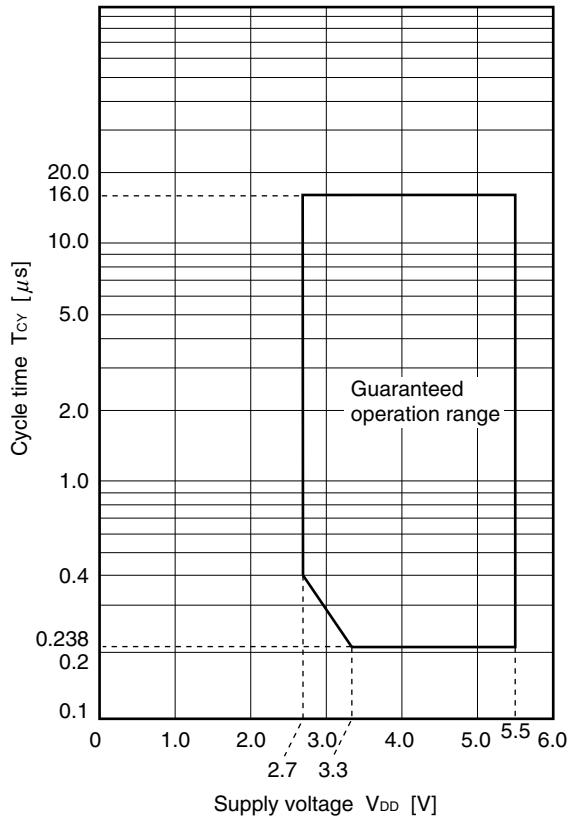
Correct)

When the REGC pin is connected to Vss via a 1 μF capacitor.

◆ **T_{CY} vs. V_{DD} (X1 Input Clock Operation)** on page 417

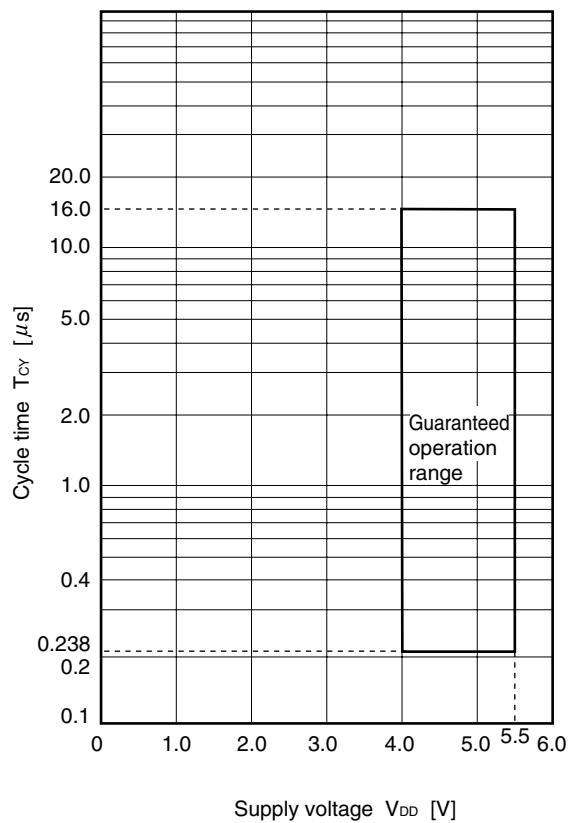
Incorrect)

(a) When REGC pin is connected to V_{SS} via 0.1 μF capacitor



Correct)

(a) When REGC pin is connected to V_{SS} via 1 μF capacitor



No.2 Erroneous description on Ring-OCS clock division

Erroneous descriptions have been found in **CHAPTER 5 CLOCK GENERATOR** as shown below.

AC Characteristics on page 419 defines the minimum instruction execution time only for 240 kHz (TYP.) operation when Ring-OSC is selected as the CPU clock, but **Figure 5-2 Format of Processor Clock Control Register (PCC)** on page 103 shows the ratings of the divided Ring-OSC clock frequency.

In the standard products and (A) grade products, the CPU can operate on a Ring-OSC clock divided by up to 2. Dividing the clock frequency in the (A1) grade products (A2) grade products is not possible.

[Details of correction]

- Modification of **Figure 5-2 Format of Processor Clock Control Register (PCC)** on page 103 (Incorrect)

CSS ^{Note 4}	PCC2	PCC1	PCC0	CPU clock (f _{CPU}) selection		
				MCM0 = 0	MCM0 = 1	
0	0	0	0	f _X	f _R	f _{XP}
	0	0	1	f _X /2	f _R /2	f _{XP} /2
	0	1	0	f _X /2 ²	f _R /2 ²	f _{XP} /2 ²
	0	1	1	f _X /2 ³	f _R /2 ³	f _{XP} /2 ³
	1	0	0	f _X /2 ⁴	f _R /2 ⁴	f _{XP} /2 ⁴
1	0	0	0	f _{XT} /2		
	0	0	1			

Correct)

CSS ^{Note 4}	PCC2	PCC1	PCC0	CPU clock (f _{CPU}) selection		
				MCM0 = 0	MCM0 = 1	
0	0	0	0	f _X	f _R	f _{XP}
	0	0	1	f _X /2	f _R /2 ^{Note 5}	f _{XP} /2
	0	1	0	f _X /2 ²	Setting prohibited	f _{XP} /2 ²
	0	1	1	f _X /2 ³	Setting prohibited	f _{XP} /2 ³
	1	0	0	f _X /2 ⁴	Setting prohibited	f _{XP} /2 ⁴
1	0	0	0	f _{XT} /2		
	0	0	1			

Note 5. Setting prohibited in the (A1) grade and (A2) grade products.

- Modification of **Table 5-2 Relationship Between CPU Clock and Minimum Instruction Execution Time** on page 104

Incorrect)

CPU Clock (f_{CPU})	Minimum Instruction Execution Time: $2/f_{CPU}$		
	X1 Input Clock ^{Note} (at 10 MHz Operation)	Ring-OSC Clock ^{Note} (at 240 kHz (TYP.) Operation)	Subsystem Clock (at 32.768 kHz Operation)
f_x	0.2 μs	8.3 μs (TYP.)	–
$f_x/2$	0.4 μs	16.6 μs (TYP.)	–
$f_x/2^2$	0.8 μs	33.2 μs (TYP.)	–
$f_x/2^3$	1.6 μs	66.4 μs (TYP.)	–
$f_x/2^4$	3.2 μs	132.8 μs (TYP.)	–
$f_{XT}/2$	–	–	122.1 μs

Note The main clock mode register (MCM) is used to set the CPU clock (X1 input clock/Ring-OSC clock) (see **Figure 5-4**).

Correct)

CPU Clock (f_{CPU})	Minimum Instruction Execution Time: $2/f_{CPU}$		
	X1 Input Clock ^{Note 1} (at 10 MHz Operation)	Ring-OSC Clock ^{Note 1} (at 240 kHz (TYP.) Operation)	Subsystem Clock (at 32.768 kHz Operation)
f_x	0.2 μs	8.3 μs (TYP.)	–
$f_x/2$	0.4 μs	16.6 μs (TYP.) ^{Note 2}	–
$f_x/2^2$	0.8 μs	–	–
$f_x/2^3$	1.6 μs	–	–
$f_x/2^4$	3.2 μs	–	–
$f_{XT}/2$	–	–	122.1 μs

Notes 1. The main clock mode register (MCM) is used to set the CPU clock (X1 input clock/Ring-OSC clock) (see **Figure 5-4**).

2. Setting prohibited in the (A1) grade and (A2) grade products.

- Modification of **AC Characteristics** on page 429

Incorrect)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock operation	X1 input clock	Note 1	4.0 V ≤ V _{DD} ≤ 5.5 V	0.238		16	μs
				Note 2	4.0 V ≤ V _{DD} ≤ 5.5 V	0.2		16	μs
					3.3 V ≤ V _{DD} < 4.0 V	0.238		16	μs
					2.7 V ≤ V _{DD} < 3.3 V	0.4		16	μs
		Ring-OSC clock		4.17	8.33	16.67	μs		
		Subsystem clock operation		114	122	125	μs		

Correct)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock operation	X1 input clock	Note 1	4.0 V ≤ V _{DD} ≤ 5.5 V	0.238		16	μs
				Note 2	4.0 V ≤ V _{DD} ≤ 5.5 V	0.2		16	μs
					3.3 V ≤ V _{DD} < 4.0 V	0.238		16	μs
					2.7 V ≤ V _{DD} < 3.3 V	0.4		16	μs
		Ring-OSC clock		4.17		33.33	μs		
		Subsystem clock operation		114	122	125	μs		

No.3 Erroneous description on watchdog timer

Erroneous descriptions have been found in **CHAPTER 10 WATCHDOG TIMER** as shown below.

Caution 3 in **Figure 10-2 Format of Watchdog Timer Mode Register (WDTM)** on page 219 indicates, “After reset is released, WDTM can be written only once by an 8-bit memory manipulation instruction. If writing attempted a second time, an internal reset signal is generated.” However, the internal reset signal is not generated while the watchdog timer operation is stopped.

Caution 1 in **Figure 10-3 Format of Watchdog Timer Enable Register (WDTE)** on page 219 indicates, “If a value other than ACH is written to WDTE, an internal reset signal is generated” and **Caution 2** indicates, “If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated.” However, the internal reset signal is not generated while the watchdog timer operation is stopped.

The relationship between the watchdog timer operation and the internal reset signal is shown below.

Internal Reset Signal Generation Cause	Ring-OSC Cannot Be Stopped	Ring-OSC Can Be Stopped by Software		
		Watchdog Timer Is Operating	Watchdog Timer Stopped	
			WDCS4 Is Set to 1	Source Clock to Watchdog Timer Is Stopped
Watchdog timer counter overflows	Internal reset signal is generated.	Internal reset signal is generated.	–	–
Write to WDTM for the second time	Internal reset signal is generated.	Internal reset signal is generated.	Internal reset signal is not generated and the watchdog timer does not resume operation.	Internal reset signal is generated when the source clock to the watchdog timer resumes operation.
Write other than “ACH” to WDTE	Internal reset signal is generated.	Internal reset signal is generated.	Internal reset signal is not generated.	Internal reset signal is generated when the source clock to the watchdog timer resumes operation.
Access WDTE by 1-bit memory manipulation instruction				

[Details of correction]

- Modification of **Caution 3** on **Figure 10-2 Format of Watchdog Timer Mode Register (WDTM)** on page 219

Incorrect)

Caution 3. After reset is released, WDTM can be written only once by an 8-bit memory manipulation instruction. If writing attempted a second time, an internal reset signal is generated.

Correct)

Caution 3. After reset is released, WDTM can be written only once by an 8-bit memory manipulation instruction. If writing attempted a second time during watchdog timer operation, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.

- Addition of **Caution 5** to **Figure 10-2 Format of Watchdog Timer Mode Register (WDTM)** on page 219

Caution 5. If “Ring-OSC cannot be stopped by software” is selected by the option byte and the watchdog timer is stopped by setting WDCS4 to 1, the watchdog timer does not resume operation even if WDCS4 is cleared to 0. In addition, the internal reset signal is not generated.

- Modification of **Cautions 1** and **2** on **Figure 10-3 Format of Watchdog Timer Enable Register (WDTE)** on page 219

Incorrect)

- Cautions 1.** If a value other than ACH is written to WDTE, an internal reset signal is generated.
- 2.** If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated.

Correct)

- Cautions 1.** If a value other than ACH is written to WDTE, an internal reset signal is generated. **If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.**
- 2.** If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated. **If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.**