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78K0/KB1 Document Modification		Document No.	SBG-DT-03-0294-E		1/2
		Date issued	November 19, 2003		
		Issued by	Microcomputer Group 2nd Solutions Division Solutions Operations Unit NEC Electronics Corporation		
Related documents	78K0/KB1 User's Manual: U15836EJ4V0UD00	Notification classification		Usage restriction	
				Upgrade	
			√	Document modification	
				Other notification	

1. Affected products

   μPD780101, 780102, 780103

   μPD78F0103Mx (x = 1 to 6)

2. Details of correction of erroneous description

(1) Erroneous descriptions have been found in **CHAPTER 5 CLOCK GENERATOR** as shown below.

AC Characteristics on page 363 defines the minimum instruction execution time only for 240 kHz (TYP.) operation when Ring-OSC is selected as the CPU clock, but **Figure 5-2 Format of Processor Clock Control Register (PCC)** on page 87 shows the ratings of the divided Ring-OSC clock frequency.

In the standard products and (A) grade products, the CPU can operate on a Ring-OSC clock divided by up to 2. Dividing the clock frequency in the (A1) grade products (A2) grade products is not possible.

See attachment 2 for details.

(2) Erroneous descriptions have been found in **CHAPTER 9 WATCHDOG TIMER** as shown below.

Caution 3 in **Figure 9-2 Format of Watchdog Timer Mode Register (WDTM)** on page 176 indicates, "After reset is released, WDTM can be written only once by an 8-bit memory manipulation instruction. If writing attempted a second time, an internal reset signal is generated." However, the internal reset signal is not generated while the watchdog timer operation is stopped.

Caution 1 in **Figure 9-3 Format of Watchdog Timer Enable Register (WDTE)** on page 176 indicates, "If a value other than ACH is written to WDTE, an internal reset signal is generated" and **Caution 2** indicates, "If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated." However, the internal reset signal is not generated while the watchdog timer operation is stopped.

See attachment 3 for details.

3. Action

Correction of the erroneous descriptions in this document will be reflected in the next revision of the user's manual.

4. List of erroneous description corrections

The history of erroneous description corrections and detailed information will be described on the following pages.

5. Revision history

78K0/KB1 Document Modification Revision History

Document Number	Date Issued	Description
SBG-DT-03-0002-E	January 14, 2003	Newly created.
SBG-DT-03-0163-E	May 28, 2003	Addition of restriction (No.6)
SBG-DT-03-0294-E	November 19, 2003	Addition of erroneous description corrections (No.1 and No.2)

Correction History of Erroneous Descriptions in 78K0/KB1

1. Product History

No.	Description	78K0/KB1 User's Manual
	Edition (Document No.)	4th Edition (U15836EJ4V0) or Earlier
1	Erroneous description on Ring-OSC clock division	×
2	Erroneous description on watchdog timer	×

Note The meaning of each symbol is as follows.

–: Erroneous description exists

√: Erroneous description already corrected

×: Erroneous description will be corrected

2. Details of Correction of Erroneous Descriptions

Item 1: The correction added this time (see attachment 2).

Item 2: The correction added this time (see attachment 3).

No.1 Erroneous description on Ring-OCS clock division

Erroneous descriptions have been found in **CHAPTER 5 CLOCK GENERATOR** as shown below.
AC Characteristics on page 363 defines the minimum instruction execution time only for 240 kHz (TYP.) operation when Ring-OSC is selected as the CPU clock, but **Figure 5-2 Format of Processor Clock Control Register (PCC)** on page 87 shows the ratings of the divided Ring-OSC clock frequency.

In the standard products and (A) grade products, the CPU can operate on a Ring-OSC clock divided by up to 2. Dividing the clock frequency in the (A1) grade products (A2) grade products is not possible.

[Details of correction]

• Modification of **Figure 5-2 Format of Processor Clock Control Register (PCC)** on page 87

Incorrect)

PCC2	PCC1	PCC0	CPU clock (f_{CPU}) selection		
				MCM0 = 0	MCM0 = 1
0	0	0	f_X	f_R	f_{XP}
0	0	1	$f_X/2$	$f_R/2$	$f_{XP}/2$
0	1	0	$f_X/2^2$	$f_R/2^2$	$f_{XP}/2^2$
0	1	1	$f_X/2^3$	$f_R/2^3$	$f_{XP}/2^3$
1	0	0	$f_X/2^4$	$f_R/2^4$	$f_{XP}/2^4$
Other than above			Setting prohibited		

Correct)

PCC2	PCC1	PCC0	CPU clock (f_{CPU}) selection		
				MCM0 = 0	MCM0 = 1
0	0	0	f_X	f_R	f_{XP}
0	0	1	$f_X/2$	$f_R/2$ Note	$f_{XP}/2$
0	1	0	$f_X/2^2$	Setting prohibited	$f_{XP}/2^2$
0	1	1	$f_X/2^3$	Setting prohibited	$f_{XP}/2^3$
1	0	0	$f_X/2^4$	Setting prohibited	$f_{XP}/2^4$
Other than above			Setting prohibited		

Note Setting prohibited in the (A1) grade and (A2) grade products.

• Modification of **Table 5-2 Relationship Between CPU Clock and Minimum Instruction Execution Time** on page 88

Incorrect)

CPU Clock (f_{CPU})	Minimum Instruction Execution Time: $2/f_{CPU}$	
	X1 Input Clock[Note] (at 10 MHz Operation)	Ring-OSC Clock[Note] (at 240 kHz (TYP.) Operation)
f_X	0.2 μs	8.3 μs (TYP.)
$f_X/2$	0.4 μs	16.6 μs (TYP.)
$f_X/2^2$	0.8 μs	33.2 μs (TYP.)
$f_X/2^3$	1.6 μs	66.4 μs (TYP.)
$f_X/2^4$	3.2 μs	132.8 μs (TYP.)

Note The main clock mode register (MCM) is used to set the CPU clock (X1 input clock/Ring-OSC clock) (see **Figure 5-4**).

Correct)

CPU Clock (f_{CPU})	Minimum Instruction Execution Time: $2/f_{CPU}$	
	X1 Input Clock[Note 1] (at 10 MHz Operation)	Ring-OSC Clock[Note 1] (at 240 kHz (TYP.) Operation)
f_X	0.2 μs	8.3 μs (TYP.)
$f_X/2$	0.4 μs	16.6 μs (TYP.) [Note 2]
$f_X/2^2$	0.8 μs	–
$f_X/2^3$	1.6 μs	–
$f_X/2^4$	3.2 μs	–

Notes 1. The main clock mode register (MCM) is used to set the CPU clock (X1 input clock/Ring-OSC clock) (see **Figure 5-4**).

2. Setting prohibited in the (A1) grade and (A2) grade products.

• Modification of **AC Characteristics** on page 372

Incorrect)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock operation	X1 input clock	4.0 V ≤ V_{DD} ≤ 5.5 V	0.2		16	μs
				3.3 V ≤ V_{DD} < 4.0 V	0.238		16	μs
				2.7 V ≤ V_{DD} < 3.3 V	0.4		16	μs
			Ring-OSC clock		4.17	8.33	16.67	μs

Correct)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock operation	X1 input clock	4.0 V ≤ V_{DD} ≤ 5.5 V	0.2		16	μs
				3.3 V ≤ V_{DD} < 4.0 V	0.238		16	μs
				2.7 V ≤ V_{DD} < 3.3 V	0.4		16	μs
			Ring-OSC clock		4.17		33.33	μs

No.2 Erroneous description on watchdog timer

Erroneous descriptions have been found in **CHAPTER 9 WATCHDOG TIMER** as shown below.
Caution 3 in **Figure 9-2 Format of Watchdog Timer Mode Register (WDTM)** on page 172 indicates, "After reset is released, WDTM can be written only once by an 8-bit memory manipulation instruction. If writing attempted a second time, an internal reset signal is generated." However, the internal reset signal is not generated while the watchdog timer operation is stopped.

Caution 1 in **Figure 9-3 Format of Watchdog Timer Enable Register (WDTE)** on page 176 indicates, "If a value other than ACH is written to WDTE, an internal reset signal is generated" and **Caution 2** indicates, "If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated." However, the internal reset signal is not generated while the watchdog timer operation is stopped.

The relationship between the watchdog timer operation and the internal reset signal is shown below.

Internal Reset Signal Generation Cause	Ring-OSC Cannot Be Stopped	Ring-OSC Can Be Stopped by Software		
		Watchdog Timer Is Operating	Watchdog Timer Stopped	
			WDCS4 Is Set to 1	Source Clock to Watchdog Timer Is Stopped
Watchdog timer counter overflows	Internal reset signal is generated.	Internal reset signal is generated.	–	–
Write to WDTM for the second time	Internal reset signal is generated.	Internal reset signal is generated.	Internal reset signal is not generated and the watchdog timer does not resume operation.	Internal reset signal is generated when the source clock to the watchdog timer resumes operation.
Write other than "ACH" to WDTE	Internal reset signal is generated.	Internal reset signal is generated.	Internal reset signal is not generated.	Internal reset signal is generated when the source clock to the watchdog timer resumes operation.
Access WDTE by 1-bit memory manipulation instruction				

[Details of correction]

• Modification of **Caution 3** on **Figure 9-2 Format of Watchdog Timer Mode Register (WDTM)** on page 176

Incorrect)

Caution 3. After reset is released, WDTM can be written only once by an 8-bit memory manipulation instruction. If writing attempted a second time, an internal reset signal is generated.

Correct)

Caution 3. After reset is released, WDTM can be written only once by an 8-bit memory manipulation instruction. If writing attempted a second time during watchdog timer operation, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.

• Addition of **Caution 5** to **Figure 9-2 Format of Watchdog Timer Mode Register (WDTM)** on page 176

Caution 5. If "Ring-OSC cannot be stopped by software" is selected by the option byte and the watchdog timer is stopped by setting WDCS4 to 1, the watchdog timer does not resume operation even if WDCS4 is cleared to 0. In addition, the internal reset signal is not generated.

• Modification of **Cautions 1** and **2** on **Figure 9-3 Format of Watchdog Timer Enable Register (WDTE)** on page 176

Incorrect)

Cautions 1. If a value other than ACH is written to WDTE, an internal reset signal is generated.

2. If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated.

Correct)

Cautions 1. If a value other than ACH is written to WDTE, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.

2. If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.