78K0/Fx2 Microcontrollers Technical Notification (Technical limitation, Direction of use, Document modification, Specification addition)	Document No.	ZBG-BG-08-0003	1/1
	Data issued	July 3, 2008	
	Issued by	1st Body Solution Group Automotive Systems Division Microcomputer Operations Unit NEC Electronics Corporation	
Related documents 78K0/FC2 User's Manual: U17555EJ4V0UD00 78K0/FE2 User's Manual: U17554EJ4V0UD00 78K0/FF2 User's Manual: U17553EJ4V0UD00	Notification classification	√	Usage restriction
			Upgrade
		√	Document Modification
		√	Other notification

1. Affected products

- All Products of 78K0/Fx2 microcontroller

78K0/FC2: μPD78F0881, μPD78F0882, μPD78F0883, μPD78F0884, μPD78F0885, μPD78F0886
78K0/FE2: μPD78F0887, μPD78F0888, μPD78F0889, μPD78F0890
78K0/FF2: μPD78F0891, μPD78F0892, μPD78F0893

2. Summary

[Direction of use]

The following direction of use has been added to this Technical Notification.

- Clock generator STOP instruction execution
  - ✓ Direction of use:

    If the microcontroller is using the internal high-speed oscillator (f_{RH}) as the CPU clock, then when a STOP instruction is executed, under certain circumstances the device will enter a state of incorrect operation and it will not exit from STOP mode from an interrupt.
    Please refer to attachment 8 for details.

    <Workaround>
    It is possible to avoid by checking RSTS bit or wait oscillator stabilization with software.
    Device modification for this restriction is not planned.

- Flash memory programming
  - ✓ Direction of use:

    There is an issue with the device not entering into flash programming mode in case that the duration of the reset signal applied to the RESET is shorter than 1,950 ms when entering the flash programming mode during user program operation.
    Please refer to attachment 9 for details.

    <Workaround>
    Secure a reset period for 1,950 ms or longer by controlling the external RESET pin when leading the flash memory programming mode.
    Device modification for this restriction is not planned.

List of Usage Technical Notifications in 78K0/Fx2 Microcontrollers

1. Product History

No.	Description	Non "A" version	"A" version
		FC2 : μPD78F0881/F0882/ F0883/F0884/F0885/F0886 FE2 : μPD78F0887/F0888/ F0889/F0890 FF2 : μPD78F0891/F0892/F0893	FC2 : μPD78F0881A/F0882A/ F0883A/F0884A/F0885A/F0886A FE2 : μPD78F0887A/F0888A/ F0889A/F0890A FF2 : μPD78F0891A/F0892A/F0893A
1	Low Voltage Detector (LVI) function -1 (Direction of use)	X	√
2	Low Voltage Detector (LVI) function -2 (Direction of use)	Δ	Δ
3	aFCAN wakeup from CAN sleep mode(Direction of use)	Δ	Δ
7	Clock generator STOP instruction execution (Direction of Use)	Δ	Δ
8	Flash memory programming (Direction of Use)	Δ	Δ

Remark: The meaning of each symbol is as follows.

√ : Already corrected
X : Applicable (correction is planned)
Δ : Applicable (correction is not planned)

1. Details of Previous description

Item 1 : Please refer to attachment 2
Item 2 : Please refer to attachment 3
Item 3 : Please refer to attachment 4
Item 7 : Please refer to attachment 8
Item 8 : Please refer to attachment 9

List of Additional Function in 78K0/Fx2 Microcontrollers

No.	Description	78K0/FC2			78K0/FE2	78K0/FF2
		μPD78F0881/F0882/ F0883	μPD78 F0884/F0885/ F0886			
	Rank	–	I	K,X	–	–
4	Add function of A/D converter to P90	–	Δ	X	–	–

Remark: The meaning of each symbol is as follows.

– : Not applicable
X : Applicable (function is added)
Δ : Applicable (function is not added)

Note There are no difference between RANK I and K/X on the device. The deference is tested or non tested.

1. Details of Previous description

Item 4: Please refer to attachment 5

List of Document Modifications in 78K0/Fx2 Microcontrollers

No.	Description	78K0/FC2	78K0/FE2	78K0/FF2
	Revision	Before 4th edition	Before 4th edition	Before 4th edition
5	Interrupt response time at self programming (Document modification)	X	X	X
6	Specification addition for Peripheral hardware clock (Specification addition)	X	X	X

Remark: The meaning of symbol is as follows.

X : Previous description applies (new is planned)

1. Details of Previous description

Item 5: Please refer to attachment 6
Item 6: Please refer to attachment 7

Item 1 (Direction of use): Low Voltage Detector (LVI) function -1

[Affected products]

78K0/FC2: μPD78F0881, μPD78F0882, μPD78F0883, μPD78F0884, μPD78F0885, μPD78F0886
78K0/FE2: μPD78F0887, μPD78F0888, μPD78F0889, μPD78F0890
78K0/FF2: μPD78F0891, μPD78F0892, μPD78F0893

[Description]

Affected usage

In case that LVI is used as RESET, this restriction will be affected.
If LVI is not used or used as "interrupt" source, this is not affected.

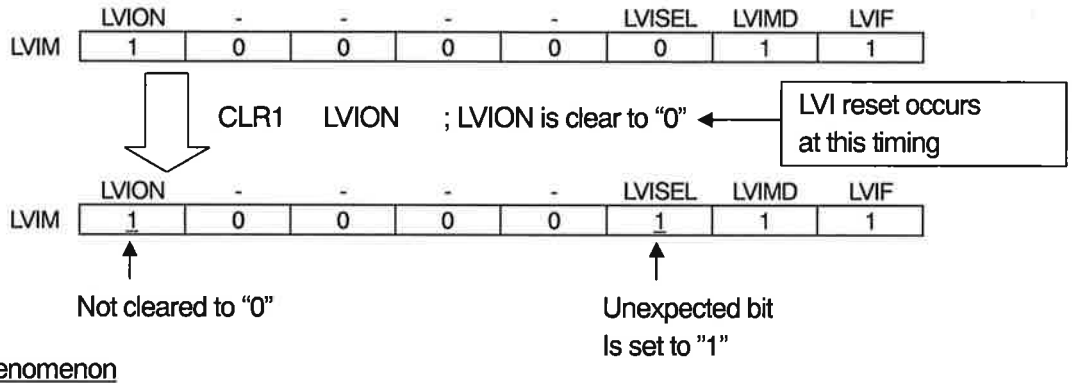
Phenomenon

If LVI reset occurs at the same timing of write timing for LVI registers (LVIS/LVIM), the value of SFR-bit of these registers might become "1". As a result, the following two phenomenon are occurred.

- LVI will be not stopped.
- Low voltage detect pin will be changed to "EXLVI" pin.
- LVI detect voltage will be changed to the lower level than the level which is set by LVIS.

These phenomenon will not be occurred by other reset signal.
Figure 1 shows the example in case this phenomenon occurs at the timing that LVION flag is operated.

Figure 1. Example of phenomenon which occurs when LVION flag is cleared to "0"



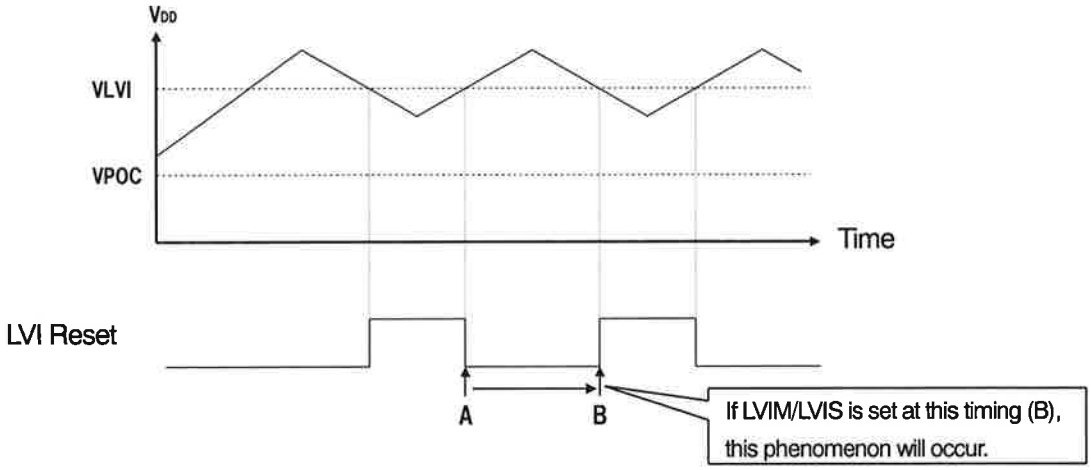
Cause of Phenomenon

Internal bus which connected to LVIM/LVIS register will become "High level" in case reset signal occurs. And these two registers will not be cleared by "LVI reset".
When SFR is written, CPU set the writing value to the bus, and the value will be set to SFR at the write signal timing. But if SFR is written during the timing internal bus is reset by LVI reset, unexpected value (=1) may be set to LVIM or LVIS register. This phenomenon may also occur in case bit manipulation instruction for LVIM/LVIS is executed.
Manipulation except for LVIM/LVIS does not affect to this phenomenon.

Example of Phenomenon

In case VDD voltage is moving around LVI detect voltage (V_{LVI}), LVI reset occur many times. In case program always initializes LVIM and LVIS after reset is released, if the time from LVI reset release timing (Figure 2-A) to LVI reset generation timing (Figure 2-B) and the time from LVI reset release timing to initialization of LVIM /LVIS correspond, this phenomenon will occur.

Figure 2 Example of Phenomenon

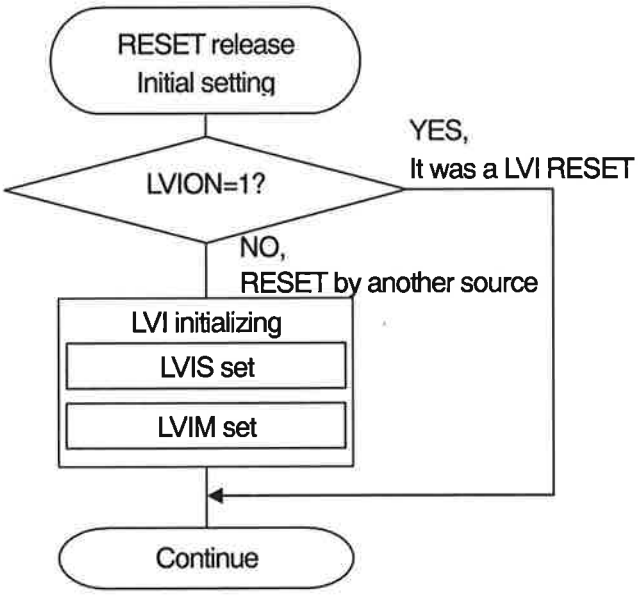


[Workaround]

It is possible to avoid by following two software workaround.

1. In case LVI is used as RESET, please do not write LVIM/LVIS register after once these registers is set.
2. Before setting of LVIM/LVIS register, please confirm that bit-7 of LVIM register (LVION) is "0". If LVION is "1", do not execute the write instruction for LVIM/LVIS. By this workaround, LVIM/LVIS will be set when external reset or POC reset or Watchdog timer reset is occurred, and not be set when LVI reset is occurred.

Both LVIRF and WDTRF might become "1" because Reset control flag register (RESF) is the register which is not cleared by LVI reset or Watchdog timer reset. When LVIRF bit is used for this judgment, it will be possible to judge LVI reset is occurred or not, but the additional instructions is needed to judge whether LVIM/LVIS is cleared by WDT reset or not. Therefore, please use LVION flag for workaround of this restriction.



[Permanent workaround]

The Specification-Expanded products will be modified. The product name of the modified product will be changed. Detail of Specification-Expanded products is described at "8bit Microcontrollers 78K0/Fx2 Release of Specification-Expanded Products" (ZBB-BG-06-0102).

Current product name : μPD78F08xx
Modified product name : μPD78F08xxA.

Please apply workaround for current products (non A version).

Item 2 (Direction of use): Low Voltage Detector (LVI) function -2

[Affected products]

All products for 78K0/Fx2 microcontrollers

[Description]

Affected usage

In case that LVI is used as "Interrupt" source and LVION flag is cleared during CPU is running, this phenomenon will be affected.

If LVI is not used or used as "RESET", or used as "Interrupt" source but LVION flag is not cleared during CPU is running, this is not affected.

Phenomenon

In case that LVI is used as "Interrupt" source, If LVI operation is disabled (LVION=0) during the voltage level of selected pin (VDD or EXLVI) for LVI detection is less than the LVI detect voltage (VLVI), interrupt request flag of LVI (LVIIF) becomes "1", and interrupt will occur if interrupt mask is enabled (LVIMK=0).

[Workaround]

In case that LVI is used as "Interrupt" source, and If LVI operation have to be disabled (LVION=0) during the voltage level of selected pin (VDD or EXLVI) for LVI detection is less than the LVI detect voltage (VLVI), please set interrupt mask flag (LVIMK=1) before LVI operation is disabled (LVION=0), and clear interrupt request flag (LVIIF=0) after LVI operation is disabled (LVION=0).

- **Item 3 (Direction of use): aFCAN wakeup from CAN sleep mode**

[Affected products]

All products for 78K0/Fx2 microcontrollers

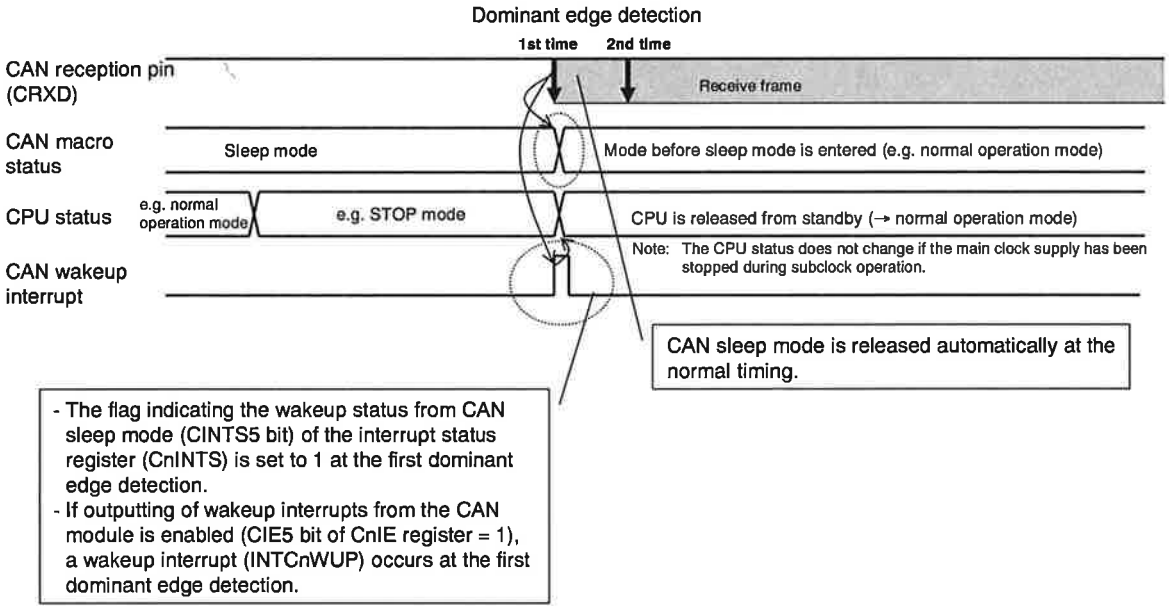
[Description]

Affected usage

In case that the CAN operation clock (peripheral hardware clock) is not supplied in CAN sleep mode (condition under which this caution does not apply)

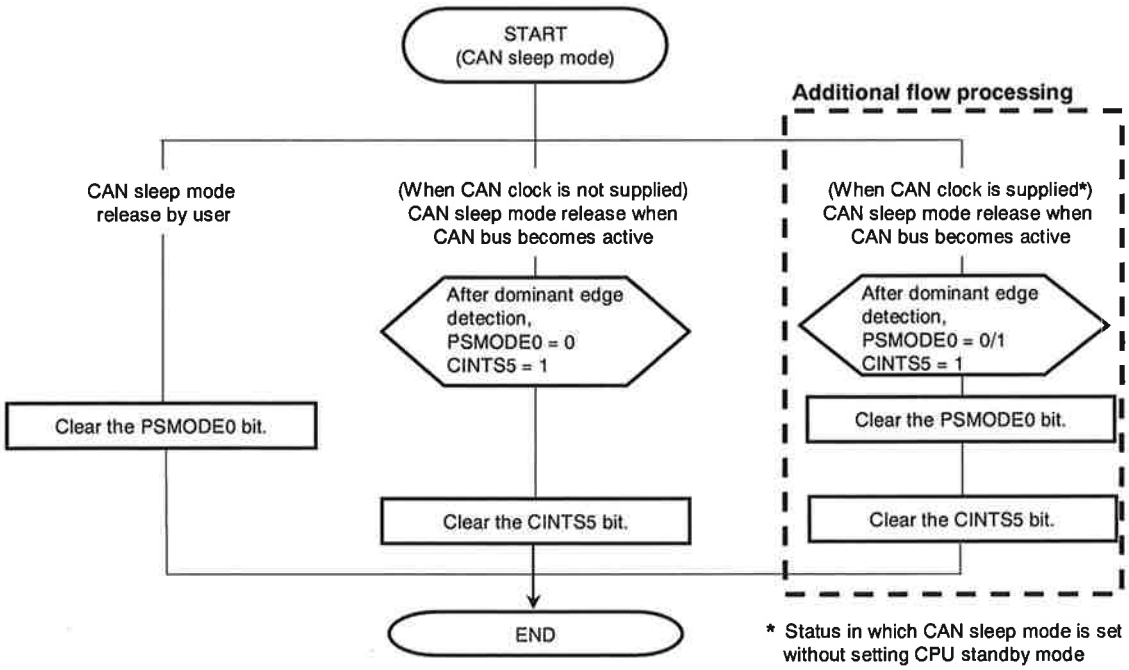
Phenomenon

A delay in returning from CAN sleep mode does not occur.



[Workaround]

When a wakeup interrupt occurs in CAN sleep mode, release CAN sleep mode with software (by clearing the PSMODE0 bit).



Item 4(Additional function): Function Addition for P90

[Affected products]

78K0/FC2 : μPD78F0884, μPD78F0885, μPD78F0886
RANK K or X

[Description]

The function of A/D converter ANI8 pin is added on P90 pin.
And added some registers to control this function. Descriptions for the added A/D converter pin will be modified in next version.

[Document Revision Plan]

This description have been modified in U17555EJ3V0UD00.

Item 5 (Document Modification): Interrupt response time at self programming

[Affected products]

All products for 78K0/Fx2 microcontrollers

[Description]

Descriptions will be changed in interrupt response time of Flash memory self programming.

Interrupt response time during Flash self programming might becomes longer than the time described in User's manual.

The deference about response time by Compiler model and clock setting will also be added.

[Previous description]

Maximum interrupt response time (us) in case internal high-speed oscillation clock is used.

Library Name	Location of "Entry RAM" is out of short direct addressing range	Location of "Entry RAM" is within short direct addressing range
Block blank check library	1300.5	727.5
Block erase library	1393.5	820.5
Word write library	1289.5	716.5
Block verify library	1324.5	751.5
Set information library	852.5	279.5
EEPROM write library	1395.5	822.5

Maximum interrupt response time (us) in case high-speed system clock is used.

Library Name	Location of "Entry RAM" is out of short direct addressing range	Location of "Entry RAM" is within short direct addressing range
Block blank check library	28/fx+698	28/fx+462
Block erase library	28/fx+745	28/fx+509
Word write library	28/fx+693	28/fx+457
Block verify library	28/fx+709	28/fx+473
Set information library	28/fx+454	28/fx+218
EEPROM write library	28/fx+783	28/fx+547

Remark: fx is high-speed system clock

[New description]

Maximum interrupt response time (us) in case internal high-speed oscillation clock is used. (Normal model, RSTS=1)

Library Name	Location of "Entry RAM" is out of short direct addressing range	Location of "Entry RAM" is within short direct addressing range
Block blank check library	933.6	668.6
Block erase library	1026.6	763.6
Word write library	2505.8	1942.8
Block verify library	958.6	693.6
Set information library	476.5	211.5
EEPROM write library	2760.8	2168.8

Remark: RSTS is a register that indicates the high-speed internal oscillator status (RSTS=1: High-speed internal oscillator operation is stable.)

Maximum interrupt response time (us) in case internal high-speed oscillation clock is used. (Static model, RSTS=1)

Library Name	Location of "Entry RAM" is out of short direct addressing range	Location of "Entry RAM" is within short direct addressing range
Block blank check library	927.9	662.9
Block erase library	1020.9	757.9
Word write library	2497.8	1934.8
Block verify library	952.9	687.9
Set information library	475.5	210.5
EEPROM write library	2759.5	2167.5

Remark: RSTS is a register that indicates the high-speed internal oscillator status (RSTS=1: High-speed internal oscillator operation is stable.)

Maximum interrupt response time (us) in case high-speed system clock is used. (Normal model, RSTOP=0, RSTS=1)

Library Name	Location of "Entry RAM" is out of short direct addressing range	Location of "Entry RAM" is within short direct addressing range
Block blank check library	179/fcpu+507	179/fcpu+407
Block erase library	179/fcpu+559	179/fcpu+460
Word write library	333/fcpu+1589	333/fcpu+1298
Block verify library	179/fcpu+518	179/fcpu+418
Set information library	80/fcpu+370	80/fcpu+165
EEPROM write library	29/fcpu+1759	29/fcpu+1468
	333/fcpu+834	333/fcpu+512

Remarks 1. fcpu is a CPU operating clock frequency. The maximum interrupt response time for the EEPROM write library varies depending on the clock frequency. Assign the frequency to be used, calculate the time, and take the largest value as its maximum time.

2. RSTOP is a register that sets whether to operate or stop the high-speed internal oscillator (RSTOP=0: High-speed internal oscillator operates)

3. RSTS is a register that indicates the high-speed internal oscillator status (RSTS=1: High-speed internal oscillator operation is stable.)

Note This spec is calculated by used NEC compiler and self-programming library which would be published with the 78K0/Fx2 Flash Memory Self Programming User's Manual at January 2007.

Maximum interrupt response time (us) in case high-speed system clock is used. (Normal model, RSTOP=1, RSTS=1)

Library Name	Location of "Entry RAM" is out of short direct addressing range	Location of "Entry RAM" is within short direct addressing range
Block blank check library	179/fcpu+1650	179/fcpu+714
Block erase library	179/fcpu+1702	179/fcpu+767
Word write library	333/fcpu+2732	333/fcpu+1605
Block verify library	179/fcpu+1661	179/fcpu+725
Set information library	80/fcpu+1513	80/fcpu+472
EEPROM write library	29/fcpu+1759	29/fcpu+1468
	333/fcpu+2061	333/fcpu+873

Remarks 1. fcpu is a CPU operating clock frequency. The maximum interrupt response time for the EEPROM write library varies depending on the clock frequency. Assign the frequency to be used, calculate the time, and take the largest value as its maximum time.

2. RSTOP is a register that sets whether to operate or stop the high-speed internal oscillator (RSTOP=1: High-speed internal oscillator stop)

Maximum interrupt response time (us) in case high-speed system clock is used. (Static model, RSTOP=0, RSTS=1)

Library Name	Location of "Entry RAM" is out of short direct addressing range	Location of "Entry RAM" is within short direct addressing range
Block blank check library	136/fcpu+507	136/fcpu+407
Block erase library	136/fcpu+559	136/fcpu+460
Word write library	272/fcpu+1589	272/fcpu+1298
Block verify library	136/fcpu+518	136/fcpu+418
Set information library	72/fcpu+370	72/fcpu+165
EEPROM write library	19/fcpu+1759	19/fcpu+1468
	268/fcpu+834	268/fcpu+512

Remarks 1. fcpu is a CPU operating clock frequency. The maximum interrupt response time for the EEPROM write library varies depending on the clock frequency. Assign the frequency to be used, calculate the time, and take the largest value as its maximum time.

2. RSTOP is a register that sets whether to operate or stop the high-speed internal oscillator (RSTOP=0: High-speed internal oscillator operates)

3. RSTS is a register that indicates the high-speed internal oscillator status (RSTS=1: High-speed internal oscillator operation is stable.)

Maximum interrupt response time (us) in case high-speed system clock is used. (Static model, RSTOP=1)

Library Name	Location of "Entry RAM" is out of short direct addressing range	Location of "Entry RAM" is within short direct addressing range
Block blank check library	136/fcpu+1650	136/fcpu+714
Block erase library	136/fcpu+1702	136/fcpu+767
Word write library	272/fcpu+2732	272/fcpu+1605
Block verify library	136/fcpu+1661	136/fcpu+725
Set information library	72/fcpu+1513	72/fcpu+472
EEPROM write library	19/fcpu+1759	19/fcpu+1468
	268/fcpu+2061	268/fcpu+873

Remarks 1. fcpu is a CPU operating clock frequency. The maximum interrupt response time for the EEPROM write library varies depending on the clock frequency. Assign the frequency to be used, calculate the time, and take the largest value as its maximum time.

2. RSTOP is a register that sets whether to operate or stop the high-speed internal oscillator (RSTOP=1: High-speed internal oscillator stop)

Note This spec is calculated by used NEC compiler and self-programming library which would be published with the 78K0/Fx2 Flash Memory Self Programming User's Manual at January 2007.

[Document Revision Plan]

This description will be modified in next revision.

Item 6 (Specification Addition): Peripheral hardware clock

[Affected products]

All products for 78K0/Fx2 microcontrollers

[Description]

AC specification for peripheral hardware clock was not described.

AC specification for peripheral hardware clock (f_{PRS}) is limited by operation voltage range as same as CPU clock.

Peripheral hardware clock frequency

Parameter	Symbol	Conditions		MIN		MAX	Unit
Peripheral hardware clock frequency	f_{PRS}	XSEL=1	4.0V=V_{DD}=5.5V			20	MHz
			2.7V=V_{DD}<4.0V			10	
			1.8V=V_{DD}<2.7V			5	
		XSEL=0	2.7V=V_{DD}=5.5V	7.6		8.4	MHz
			1.8V=V_{DD}<2.7V[Note]	7.6		10.4	

Note This specification is described as internal high-speed oscillator frequency characteristics. When this clock is used for peripheral hardware, please select the divided source clock for each peripheral clock selection.

[Document Revision Plan]

This description will be modified in next revision.

• Item 7 (Direction of use): Clock generator STOP instruction execution

[Affected products]

All products for 78K0/Fx2 microcontrollers

[Description]

Affected usage

In case that STOP instruction is executed at high-speed oscillator period.

Phenomenon

If the microcontroller is using the internal high-speed oscillator (fRH) as the CPU clock, then when a STOP instruction is executed, under certain circumstances the device will enter a state of undefined operation and it will not exit from STOP mode by interrupt. There are certain timing conditions between the execution of the STOP instruction and the internal high speed oscillator which cause this situation and they are listed below.

- The instruction is executed 888-889 clock cycles after the internal high speed oscillator is enabled (RSTOP set to 0).
- The instruction is executed 888-889 clock cycles after the device exits from STOP mode, and the CPU was operating from the high speed internal oscillator prior to entering STOP mode and continues to operate from the same clock source when it exits STOP mode.
- The instruction is executed 408-701 clock cycles after the device finishes initializing after a non-POC (power up) Reset; i.e. WDT, LVI, external reset.

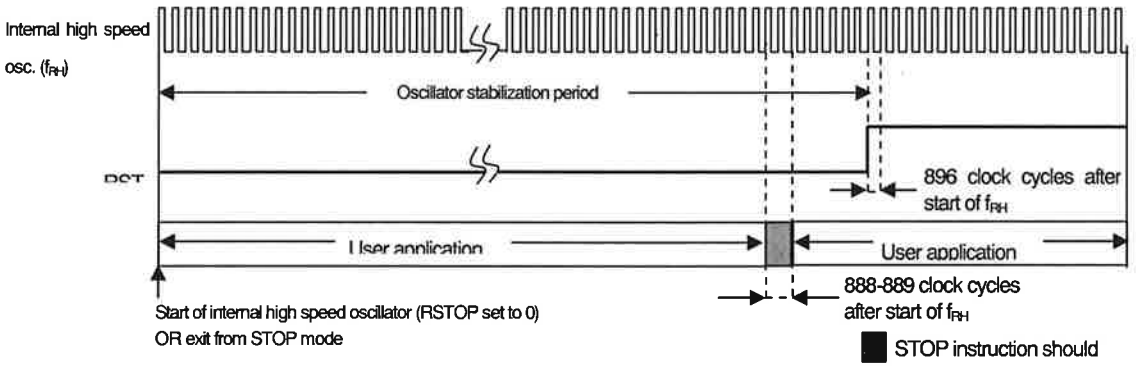


Fig. 4−1 Operation of internal high-speed oscillator after initial starting or after exit from STOP mode

NOTE: Figure is not drawn to scale.

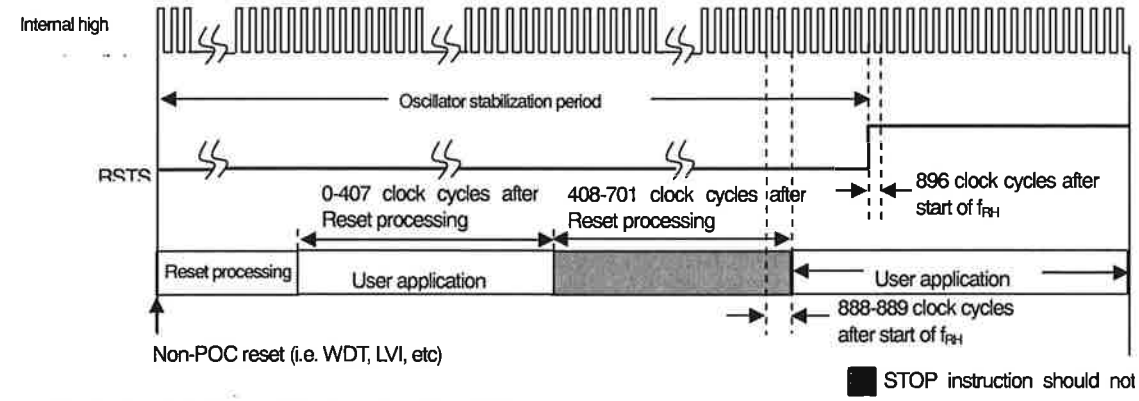


Fig. 4−2 Reset due to factors other than POC

NOTE: Figure is not drawn to scale

When one of the described situations occur s, the device abnormally enters into STOP mode. As a result, the following conditions occur-

• The device will not exit STOP mode when an interrupt occurs

• The internal high speed oscillator does not stop. Hence the current consumption is greater than what is specified for STOP mode; approximately 150-400 uA.

If the watchdog timer is enabled (WDTON=1) and it is configured to operate in STOP mode (Option Byte->LSROSC=1), then it can Reset the device once the counter overflows and release the device from STOP mode.

[Workaround]

This condition can be avoided using a software modification. There are two different modifications which can be utilized.

1) Postpone the execution of the STOP instruction until a check is performed on the RSTS bit and it is verified that it is 1.
2) A delay is implemented in the software such that it can be insured that the STOP instruction will not be executed until after the previously mentioned conditions have passed.

It is suggested to use modification (1) if the STOP instruction will be executed during interrupt processing.

Following is a table of application conditions and which modifications will work for each.

Application condition	Modification	
	(1)	(2)
STOP instruction will be executed shortly after the internal high speed oscillator begins operation	✓	✓
STOP instruction will be executed shortly after exiting STOP mode	✓	✓
STOP instruction will be executed shortly after a non-POC reset	✓	✓
The time from which the internal high speed oscillator begins to when the STOP instruction will be executed can not be defined	✓	×

✓:Not applicable

× applicable

- **Item 8 (Direction of use): Flash memory programming**

[Affected products]

All products for 78K0/Fx2 microcontrollers

[Description]

Affected usage

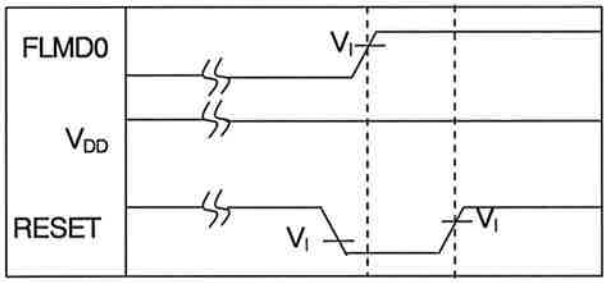
In case that the duration of the reset signal applied to the RESET is shorter than 1,950 ms when entering the flash programming mode during user program operation.

Phenomenon

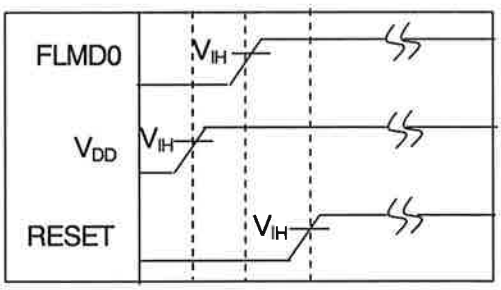
There is an issue with the device not entering into flash programming mode. There are two situations in which the microcontroller may not enter into the programming mode and they are listed below.

•When the Run After Disconnect function is used during programming with the flash memory programmer (PG-FP5) or MINICUBE2.
•When the programming environment has been configured based on the Application Note (Programmer) (U17739EJ2V0AN00) and when leading the user program operation to the flash memory programming mode (Figure 5-1 (1))

Even if either of the above situations exist, the device may still correctly enter into programming mode and the flash can be successfully programmed. If the verify indicates correct programming, then the flash programming worked correctly.
This issue is not applicable for the circumstances listed below.
• When entering into the programming mode at the same time as power-on
• When performing self programming
• When performing EEPROM emulation



① Entering into flash programming mode during user program operation



② Entering into flash programming mode at the same time as power-on

Figure 5-1 Methods of entering flash memory programming mode

If the duration of the reset signal applied to the external RESET pin is shorter than 1,950 ms when entering the flash programming mode during user program operation without dropping the power supply voltage to the level of the POC detection voltage (VPOC = 1.59 V ±0.15 V), the following phenomenon may occur.
• A POC reset occurs upon reset release and the flash memory programming mode is not entered normally. Consequently, the user program is executed without performing programming processing.

[Workaround]

Secure a reset period for 1,950 ms or longer by controlling the external RESET pin when leading the flash memory programming mode.

For those configuring the programming environment based on the Application Note (Programmer) (U17739EJ2V0AN00). Please apply and use the workaround.
For 3rd party programmers please contact directly the manufacturer of your programmer.