Microcontroller Technical Information

32-Bit Microcontrollers V850E/MA3 Usage Restrictions		Document No.	ZBG-CC-07-0025		1/1
		Date issued	December 18, 2007		
		Issued by	2nd Product Solution Group Multipurpose Microcomputer Systems Division Microcomputer Operations Unit NEC Electronics Corporation		
Related documents	V850E/MA3 Hardware User's Manual: U16397EJ V850E1 Architecture User's Manual: U14559EJ	Notification classification	√	Usage restriction	
				Upgrade	
				Document modification	
				Other notification	

1. Affected products

V850E/MA3

- μPD703131A, μPD703131AY, μPD703131BY (ROM: 256 KB, RAM: 16 KB)
- μPD703132A, μPD703132AY, μPD703132BY (ROM: 256 KB, RAM: 32 KB)
- μPD703133A, μPD703133AY, μPD703133BY (ROM: 512 KB, RAM: 16 KB)
- μPD703134A, μPD703134AY, μPD703134BY (ROM: 512 KB, RAM: 32 KB)
- μPD703136A, μPD703136AY, μPD703136BY (ROM: 256 KB, RAM: 8 KB)
- μPD70F3134A, μPD70F3134AY, μPD70F3134BY (flash memory: 512 KB, RAM: 32 KB)

Remark For restrictions on non-A products (μPD703131, μPD703132, μPD703133, μPD703134, μPD70F3134 and μPD70F3134Y), individually contact an NEC Electronics sales representative or distributor.

2. Notification

The product lineup has been revised in conjunction with a release of V850E/MA3 version B products (notified in document ZBB-CC-07-0256).

3. List of restrictions

The restriction history and detailed information is described in the attachment.

4. Document revision history

32-Bit Microcontrollers V850E/MA3 Usage Restrictions

Document Number	Date Issued	Description
ZBG-CC-05-0011	January 17, 2005	Newly created. Addition of restriction No. 1.
ZBG-CC-06-0031	September 1, 2006	Addition of restriction No. 2
ZBG-CC-07-0025	December 18, 2007	Revision of product lineup

List of Usage Restrictions in V850E/MA3

1. Product Version

μPD703131A: Rank K
μPD703131AY: Rank K
μPD703132A: Rank K
μPD703132AY: Rank K
μPD703133A: Rank K
μPD703133AY: Rank K
μPD703134A: Rank K
μPD703134AY: Rank K
μPD703136A: Rank K
μPD703136AY: Rank K
μPD70F3134A: Ranks K, E
μPD70F3134AY: Ranks K, E
μPD703131BY: Rank K
μPD703132BY: Rank K
μPD703133BY: Rank K
μPD703134BY: Rank K
μPD703136BY: Rank K
μPD70F3134BY: Rank K

* The rank is indicated by the letter appearing as the 5th digit from the left in the lot number marked on each product.

2. Product History

- μPD703131A, μPD703131AY, μPD703132A, μPD703132AY, μPD703133A, μPD703133AY, μPD703134A, μPD703134AY, μPD703136A, μPD703136AY

No.	Bugs	Rank
		K
1	Restriction on sequence for turning on/off power	Δ
2	Restriction on flash memory programming	√

√: Bug does not occur, Δ: Bug will also apply in future, ×: Bug occurs

- μPD70F3134A, μPD70F3134AY

No.	Bugs	Rank	
		K	E
1	Restriction on sequence for turning on/off power	Δ	Δ
2	Restriction on flash memory programming	×	√

√: Bug does not occur, Δ: Bug will also apply in future, ×: Bug occurs

- μPD703131BY, μPD703132BY, μPD703133BY, μPD703134BY, μPD703136BY, μPD70F3134BY

No.	Bugs	Rank
		K
1	Restriction on sequence for turning on/off power	Δ
2	Restriction on flash memory programming	√

√: Bug does not occur, Δ: Bug will also apply in future, ×: Bug occurs

3. Details of Usage Restrictions

No. 1 Restriction on sequence for turning on/off power

[Description]

When turning on/off the power, if the voltage on the internal power supply pin (V_{DD}) exceeds the operation guaranteed range (2.3 to 2.7 V) while the voltage has been applied to the external power supply pins (EV_{DD}, CV_{DD}, AV_{DD0} and AV_{DD1}), the following operations may occur.

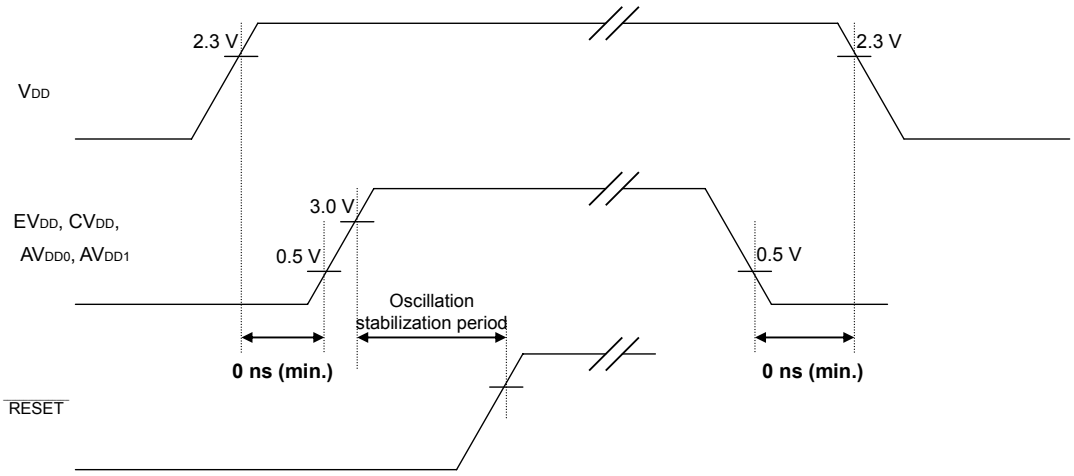
- A current of approximately 130 mA (typ.) may flow into the EV_{DD} pin.
- An undefined value may be output from the following pins.
  TDO/$\overline{TC3}$/P27 pin
  ANO0/P80 pin
  ANO1/P81 pin

To avoid this bug, it is recommended to turn on or off the power in the procedure shown below.

[Recommended procedure]

<When turning on power>

Keep the voltage on the EV_{DD}, CV_{DD}, AV_{DD0}, and AV_{DD1} pins at 0.5 V or lower until the voltage on the V_{DD} pin reaches the operation guaranteed range (2.3 to 2.7 V).

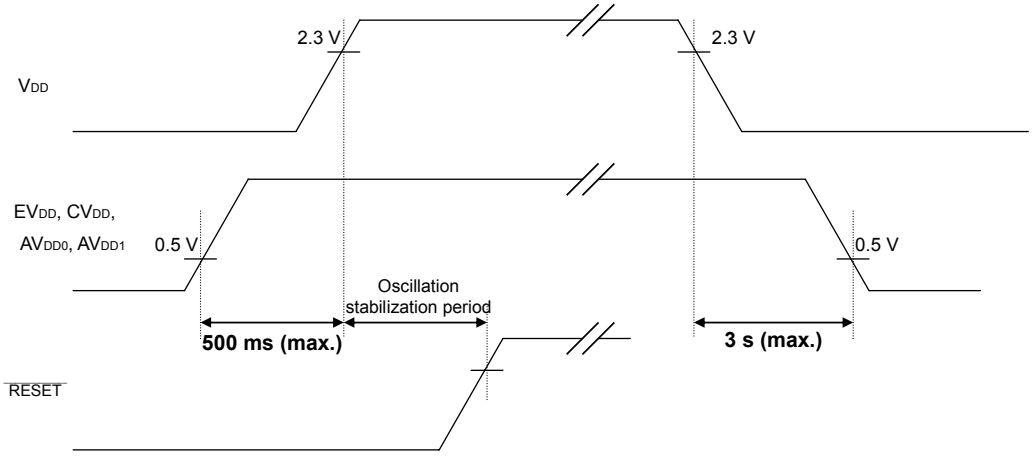


<When turning off power>

Keep the voltage on the V_{DD} pin to within the operation guaranteed range (2.3 to 2.7 V) until the voltage on the EV_{DD}, CV_{DD}, AV_{DD0}, and AV_{DD1} pins drops to 0.5 V or lower.

[Caution]

Also observe the timing shown below when turning on/off the power to the external power supply pins (EV_{DD}, CV_{DD}, AV_{DD0} and AV_{DD1}) before turning on/off the power to the internal power supply pin (V_{DD}).



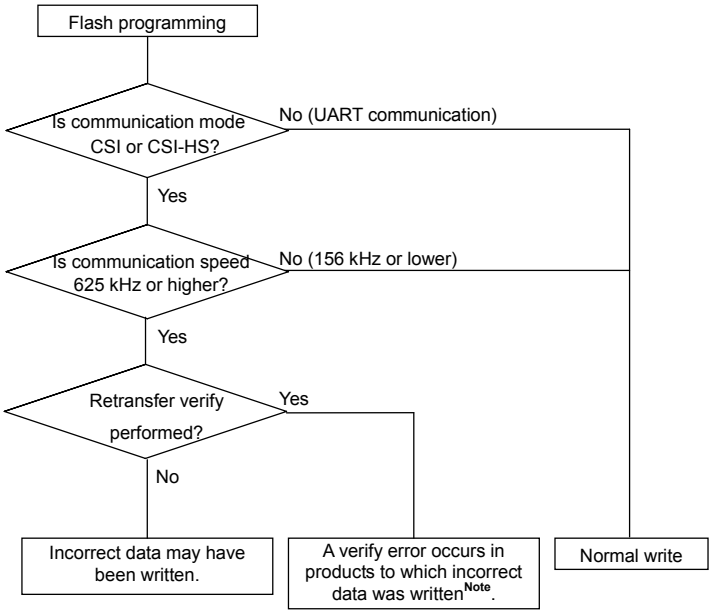
No. 2 Restriction on flash memory programming

[Description]

When programming to flash memory is performed using flash programmer PG-FP4, unexpected data may be written. If verify (set by selecting “Read verify after Program” in the PG-FP4 setting screen) is not executed, operation ends without causing an error even if unexpected data is written, so erroneous programming cannot be detected. If verify is executed, a verify error occurs and thus erroneous programming can be detected.

[Conditions under which this bug occurs]

Erroneous programming may occur if PG-FP4 communication is performed in CSI or CSI-HS mode, with a 625 kHz or higher communication speed.



Note If the PG-FP4 is set so as to perform verify, erroneous programming is detected as a verify error. If verify is performed and programming to the target device is completed normally, the written data is normal.

Remark This condition does not apply to self-programming.

[Temporary workarounds]

1. Products with a lot number earlier than 0610Kxxxx[Note]

Perform flash programming under one of the following conditions. Execution of verify is recommended even if condition (1) or (2) is satisfied.

(1) Use UART communication mode.

(2) If CSI or CSI-HS communication mode is used, set the communication speed to 156 kHz or lower.

(3) Set the PG-FP4 so as to perform verify (regardless of communication mode and speed). For devices in which a verify error is detected, perform programming with condition (1) or (2) satisfied.

2. Products with a lot number 0611Kxxxx[Note] or later

Perform flash programming under one of the following conditions. Execution of verify is recommended even if condition (1), (2) or (3) is satisfied.

(1) Use UART communication mode.

(2) If CSI communication mode is used, set the communication speed to 625 kHz or lower.
If CSI-HS communication mode is used, set the communication speed to 156 kHz or lower.

(3) If CSI communication mode is used and the communication speed is set to 2,500 kHz, keep the programming environment temperature within 0 to +70°C.

(4) Set the PG-FP4 so as to perform verify (regardless of communication mode and speed). For devices in which a verify error is detected, perform programming with condition (1), (2) or (3) satisfied.

Note In lot numbers, “06” indicates the year of manufacture, while 10 and 11 indicate the week of manufacture.

[Permanent workaround]

Flash programming firmware incorporated in devices will be modified. This restriction will then be removed through a running change from the current products (rank K[Note]) to the modified products (rank E[Note]), starting from November 2006 (planned). In conjunction with firmware modification, the parameter file for the flash programmer will be upgraded (planned in November 2006). The current parameter file (V1.10) cannot be used for programming with products after the upgrade, so be sure to use the new parameter file (V1.20 or later).

* The rank is indicated by the letter appearing as the 5th digit from the left in the lot number marked on each product.

Parameter File Version	Rank K	Rank E
V1.10	O[Note]	x
V1.20	O[Note]	O

O: Usable for programming, x: Unusable for programming

Note Implement the temporary workaround.

[Other]

Contact an NEC Electronics sales representative when using a flash programmer other than the PG-FP4.

[Verify setting]

To enable verify, select the “Read verify after Program” check box on the PG-FP4 GUI software screen. Refer to the PG-FP4 user’s manual for details.