Microcomputer Technical Information

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32-Bit Microcontroller V850E/MA3 Usage Restrictions		Document No.	ZBG-CC-05-0011		1/1
		Date issued	January 17, 2005		
		Issued by	Microcomputer Group Multipurpose Microcomputer Systems Division 4th Systems Operations Unit NEC Electronics Corporation		
Related documents	V850E/MA3 Hardware User's Manual: U16397EJ V850E1 Architecture User's Manual: U14559EJ	Notification classification	√	Usage restriction	
				Upgrade	
				Document modification	
				Other notification	

1. Affected products

V850E/MA3

- μPD703131A, μPD703131AY (ROM: 256 KB/RAM: 16 KB)
- μPD703132A, μPD703132AY (ROM: 256 KB/RAM: 32 KB)
- μPD703133A, μPD703133AY (ROM: 512 KB/RAM: 16 KB)
- μPD703134A, μPD703134AY (ROM: 512 KB/RAM: 32 KB)
- μPD70F3134A, μPD70F3134AY (Flash memory: 512 KB/RAM: 32 KB)

Remark For restrictions on non-A products (μPD703131, μPD703132, μPD703133, μPD703134, μPD70F3134, and μPD70F3134Y), individually contact an NEC Electronics sales representative or distributor.

2. New restriction

This notification concerns the following restriction (No. 1). See the attachment for details.

- No. 1 Restriction on sequence for turning on/off power

3. Action

This restriction is not planned for modification. Please regard this item as a usage restriction.

4. List of restrictions

The restriction history and detailed information is described in the attachment.

5. Document revision history

32-Bit Microcontroller V850E/MA3 Usage Restrictions

Document Number	Date Issued	Description
ZBG-CC-05-0011	January 17, 2005	Newly created. Addition of restriction No. 1.

List of Usage Restrictions in V850E/MA3

1. Product Version

μPD703131A: Rank K
μPD703131AY: Rank K
μPD703132A: Rank K
μPD703132AY: Rank K
μPD703133A: Rank K
μPD703133AY: Rank K
μPD703134A: Rank K
μPD703134AY: Rank K
μPD70F3134A: Rank K
μPD70F3134AY: Rank K

* The rank is indicated by the letter appearing as the 5th digit from the left in the lot number marked on each product.

2. Product History

- μPD703131A, μPD703131AY, μPD703132A, μPD703132AY, μPD703133A, μPD703133AY, μPD703134A, μPD703134AY

No.	Bugs	Rank
		K
1	Restriction on sequence for turning on/off power	Δ

√: Bug does not occur, Δ: Bug will also apply in future, ×: Bug occurs

- μPD70F3134A, μPD70F3134AY

No.	Bugs	Rank
		K
1	Restriction on sequence for turning on/off power	Δ

√: Bug does not occur, Δ: Bug will also apply in future, ×: Bug occurs

3. Details of Usage Restrictions

No. 1 Restriction on sequence for turning on/off power

[Description]

When turning on/off the power, if the voltage on the internal power supply pin (V_{DD}) exceeds the operation guaranteed range (2.3 to 2.7 V) while the voltage has been applied to the external power supply pins (EV_{DD}, CV_{DD}, AV_{DD0}, and AV_{DD1}), the following operations may occur.

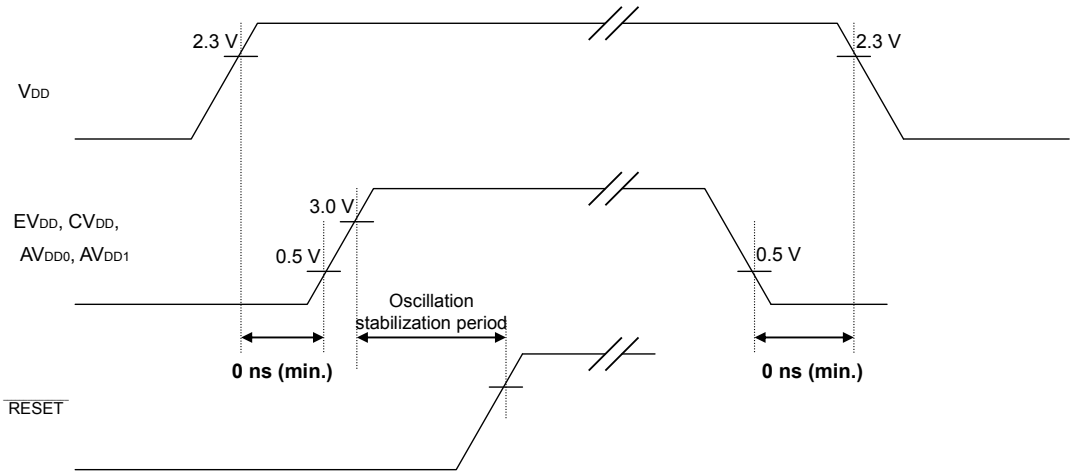
- A current of approximately 130 mA (typ.) may flow into the EV_{DD} pin.
- An undefined value may be output from the following pins.
  TDO/$\overline{\text{TC3}}$/P27 pin
  ANO0/P80 pin
  ANO1/P81 pin

To avoid this bug, it is recommended to turn on or off the power in the procedure shown below.

[Recommended procedure]

<When turning on power>

Keep the voltage on the EV_{DD}, CV_{DD}, AV_{DD0}, and AV_{DD1} pins at 0.5 V or lower until the voltage on the V_{DD} pin reaches the operation guaranteed range (2.3 to 2.7 V).



<When turning off power>

Keep the voltage on the V_{DD} pin to within the operation guaranteed range (2.3 to 2.7 V) until the voltage on the EV_{DD}, CV_{DD}, AV_{DD0}, and AV_{DD1} pins drops to 0.5 V or lower.

[Caution]

Also observe the timing shown below when turning on/off the power to the external power supply pins (EV_{DD}, CV_{DD}, AV_{DD0}, and AV_{DD1}) before turning on/off the power to the internal power supply pin (V_{DD}).