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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0154A/E	Rev.	1.00
Title	Restriction for A-Format, and addition / change for electrical characteristics		Information Category	Technical Notification		
Applicable Product	RZ/T2M Group, RZ/T2ME Group, RZ/T2L Group, RZ/N2L Group	Lot No. All	Reference Document	RZ/T2M Group User's Manual: Hardware Rev.1.20 (R01UH0916EJ0120), RZ/T2ME Group User's Manual: Hardware Rev.1.00 (R01UH1062EJ0100), RZ/T2L Group User's Manual: Hardware Rev.1.20 (R01UH0985EJ0120), RZ/N2L Group User's Manual: Hardware Rev.1.30 (R01UH0955EJ0130)		

This document informs a restriction for A-Format on RZ/T2L, and addition / change for electrical characteristics of RZ/T2M, RZ/T2ME, RZ/T2L and RZ/N2L. These are reflected in revised User's Manual: Hardware.

[Revised User's Manual: Hardware]

- RZ/T2M Group User's Manual: Hardware Rev.1.30 (R01UH0916EJ0130)
- RZ/T2ME Group User's Manual: Hardware Rev.1.10 (R01UH1062EJ0110)
- RZ/T2L Group User's Manual: Hardware Rev.1.30 (R01UH0985EJ0130)
- RZ/N2L Group User's Manual: Hardware Rev.1.40 (R01UH0955EJ0140)

1. A-Format (AFMT)

Applicable product：RZ/T2L Group products

Restriction
Supported protocol version is Ver.2.0 only. Ver.1.x is not supported because serial data transmission timing was changed.

2. Electrical Characteristics

Items in red are added or changed.

2.1 Ethernet PHY Reference Clock Output Timing

Applicable product: Products of RZ/T2M Group, RZ/T2ME Group, RZ/T2L Group, and RZ/N2L Group

Table 45.16 Ethernet PHY reference clock output timing (RZ/T2M Group, RZ/T2ME Group)

Table 52.16 Ethernet PHY reference clock output timing (RZ/T2L Group)

Table 48.16 Ethernet PHY reference clock output timing (RZ/N2L Group)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
ETHn_REFCLK cycle time	t_{CK}	—	40	—	—	ns
ETHn_REFCLK frequency	—	—	25.00 ± 50 ppm			MHz
		EtherCAT in use	25.00 ± 25 ppm			MHz
ETHn_REFCLK duty	—	—	45	—	55	%
ETHn_REFCLK rising / falling time	t_{CKr} / t_{CKf}	—	0.5	—	4.0	ns
RMIIn_REFCLK cycle time	t_{CK}	—	20	—	—	ns
RMIIn_REFCLK frequency	—	—	50.00 ± 50 ppm			MHz
RMIIn_REFCLK duty	—	—	45	—	55	%
RMIIn_REFCLK rising / falling time	t_{CKr} / t_{CKf}	—	0.5	—	3.5	ns

2.2 SCI Timing

Applicable products: Products of RZ/T2M Group, RZ/T2ME Group, RZ/T2L Group, and RZ/N2L Group

Table 45.32 SCI timing (RZ/T2M Group, RZ/T2ME Group)

Table 52.32 SCI timing (RZ/T2L Group)

Table 48.32 SCI timing (RZ/N2L Group)

Parameter			Symbol	Min.	Max.	Unit	Reference figure
SCI (Ckock sync, Simple SPI)	SCK output clock cycle (master)		t_{SPcyc}	2	65536	$t_{PSCIcyc}$	Figure xx.57 to Figure xx.62
	SCK input clock cycle (slave)			2	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKR}、t_{SPCKF}	—	3	ns	
	Data input setup time	Internal clock	t_{SU}	7	—	ns	
		External clock		3	—		
	Data input hold time	Internal clock	t_{H}	3	—	ns	
		External clock		3	—		
	Data output delay time	Internal clock	t_{OD}	—	3	ns	
		External clock		—	12		
	Data output hold time	Internal clock	t_{OH}	-3	—	ns	
		External clock		0	—		
	Data rise/fall time		t_{DR}、t_{DF}	—	3	ns	
	Slave access time	Internal clock	t_{SA}	—	3 × $t_{PSCIcyc}$ + 12	ns	
		External clock		—	3 × $t_{PSCIcyc}$ + 12		
	Slave output release time	Internal clock	t_{REL}	—	3 × $t_{PSCIcyc}$ + 12	ns	
		External clock		—	3 × $t_{PSCIcyc}$ + 12		
SCI (Simple SPI)	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	SS input rise/fall time		t_{SSR}、t_{SSF}	—	3	ns	

2.3 xSPI Timing

Applicable products: Products of RZ/T2M Group, RZ/T2ME Group, RZ/T2L Group, and RZ/N2L Group

Table 45.36 xSPI timing (RZ/T2M Group, RZ/T2ME Group)

Table 52.36 xSPI timing (RZ/T2L Group)

Table 48.36 xSPI timing (RZ/N2L Group)

Parameter		Symbol	1.8 V		3.3 V		Unit	Reference figure
			Min.	Max.	Min.	Max.		
Cycle time	SDR	t_{PERIOD}	7.5	—	13.3	—	ns	Figure xx.73
	DDR		10.0	—	13.3	—	ns	
Clock output slew rate		t_{SRck}	0.75/0.56 *2	—	0.56	—	V/ns	
Clock duty cycle distortion		t_{CKDCD}	0.0	t_{PERIOD} × 0.05	0.0	t_{PERIOD} × 0.05	ns	
Clock minimum pulse width		t_{CKMPW}	t_{PERIOD} × 0.45	—	t_{PERIOD} × 0.45	—	ns	
Differential clock crossing voltage		$V_{OX(AC)}$	0.4 × VCC18	0.6 × VCC18	—	—	V	
DS duty cycle distortion		t_{DSDCD}	0.0	t_{PERIOD} × 0.04	0.0	t_{PERIOD} × 0.04	ns	
DS minimum pulse width		t_{DSMPW}	t_{PERIOD} × 0.41	—	t_{PERIOD} × 0.41	—	ns	
Data input/output slew rate		t_{SR}	0.75/0.56 *2	—	0.56	—	V/ns	
Data input setup time (to CK)	SDR	t_{SU}	2.0	—	2.0	—	ns	Figure xx.74
Data input hold time (to CK)		t_{H}	1.0	—	1.0	—	ns	
Data output delay time		t_{OD}	—	1.0 *3	—	2.0 *3	ns	
Data output hold time		t_{OH}	-1.0	—	-2.0	—	ns	
Data output buffer off time		t_{BOFF}	-1.0	—	-2.0	—	ns	
Data input setup time (to DS)	DDR *1 *3	t_{SU}	-0.8	—	-0.8	—	ns	Figure xx.75, Figure xx.76
Data input hold time (to DS)		t^{H}	t_{PERIOD} × 0.41 - 0.8	—	t_{PERIOD} × 0.41 - 0.8	—	ns	
Data output setup time (to CK)		t_{SUO}	1.0	—	1.0	—	ns	
Data output hold time (to CK)		t_{HO}	1.0	—	1.0	—	ns	
CS low to clock high		t_{CSLCKH}	6.0/8.0 *2 *4	—	8.0 *4	—	ns	Figure xx.74 to Figure xx.76
Clock low to CS high		t_{CKLCSH}	6.0/8.0 *2	—	8.0	—	ns	
CS high time		t_{CSTD}	1	16	1	16	t_{PERIOD}	
DS low to CS high		t_{DSLCSH}	6.0/8.0 *2 *5	—	10.6 *5	—	ns	Figure xx.77
CS high to DS tri-state		t_{CSHDST}	0.0	t_{PERIOD}	0.0	t_{PERIOD}	ns	
CS low to DS low *8		t_{CSLDSL}	0.0	16.0 *9	0.0	20.0 *9	ns	
DS tri-state to CS low		t_{DSTCSL}	0.0	—	0.0	—	ns	
CK low to DS low *6		t_{CKLDSL}	—	(0.45 + e) × t_{PERIOD} – 2 *7	—	(0.45 + e) × t_{PERIOD} – 2 *7	ns	

Note 1. The DS shift setting (WRAPCFG.DSSFTCSx[4:0]) is 01000b for xSPI200.

Note 2. Specification at 133 MHz / Specification at 100 MHz

Note 3. These are values when the OEN assertion is extended in the Output Enable Asserting extension bit (COMCFG.OEASTEX = 1).

Note 4. These are the values when the CS assertion is extended in the CS asserting extension bit (LIOCFGCSn.CSASTEX = 1).

Note 5. There are the values when the t_{CKLDSL} constraint is satisfied.

Note 6. This constraint is necessary only to satisfy the t_{DSLCSH} requirement in JESD251, which specifies that t_{DSLCSH} must be at least 80% of tPERIOD. Set LIOCFGCSn.CSNEGEX to the appropriate value to ensure the memory specification complies with this constraint.

Note 7. e = LIOCFGCSn.CSNEGEX

Note 8. If the DS is high during the command and modifier phase when using JESD251 Profile 2.0 memory, the time from CS low to DS high must also meet this specification.

Note 9. When using JESD251 Profile 1.0 memory or JESD251 Profile 2.0 memory with LIOCFGCSn.LATEMD set to 0, this constraint does not apply if the internal pull-down resistor of the DS pin is enabled.

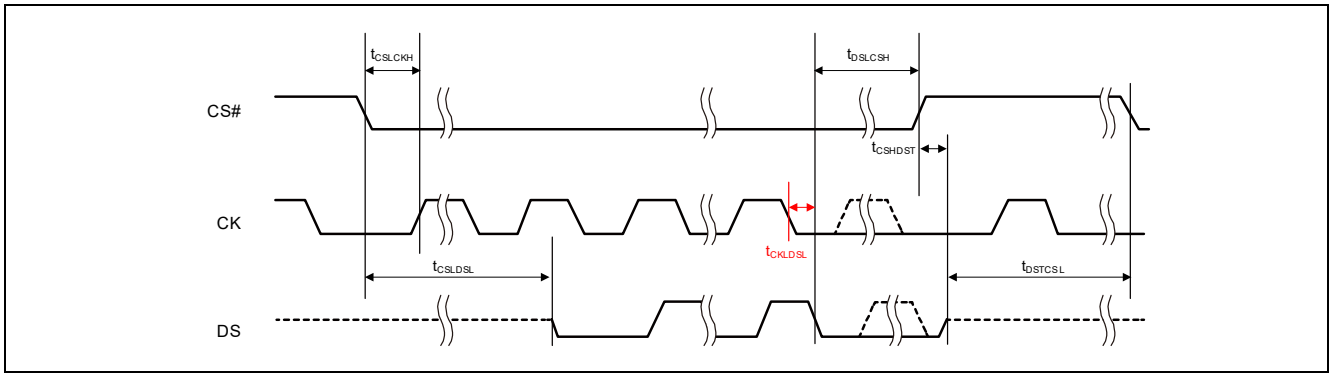

Figure xx.77 DS to CS signal timing

2.4 Ethernet Interface Timing

Applicable product: Products of RZ/T2M Group, and RZ/T2ME Group

Table 45.38 Ethernet interface timing

Parameter			Symbol	Min.	Max.	Unit	Reference figure
Ethernet (RGMII)	ETHn_TXCLK, ETHn_RXCLK cycle time duration	1 Gbps	$t_{RGMIIck}$	7.2	8.8	ns	Figure 45.81
		100 Mbps		36	44		
		10 Mbps		360	440		
	ETHn_TXCLK, ETHn_RXCLK frequency	1 Gbps	—	125 - 50 ppm	125 + 50 ppm	MHz	
		100 Mbps		25 - 50 ppm	25 + 50 ppm		
		10 Mbps		2.5 - 50 ppm	2.5 + 50 ppm		
	ETHn_TXCLK, ETHn_RXCLK duty cycle	1 Gbps	—	45	55	%	
		100 Mbps 10 Mbps		40	60		
	ETHn_TXCLK, ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN (TX_CTL), ETHn_RXCLK, ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) rise/fall time		t_{RGMIIr}, t_{RGMIIf} +[1]	—	0.75	ns	
	ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN (TX_CTL) to ETHn_TXCLK output skew		$t_{RGMIIos}$	-0.5	0.5	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) setup time		t_{RGMIIs}	1	—	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) hold time		t_{RGMIIh}	1	—	ns	
Ethernet (RMII)	ETHn_RXCLK cycle time		t_{RMIIck}	20	—	ns	Figure 45.82, Figure 45.83
	ETHn_RXCLK frequency Typ. 50 MHz		—	50 - 50 ppm	50 + 50 ppm	MHz	
	ETHn_RXCLK duty		—	35	65	%	
	ETHn_RXCLK rise/fall time		$t_{RMIIckr}$, tRMIIckf	0.5	3.5	ns	
	ETHn_TXD0, ETHn_TXD1, ETHn_TXEN output delay time		t_{RMIId}	2.5	12	ns	
	ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) setup time	**Case A *2**	**t_{RMIIs}**	**4.0**	**—**	**ns**	
		Case B *2		**4.0**	**—**	**ns**	
		Case C *2		**4.8**	**—**	**ns**	
	ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) hold time		t_{RMIIh}	2	—	ns	

	ETHn_TXD0, ETHn_TXD1, ETHn_TXEN, ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) rise/fall time		t_{RMIIr}, t_{RMIIf}	0.5	4	ns	
Ethernet (MII)	ETHn_TXCLK, ETHn_RXCLK cycle time	100 Mbps	t_{MIIck}	40	—	ns	Figure 45.84, Figure 45.85
		10 Mbps		400	—		
	ETHn_TXCLK, ETHn_RXCLK frequency	100 Mbps	—	25 - 50 ppm	25 + 50 ppm	MHz	
		10 Mbps		2.5 - 50 ppm	2.5 + 50 ppm		
	ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN, ETHn_TXER output delay time		$t_{MIIdESC}$	1	20	ns	
	ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN output delay time (ESC, Automatic TX shift disabled (ETHn_TXCLK is clamped))	**TXSFTn = 00b**	**$t_{MIIdESC}$**	**20.2**	**25.0**	**ns**	
		TXSFTn = 01b		**30.2**	**35.0**	**ns**	
		TXSFTn = 10b		**0.2**	**5.0**	**ns**	
		TXSFTn = 11b		**10.2**	**15.0**	**ns**	
	ETHn_RXD0 ~ ETHn_RXD3、ETHn_RXDV、ETHn_RXER setup time		t_{MIIs}	10	—	ns	
	ETHn_RXD0 ~ ETHn_RXD3、ETHn_RXDV、ETHn_RXER hold time		t_{MIIh}	10	—	ns	

Note 1. Measurement condition of tRGMIIr and tRGMIIf is FIGURE 3 in Reduced Gigabit Media Independent Interface (RGMII) 12/10/2000 Version 1.3.

Note 2. Details for each case are as follows:

Case A: ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) setup time when using ETHn_RXCLK (Reference clock input)

Case B: ETHn_RXD0, ETHn_RXD1, ETHn_RXDV (CRS_DV) setup time when using RMIIn_REFCLK (Reference clock output)

Case C: ETHn_RXER setup time when using RMIIn_REFCLK (Reference clock output)

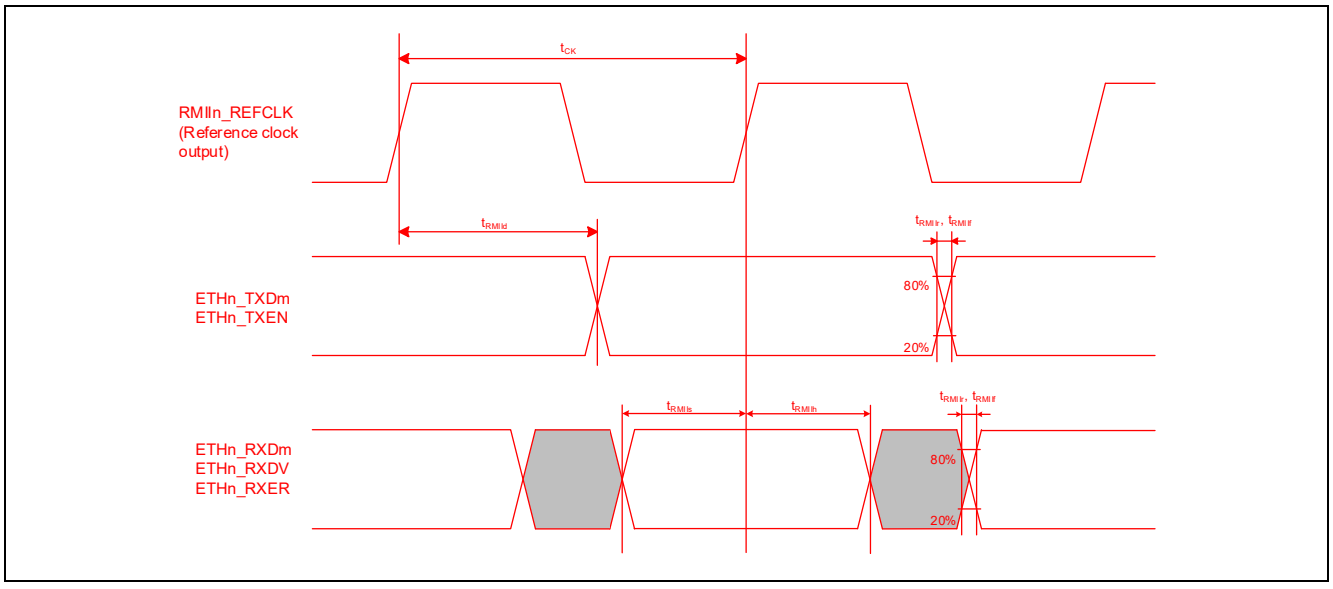

Figure 45.83 RMII transmission and reception timing (Reference clock output) (n = 0 to 2, m = 0 to 1)

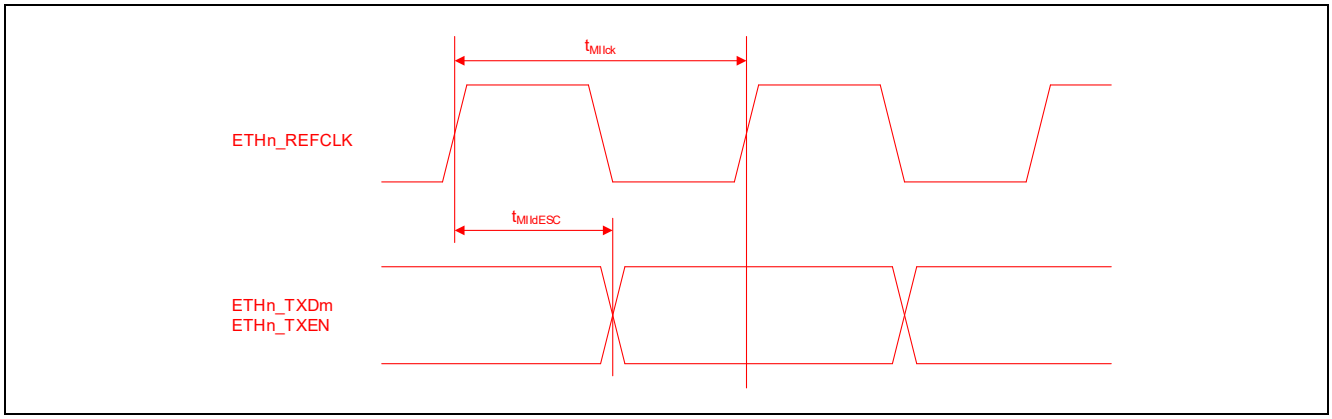

Figure 45.85 ESC MII transmission timing (Automatic TX shift disabled) (n = 0 to 2, m = 0 to 3)