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1 SSOP14 Package

The ZSC31150 is available assembled in a SSOP14 (sales codes ZSC31150**G1-*) RoHS-compliant package (5.3mm body) with a lead-pitch of 0.65mm.

Package R_{th}: ~120W/K **Weight:** ≤ 0.3 g

Package Body Material: Low-Stress Epoxy

Lead Material: FeNi-Alloy or Cu-Alloy **Lead Finish:** Solder Plating **Lead Form:** Z-Bends

1.1. SSOP14 Package Dimensions

Figure 1.1 Package View

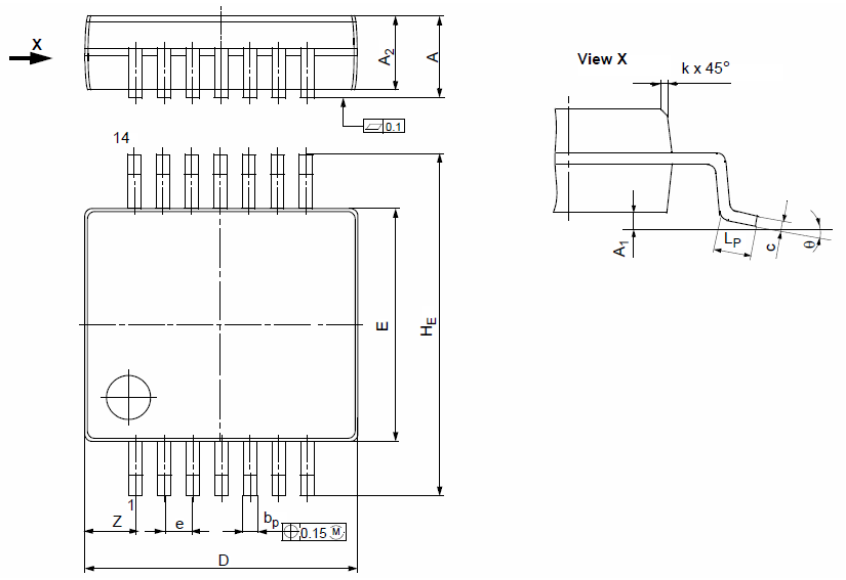


Table 1.1 Package Dimension

Package Dimensions					
Dimension	**Value**	**Dimension**	**Value**	**Dimension**	**Value**
A_{max}	1.99mm	c_{min}	0.09mm	H_{Emin}	7.65mm
A_{min}	1.73mm	c_{max}	0.20mm	H_{Emax}	7.90mm
$A1_{min}$	0.05mm	D_{min}*	6.07mm	k_{min}	0.25mm
$A1_{max}$	0.21mm	D_{max}*	6.33mm	LP_{min}	0.63mm
$A2_{min}$	1.68mm	E_{min}*	5.20mm	Z_{max}	1.22mm
$A2_{max}$	1.78mm	E_{max}*	5.38mm	θ_{min}	0°
b_{Pmin}	0.25mm	e_{nom}	0.65mm	θ_{max}	10°
b_{Pmax}	0.38mm	* without mold-flash			

1.2. SSOP14 Package Marking and Pin Assignments

Table 1.2 SSOP14 Package Marking

Top Side		Comments
1st Line	ZSC	
2nd Line	31150%$G1	% = Revision Identifier; $ = Temperature Range Identifier; example: ZSC31150AAG1
3rd Line	XXXXXXXX	Production Lot Number
4th Line	YYWW	Package Assembly Date: YEAR,YEAR,WEEK,WEEK

Table 1.3 Pin Assignments

Pin	Name	Description	Notes	Usage/ Connection [1)]	Latch-up Related Application Circuit Restrictions and/or Notes
1	VDDA	Positive analog supply voltage	Analog IO	Required/N.A.	
2	VSSA	Negative analog supply voltage	Analog IO	Required/N.A.	
3	SDA	I²C™* data IO	Digital IO, pull-up	N.A./VDDA	Trigger current/voltage to VDDA/VSSA: +/-100mA or 8/-4V
4	SCL	I²C™ clock	Digital IN, pull-up	N.A./VDDA	
5	N.C.	No connection			
6	VDD	Positive digital supply voltage	Analog IO	Required or open/N.A.	Only capacitor to VSSA is allowed; otherwise no application access
7	VDDE	Positive external supply voltage	Supply	Required/N.A.	Trigger current/voltage: -100mA/33V
8	VSSE	Negative external supply voltage	Ground	Required/N.A.	
9	AOUT	Analog output and one-wire Interface I/O	IO	Required/N.A.	Trigger Current/Voltage: -100mA/33V
10	VBN	Negative input sensor bridge	Analog IN	Required/N.A.	
11	VBR_B	Bridge bottom potential	Analog IO	Required/VSSA	Depending on application circuit, short to VDDA/VSSA possible
12	VBP	Positive input sensor bridge	Analog IN	Required/N.A.	
13	VBR_T	Bridge top potential	Analog IO	Required/VDDA	
14	IRTEMP	Temperature sensor and current source resistor	Analog IO	N.A./VDDA, VSSA	Depending on application circuit

1) **Usage**: If “Required” is specified, an electrical connection is necessary.
Connection: To be connected to this potential if not used or if no application/configuration-related constraints are given.
N.A.: Not applicable.

* I²C™ is a trademark of NXP>

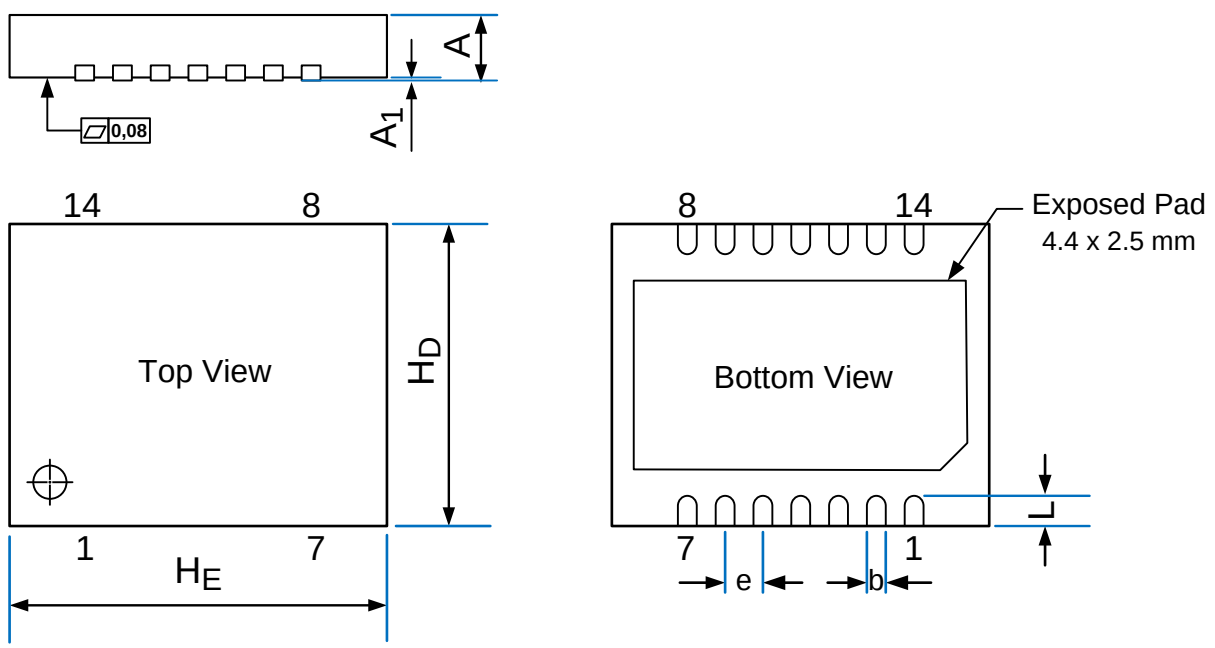
2 DFN14 Package

The ZSC31150 is also available assembled in a DFN14 package (sales codes ZSC31150**G2-*) with wettable flanks. For this package option, the pin assignments are the same as for the SSOP14 option.

2.1. DFN14 Package Dimensions

Figure 5.2 provides the dimensions for the DFN14 package option, which are based on JEDEC MO-229.

Figure 2.1 Outline Drawing for DFN14 Package with Wettable Flanks



Dimension	Minimum (mm)	Maximum (mm)
A	0.8	0.9
A_1	0	0.05
b	0.2	0.3
e	0.5 nominal	
H_D	3.9	4.1
H_E	4.9	5.1
L	0.3	0.5

2.2. Footprint and Wettable Flank Description

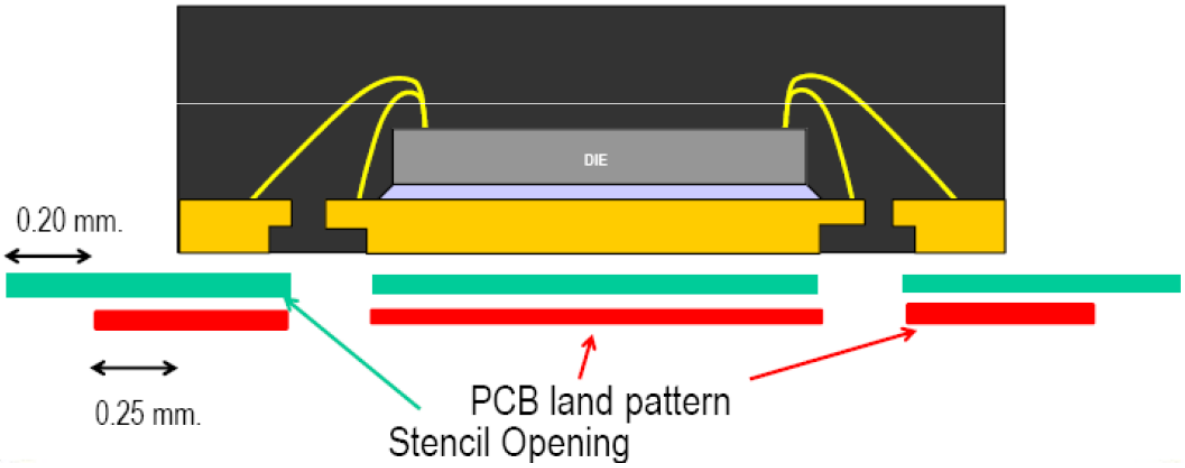
Figure 2.2 illustrates the general concept of the wettable flank (side plating), which allows automatic optical inspection when using the DFN14 package option.

Figure 2.2 Wettable Flank General Concept

Figure 2.3 illustrates a suggested footprint for printed circuit board (PCB) designs using the ZSC31150 DFN14.

- The exposed area of the ZSC31150 landing pattern is 0.25mm for the unit edge.
- The stencil opening excess is about 0.2mm from the landing pattern.

Figure 2.3 Footprint Dimensions for DFN14 with Wettable Flanks



2.3. DFN14 Package Marking

Table 2.1 DFN14 Package Marking

Top Side		Comments
1st Line	31150	
2nd Line	%$YWW	% = Revision Identifier; $ = Temperature Range Identifier; Y = Year (e.g., 4 for 2014, 5 for 2015, ...); WW = Workweek (e.g., 15)
3rd Line	XXXXX	Last five digits of IDT lot number

3 Pin Short-Circuit Information

Table 3.1 Pin Short-Circuit Description

Pin#	Name	Short to Pin	Behavior/Comment
1	VDDA	VSSA	Internal supply voltage is shorted with short current depending on the short resistance; abortion of signal conditioning functions if the reset threshold is reached by the resulting VDDA-VSSA potential. AOUT is switched to a high impedance condition (tri-state) in this case. Resulting alternating behavior of power on and off is possible.
2	VSSA	SDA	***No I²C™* communication:*** Current flow via the internal pull-up resistor (50kΩ). No effect on signal conditioning functions. ***I²C™ communication***: Communication abortion depending on short resistance. No internal current limitation.
3	SDA	SCL	***No I²C™ communication:*** Current flow via the internal pull-up resistor (50kΩ). No effect on signal conditioning function. ***I²C™ communication***: Communication abortion depending on short resistance. No internal current limitation.
4	SCL	n.c.	No effect on signal conditioning functions.
5	n.c.	VDD	No effect on signal conditioning functions.
6	VDD	VDDE	No effect on signal conditioning functions; protection function (overvoltage and reverse polarity) does not operate.
7	VDDE	VSSE	Abortion of signal conditioning functions if reset threshold is reached by resulting VDDA-VSSA potential. AOUT is switched to a high impedance condition (tri-state) in this case.

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Pin#	Name	Short to Pin	Behavior/Comment
8	VSSE	AOUT	AOUT current is limited to 20mA maximum. After activating the current limitation, the AOUT signal measured by the ECU is incorrect.
9	AOUT	VBN	The AOUT signal measured by the ECU is incorrect. Depending on short resistance, these failures can be detected in most cases by the built-in failsafe tasks SSC, SCC, and CMV (see section 7).
10	VBN	VBR_B	
11	VBR_B	VBP	
12	VBP	VBR_T	
13	VBR_T	IRTEMP	Wrong temperature measurement. Depending on the short resistance, failure can be detected by the built-in temperature sensor (TS) check failsafe task.
14	IRTEMP	VDDA	

4 Temperature Profile

ZSC31150*EG* and ZSC31150*AG* are qualified according to the AEC-Q100 automotive reliability standard.

ZSC31150*EG* is qualified to AEC-Q100 grade 0, which has a summed temperature stress rating of 1000h at 150°C.

ZSC31150*LG* is qualified according to AEC-Q100 grade 0 with an extended temperature stress of 5000h at 150°C.

ZSC31150*AG* is qualified for the same summed temperature stress, but the maximum temperature in applications is limited to 125°C (AEC-Q100 grade 1).

An actual temperature profile for an application can be checked by using the Arrhenius equation with a given temperature stress level of 1000h at 150°C or 5000h at 150°C. For these calculations, use an activation energy of 0.7eV.

Refer to calculation sheet *ZMDI Temperature Profile Calculation Sheet* for details.

5 Storage Conditions

For detailed information about storage conditions requirements, refer to the document *IDT Storage Conditions*. This document is included in all deliveries of packaged parts. It is also available upon request.

6 Related Documents

Document
ZSC31150 Feature Sheet
ZSC31150 Data Sheet
IDT Temperature Profile Calculation Sheet
*ZSC31150 Technical Note – Die and Pad Dimensions**
IDT Wafer Dicing Guidelines

Visit the ZSC31150 product page (www.IDT.com/ZSC31150) or contact your nearest sales office for the latest version of these documents.

* Note: Documents marked with an asterisk (*) are available upon request.

7 Glossary

Term	Description
AEC	Automotive Electronics Council
CMV	Common Mode Voltage Check
SCC	Sensor Connection Check
SSC	Sensor Signal Conditioner or Sensor Short Check, depending on context

8 Document Revision History

Revision	Date	Description
1.01	August 3, 2008	First revision of document.
1.02	November 29, 2010	Section for “Traceability” added. ZMD31151 removed. Changed to new IDT naming conventions and template.
1.03	August 16, 2011	Temperature profile for ZSC31150*LG1 (refer to section 4).
1.04	December 19, 2012	Update for package marking definitions. Minor edits and update for contact information.
1.05	January 28, 2013	Minor edits to illustrations for clarity.
1.06	February 11, 2014	Added wafer drawing and defined scribe line. Update for cover imagery and contact information.
1.07	April 6, 2014	DFN14 package and pin assignment added; temperature profile grades assigned according to the products. Corrections for pad names. Minor edits to “Related Documents” section.
1.10	April 29, 2014	Wettable flanks concept and PCB design recommendations added.
1.20	October 7, 2014	Temperature profile grades added for DFN packages. Minor edits for clarity. Updates for contact information.
1.30	November 24, 2015	Split revision 1.20 into separate documents for die (on-request only) and for SSOP14/DFN14 package specifications. Update for contact information.
	April 26, 2016	Changed to IDT branding.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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