Packaging Information

Surface Mount Assembly Guidelines for Optical Dual Flat Pack No Lead (ODFN) Package

Abstract

Optical Dual-in-line Flat No-lead (ODFN) packages are developed for light sensor applications. The ODFN mechanical structure is similar to that of a conventional DFN, except the molding compound is a transparent material rather than the conventional black compound. Transparent molding compound allows transmission of ambient light through the molding compound to reach the die sensor area. This package is lead-free, with pre-plated Nickel-Palladium-Gold (NiPdAu) finish on the terminals. Figure 1 shows a 6 Ld ODFN. As the image shows, the package finish is transparent to allow light transmission and at the same time, protects the device from the environment.

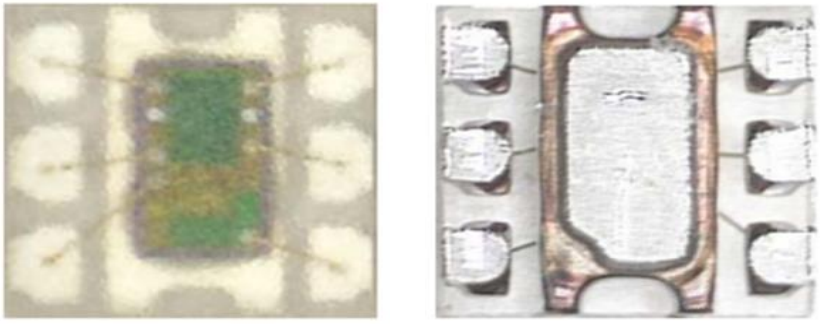

Figure 1. 6 Ld ODFN Top View (Left) and Bottom View (Right)

This package follows conventional DFN/QFN guidelines for PCB land pattern design and surface mount processing. Some additional recommendations are made to accommodate the special clear mold compound, which has a lower glass transition temperature (Tg) and a higher Coefficient of Thermal Expansion (CTE) compared to conventional molding compounds. This technical brief provides guidelines for assembly and handling during the board mounting process.

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1. Board Mounting Guidelines

The package board mounting process is similar to that of conventional DFN/QFN packages. However, there are some key differences in the materials used; therefore, Renesas recommends that you account for these differences in their application method. Specific guidelines in this document are meant to accommodate for the differences in the materials.

2. Product Packing

ODFN products have been qualified under JEDEC MSL test criteria, and are shipped in either a tube or tape and reel format. See the product packing label for further details. In addition to the JEDEC MSL condition, there is an additional optical characteristic (OP) that denotes baking at different conditions, see Table 1. The packing quantity varies depending on the application and purchasing options. The moisture protection seal should not be broken until the board mounting process is ready. If the seal is broken, follow standard instructions for baking conditions per Table 1.

Table 1. Dry Bake Temperature for Clear (OP) Mold Compound

Package Type	Example Pkg Types	Bake Temperature	Bake Time Duration
Optical Clear Packages	Optical clear mold compound packages for sensor IC's such as ODFN packages	110°C ±5°C	4 hours +1/-0 hrs
Optical Co-Package	Optical clear compound packages with LED and sensor.	100°C ±5°C	24 hours +1/-0 hrs

Note: Packages molded with optical (OP) clear mold compounds for photosensor and other optical IC devices turn yellow/brown if baked at higher temperatures or for long time durations. This impedes light transmission to the photosensor IC.

3. Package Construction

ODFN packages have a nominal package thickness of 0.7mm. Figure 2 shows package outline for a 6 Ld ODFN. For specific packages, see plastic packaging. It is important to design PCB land patterns that correspond to the lead dimension as explained in “PCB Land Pattern Design” on page 3.

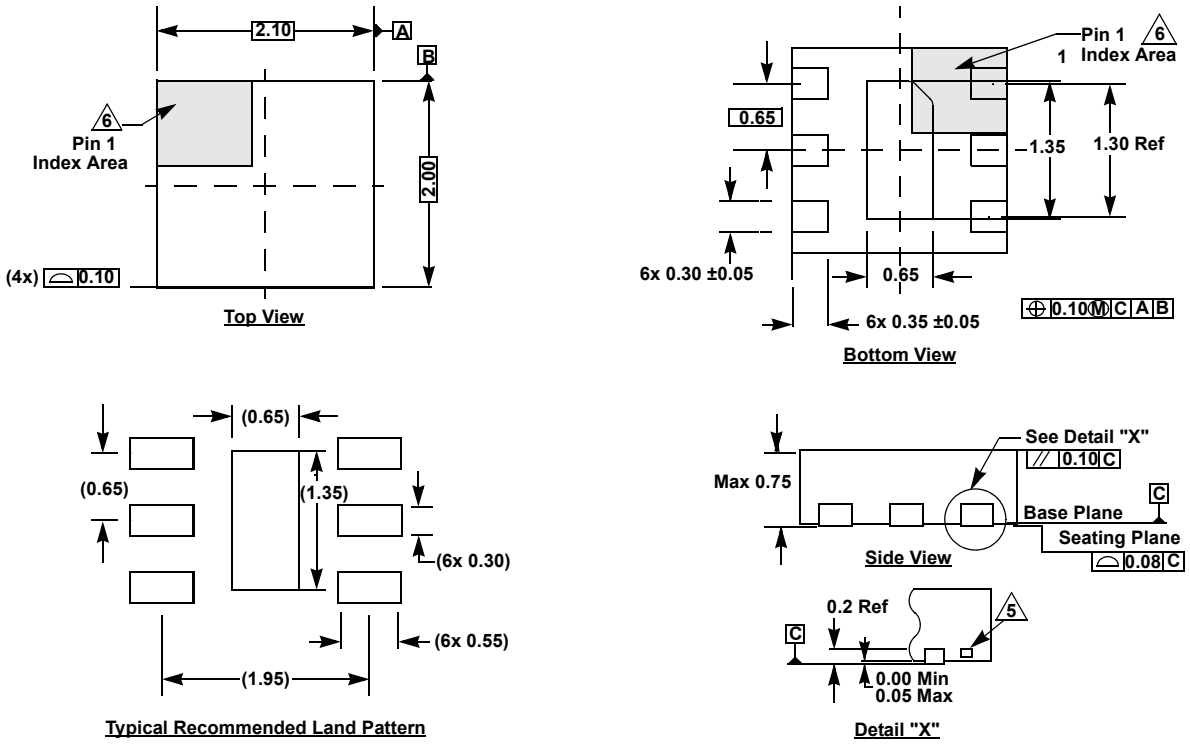

Figure 2. 6 Ld ODFN Package Dimensions

Similar to DFN and QFN packages, the ODFN has an exposed die paddle/pad as part of the package construction. As shown in Figure 2, the chamfered corner of the exposed thermal pad indicates the Pin 1 location for the product. As with the DFN or QFN, the exposed pad provides robustness to the overall solder joint strength after board mounting.

ODFN packages are assembled on pre-plated copper lead-frames, and individual units are singulated by the sawing process. The occasional presence of a slight oxide layer at the sawn surface of the copper leads is not a concern for solder joint quality. Poor wetting to this exposed side edge does not impact the solder joint quality or reliability.

3.1 PCB Land Pattern Design

TB389 provides detailed information for PCB design, DFN, QFN packages, and is applicable to ODFN packages. Additionally, package-specific land pattern information is available on package outline drawings, see Renesas support. The package outline drawings are also included in product datasheets. See Figure 3 for an example of land pattern recommendations for the 6 Ld ODFN. The main features are summarized as follows:

- 1:1 match with exposed pad area (for the 6 Ld ODFN, 0.65mmx1.35mm)
- 1:1 match with pin width (for the 6 Ld ODFN, 0.3mm)
- Land length for pin = pin length + 0.2mm (extending out from the package edge)

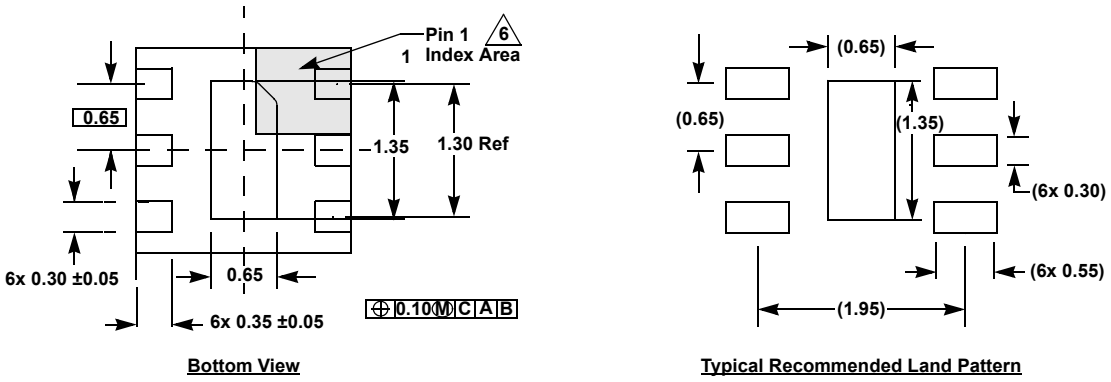

Figure 3. 6 Ld ODFN Footprint (Left) and Corresponding Land Pattern for PCB Design (Right)

Figure 4 shows a reference solder joint shape after ODFN package mounting on the PCB. The solder joint under the exposed pad is intended to provide the package stand-off height and robust assembly.

Renesas recommends that the pad definition on the board is Non Solder Mask Defined (NSMD), though Solder Mask Defined (SMD) pads of the same effective wet able dimension are acceptable. A Nickel/Gold surface finish with 0.2 micron maximum gold thicknesses is recommended for good solder wettability and shelf-life for the SMT process. OSP surface finish is also acceptable, but requires appropriate controls on shelf life and exposure of PCB to environment. HASL or solder plated finishes (pre-plated solder) should not be used for these products.

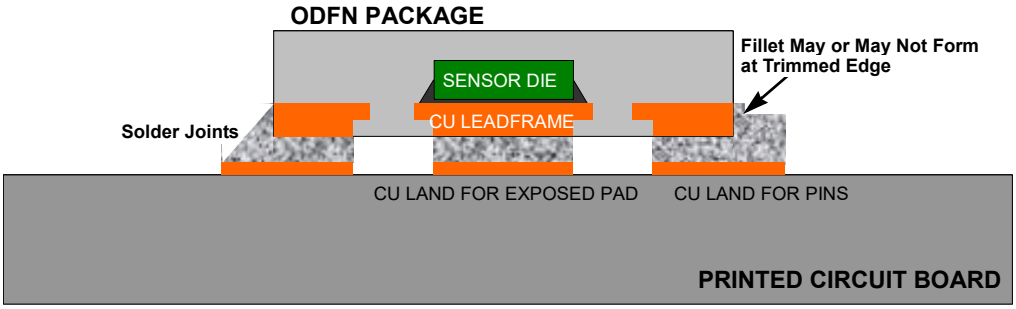

Figure 4. Schematic Showing ODFN Package Mounted on PCB

3.2 Solder Stencil

- 0.100mm or 0.125mm thick stainless steel stencil is recommended.
- The stencil is laser-cut followed by an electro-polish (chemical finishing not recommended). Alternatively an additive build-up stencil can be used.
- Solder Paste volume is a key contributor to solder joint reliability (higher solder volume leads to greater reliability). However, this must be controlled, as solder bridging can occur when the solder paste is excessive.
- Renesas highly recommends soldering the exposed package pad to the corresponding landing pad on the PCB. Care should be taken to ensure there is no excessive solder under the exposed area, as this can cause open solder joints due to excess stand-off created by the exposed pad. The optimal value for solder paste in the center pad is 70% to 80% solder paste coverage on the exposed pad area.

3.3 Solder Paste

The package itself is Pb-free, and is compatible with both eutectic Tin/Lead or Pb-free Tin/Silver/Copper solders. These packages are qualified at a +235°C maximum temperature reflow profile for eutectic solder, and at a +260°C maximum temperature reflow profile for Pb-free solder. Solder paste with “no-clean” flux and “Type 3” or “Type 4” solder particle size distribution is recommended.

3.4 Reflow Profile

Direct Infrared (IR) heating of these packages must not be done as it can damage the part. Pure convection reflow of these parts is recommended. Typical reflow profiles per JEDEC J-STD-020 criteria are recommended for the eutectic Sn/Pb and PB-free Sn/Ag/Cu solders. Peak temperature for the eutectic Sn/Pb profile is not to exceed +235°C. The Pb-free profile is not to exceed +260°C.

3.5 Visual Inspection

Visual inspection of solder joints should be done. Verify that there is no solder bridging between pads, and that the solder joint is “bright-and-shiny” (lead-free appears 'dull' compared to Sn/Pb). The package can not be tilted or off-center with respect to the PCB land pattern. A solder fillet at the edge of the package leads is not a requirement, and in fact may not form at all. Hand solder touch-up is not recommended as excess heat from the air nozzle or soldering iron can damage the transparent mold compound.

3.6 ODFN Specific Application Guidelines

The transparency requirement of Ambient Light Sensing products (ALS) does not allow conventional filler loading as a means for controlling mechanical properties of the mold compound (such as Coefficient of Thermal Expansion (CTE), modulus, glass transition temperature (Tg)). As such, the CTE of a clear epoxy is higher than a conventional black epoxy with fillers, has a lower modulus, and a lower Tg. The following sections outline features of the ODFN product for proper application of the product.

3.6.1 Sensor Location and Optics Design

In general, the package body center does not always coincide with the center of the light sensor. The sensor location (green area in top part of IC) is offset from the geometric center of the IC. The location of the sensor itself is specific to the product design in question, and therefore is obtained from the product datasheet. Figure 5 on page 5 shows an example of the sensor location description. In this example, the sensor area is 0.43mmx0.61mm, and it is offset from the center of the IC by 0.25mm. The application set-up should be designed to lead the light to the center of the sensor area and not to the center of the package. On the other hand, the sensor surface height is always located at 0.28 ±0.10mm below the top surface of the package. Solder joint and package height (0.7mm) should also be considered in calculating the sensor surface height from the PCB top surface.

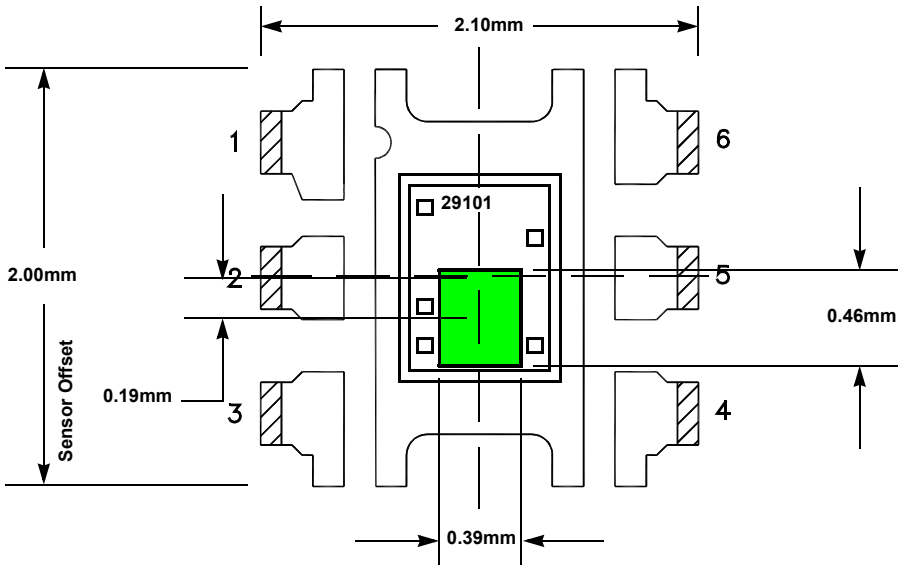

Figure 5. Example of Sensor Location Description

3.6.2 Moisture Sensitivity and Bake Conditions

ODFN packages are qualified at JEDEC moisture sensitivity levels for both +235°C and +260°C solder reflow profiles. The properties of clear mold compound are such that moisture saturation occurs rapidly. Therefore, it is important to control the exposure time when the moisture protection seal is broken. Renesas recommends that ODFN components are baked according to the moisture sensitivity level labeling on the reel if the exposure time exceeds the recommended level on the label prior to board mounting.

For recommended baking conditions, see Table 1 on page 2. A bake temperature higher than +110°C can result in discoloration of the clear molding compound.

3.6.3 Pick-and-Place with Clear Packages

These optically clear packages are fully compatible with vision-based placement machines. For machines without “auto vision recognition”, it may be necessary to manually adjust the machine sensitivity to avoid recognition errors. Renesas does not recommend placing these packages using mechanical centering placement machines or Chip-shooters.

3.6.4 Rework and Associated Risks

ODFN products can be reworked using a reflow profile that closely matches the production reflow profile described earlier. Do not expose ODFN packages to >260°C during rework operation. When rework is involved, do not use the same ODFN unit upon removal from the PCB. Replace with a new ODFN unit.

Maximum reflow that the ODFN unit can see is three times. Excessive heating of the clear mold compound can result in change in color of the mold compound and can also compromise wire bond integrity due to high coefficient of thermal expansion of the mold compound material.

3.6.5 Marking and Traceability

ODFN products cannot be marked on the top side of the package due to the need for unobstructed transparency. On the bottom of the package, there is a 4-letter code laser-marking that traces the lot and part details. In addition, the lead frame has a special Pin 1 notch cut-out in the exposed pad next to the Pin 1 lead (top view), which allows verification for correct Pin 1 orientation after mounting on the PCB.

4. Revision History

Rev.	Date	Description
3.00	May.31.19	Updated to new formatting throughout. Updated Figure 1. Changed JEDEC MSL-3 to: JEDEC MSL. Updated Product Packing section and added Table 1. Updated Package Construction, PCB Land Pattern Design, Moisture Sensitivity and Bake Conditions, Pick-and-Place with Clear Packages, and Rework and Associated Risks sections. Added Revision History section. Updated Disclaimer.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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