

Introduction

Today's high speed D/A converters are used in communications applications such as:

- Frequency Hopping Radios
- Cellular Base Stations
- Direct Digital Synthesis

These converters need to provide good Spurious Free operation to ensure signal integrity and low inter-channel interference.

The glitch of a given DAC can limit the overall spectral performance of the converter and make it unusable. There are many definitions of this phenomena known as glitch and this article will try to explain them.

Glitch Area

When a given converter is updated with a new data value the output of the DAC tries to generate a new output voltage. As shown in Figure 1 the output slews to a new final voltage. This step response contains glitch, and settling effects, that must die down in order to reach the new steady state output.

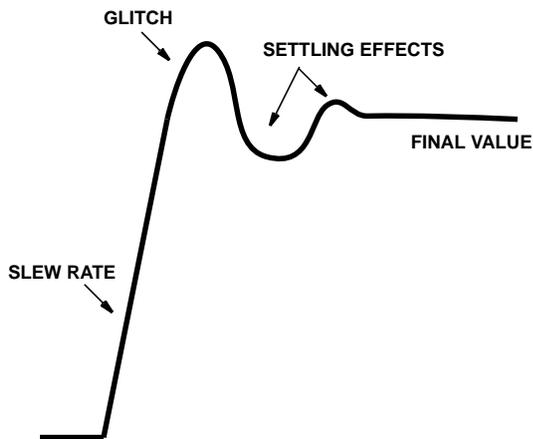
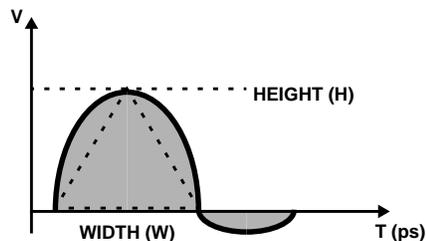


FIGURE 1. DAC OUTPUT RESPONSE

Glitch Area is the measure of the area under the first transient of the output of the D/A converter. The glitch is assumed to be triangular in shape and is calculated as shown in Figure 2.



GLITCH AREA = 1/2 (H X W)

FIGURE 2. GLITCH AREA

The glitch is the first peak transient. Some manufacturers use the glitch 'doublet' theory where the specification given is a net glitch area

The glitch doublet sums the area of the initial glitch transient and the area of the settling effects. These areas are then added together to yield some very small unrealizable number by most board level designers.

The 'singlet' or peak glitch area is a more realistic specification for board and system level designers as they can more adequately evaluate the severity of the glitch.

Glitch Cause

One cause of glitch is the time skew between bits of the incoming digital data. In a DAC that has no internal register, the time delta between logic inputs causes internal current sources to switch asynchronously resulting in a momentary surge in current. The HI5721 employs an internal register to synchronize the incoming data.

Typically the switching time of digital inputs are asymmetrical, meaning that the turn off time is faster than the turn on time. Unequal delay paths through the device can cause one current source to change before another.

To reduce this, an internal register is used to latch all the digital input data on one clock edge so as to synchronize them in time. Careful layout and sizing of the internal current sources also helps to maintain concurrent switching times.

Reducing Glitch

In traditional DACs the worst case glitch usually happens at the major transition i.e. 01 1111 1111 to 10 0000 0000. But in the HI5721, the worst case glitch is moved to the 00 0001 1111 to 11 1110 0000 transition. This is achieved by the split R/2R-segmented current source architecture, which decreases the amount of current switching at any one time and makes the glitch practically constant over the entire output range.

Deglitching Techniques

Deglitching the output of a high speed converter is no trivial task. Figure 3 shows an ideal deglitching circuit. A deglitcher is a sample and hold that holds the previous conversion while the converter is settling to the new output. A deglitching sample and hold potentially could have a hold to track glitch, that can be larger than the DAC's glitch. The amplifiers in this circuit must be unity gain stable to 500MHz and have a settling time of 2ns for a 1V_{P-P} swing to an error band of 0.1%.

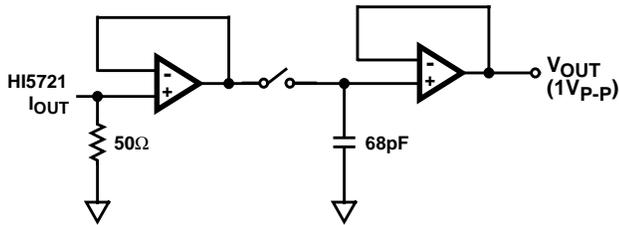


FIGURE 3. A CLASSIC D/A DEGLITCHING CIRCUIT

The on resistance of the switch must be less than 2Ω and have a leakage of less than 1pA to minimize droop. This is practically impossible with the switches available on the market today. The best way to reduce glitch is to optimize the high speed DAC design as done in the Intersil HI5721.

Filtering Glitch

Since the glitch is a transient event this leads designers to believe that a simple low pass filter can be used to eliminate or reduce the size of the glitch. In effect low pass filtering a glitch tends to “smear” the event and does little to remove the energy of the transient. Glitch contains many spectra from near DC up to and beyond the Nyquist sampling rate of the converter. By low pass filtering, the high frequency components of the glitch are removed but the main or majority of low frequency components are not.

This leaves a designer with a usable spectral window however, this technique usually results in a higher noise floor at low frequencies. Noise also increases closest to the cutoff frequency of the filter.

Picking a Low Glitch D/A

The best methods for choosing a low glitch converter are to choose those that specify the first transient area and those converters that incorporate architectures to minimize glitch. Trying to remove the glitch from a ‘glitchy’ DAC is not trivial and can simply move the problem to other places as well as complicate the design.

The HI5721's Peak Glitch

Although the HI5721 specifies a glitch doublet area of 1.5pV-sec (to meet specs quoted by other D/A manufacturers) the peak glitch is ~3.0pV-sec. Figures 4 and 5 show the typical glitch height and width.

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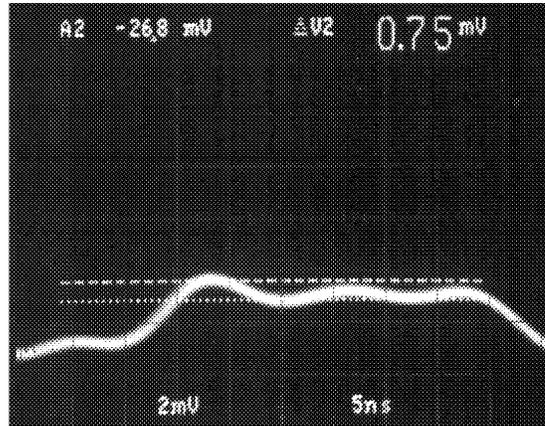


FIGURE 4. GLITCH HEIGHT
Code 64_D - 60_D, Scope 50Ω GND

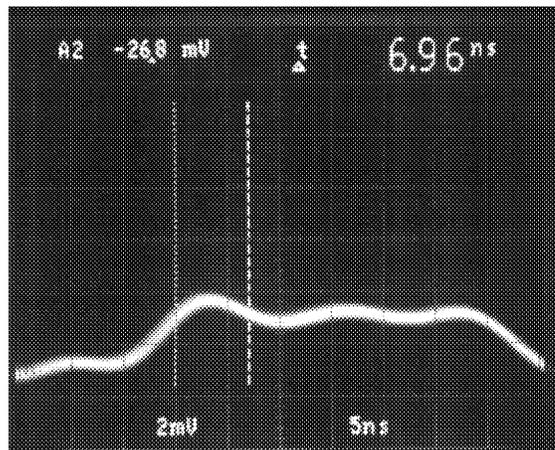


FIGURE 5. GLITCH WIDTH
Code 64_D - 60_D, Scope 50Ω GND

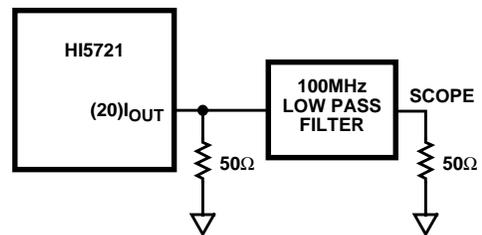


FIGURE 6. GLITCH TEST SETUP

Summary

Testing standards are evolving and as technology improves the real specifications become evident. For state of the art D/A converters, the HI5721 provides designers with the lowest glitch performance, tested under the most stringent conditions.