PCB Design and Assembly Recommendations for Renesas Power Modules

The Renesas power module product family offers a unique packaging concepts. Power modules encompass lead pitches of 0.5mm and above. These packages offer a variety of benefits including reduced lead inductance and both perimeter I/O pins (to ease PCB trace routing) and in-board I/O pins (for complex pinouts). Also, the exposed Au plated copper ePad technology offers good thermal and electrical performance. These features make the power packaged POL module an ideal choice for many new applications where thermal and electrical performance are important.

This tech brief provides general guidelines for use in developing land pattern layouts and solder mounting processes. It should be emphasized that these guidelines are general in nature and should only be considered a starting point in this effort. The user must apply their actual experiences and development efforts to optimize designs and processes for their manufacturing practices and the needs of varying end-use applications.

Contents

1. Moisture Sensitivity 2
1.1 Moisture Sensitivity Handling, Packing, and Use 2
1.1.1 Moisture Sensitivity 2
1.1.2 Packing and Labeling 2
1.1.3 Handling and Use 2
2. Reliability 2
2.1 Standard Power Module Development Flow and Qualification 2
2.2 Typical Reliability Qualification Stress Tests 2
3. PCB Design Guidelines 3
4. PCB Assembly Process 3
4.1 PCBA Solder Joint Voiding Recommendations 4
5. Revision History 5

© 2024 Renesas Electronics

1. Moisture Sensitivity

1.1 Moisture Sensitivity Handling, Packing, and Use

1.1.1 Moisture Sensitivity

Renesas power modules are moisture-sensitive devices. All Renesas power modules meet Moisture Sensitivity Level (MSL) 3 per J-STD-020.

Pb-free reflow is qualified per J-STD-020. Peak temperatures vary based on module thickness and volume and are specified on the MSL label and our product pages.

1.1.2 Packing and Labeling

Renesas packs and labels power modules per J-STD-033. Standard packing is in JEDEC trays. For more information about tape and reel specifications for integrated circuits, see TB347.

1.1.3 Handling and Use

Customers should handle and use power modules per J-STD-033. The modules are MSL 3 qualified – do not exceed 168-hour floor life. If floor life is exceeded, bake at +125°C for 48 hours.

2. Reliability

2.1 Standard Power Module Development Flow and Qualification

Discrete component reliability reports are reviewed and approved before the package and product build for qualification (design phase). The Renesas corporate process reliability group tests and approves process technology wear-out data (TDDB, Hot Carrier, HTRB, and EM) to ensure the process technology for embedded controllers, power FETs, and power stage meets the Renesas wear-out goals.

The package engineering group executes look-ahead evaluations to ensure the package is robust and meets design goals. The power module and package move into the product/package reliability qualification phase when the design phase is complete.

2.2 Typical Reliability Qualification Stress Tests

- MSL Test – Determines Moisture Sensitivity Level per J-STD-020.
- Precondition Stress – BHAST, UHAST, THB, and TMCL samples are preconditioned. Stress includes moisture soak per MSL and three-time reflow cycles at the Pb-free peak reflow temperature, per J-STD-020.
- BHAST or THB – Static bias in a moisture-rich environment. Stress targets possible electrolytic-related failure mechanisms. Typical stress runs for 96 hours or 1000 hours, respectively.
- High-Temperature Operating Life (HTOL) – Dynamic operation, maximum operating voltage per datasheet. This stress test verifies the long-term reliability of the module. Data is used to calculate the FIT rate and MTTF. Typical stress runs for 1000 hours with module temperature set at +125°C.
- Temperature Cycling (TMCL) – This stress test targets flaws in the thermo-mechanical properties of the module design or BOM. Typical stress includes 500 cycles at -65°C/+150°C or 1000 cycles at -40°C/+125°C.
- High-Temperature Storage Life (HTSL) – This stress test indicates thermally activated failure mechanisms. Typical stress runs for 1000 hours at 150°C.
- Unbiased HAST (UHAST) – This stress test accelerates moisture penetration through a protective mold compound and is used to identify failure mechanisms internal to the package, such as galvanic corrosion. Typical stress runs for 96 hours at +130°C/85% RH, 2ATM pressure.

3. PCB Design Guidelines

- The power module package outline drawing in the product datasheet includes a recommended PCB land pattern.
- PCB lands in the form of SMD pads are preferred to improve gasketing.
- PCB lands should match the recommended power module package POD.
- Large ePads should be windowpaned with SM.
  - The SM webs provide gasketing to improve solder release during printing, control solder spread/thickness, and provide venting for out-gassing during reflow.
  - See the Package Outline Drawing (POD) for specific design recommendations.
- Solder stencil apertures should be slightly smaller than the solder mask openings, 30µm typical.
- Via in pad should be filled and plated over (VIPPO) to prevent solder wicking into the vias.
- Electroless Nickel Immersion Gold (ENIG) PCB finish recommended.

4. PCB Assembly Process

- Profile with a thermal couple placed under the power module.
- Follow solder paste supplier's reflow profile, but do not exceed the power module's recommended peak reflow temperature. Pb-free reflow peak temperature is 245°C.
- Do not exceed 168-hour out of bag limit (MSL 3 qualified).
  - If time limit exceeded bake per MSL label instructions.
- Solder foil preforms may be used on large ePads to reduce solder voids and flux residue and to increase stand-off height.
- Use the following assembly tooling materials for the SMT process.
  - Electroless Nickel Immersion Gold PCB finish (ENIG)
  - Stainless steel, laser cut stencils with Nano-coating
  - 4 mil or 5 mil stencil thickness
  - No clean, low void, Type 3 or 4 solder paste per ANSI/J-STD-005
- Follow paste suppliers recommendation for air or nitrogen purge during reflow.
- Solder Print Inspection (SPI) is recommended to ensure consistent solder deposit area, height, and volume.

Table 1. Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat/Soak	
Temperature Min (T_{SMIN})	150°C
Temperature Max (T_{SMAX})	200°C
Time (t_S) from (T_{SMIN} to T_{SMAX})	100-140 seconds
Ramp-up rate (T_L to T_P)	1.3-3.0 °C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) maintained above T_L	60-90 seconds
Peak package body temperature (T_P)	245°C
Time (t_P) within 5°C of the specified classification temperature (T_C); see Figure 1	30 seconds max.
Ramp-down rate (T_P to T_L)	4°C/second max.
Time 25°C to peak temperature	8 minutes max.

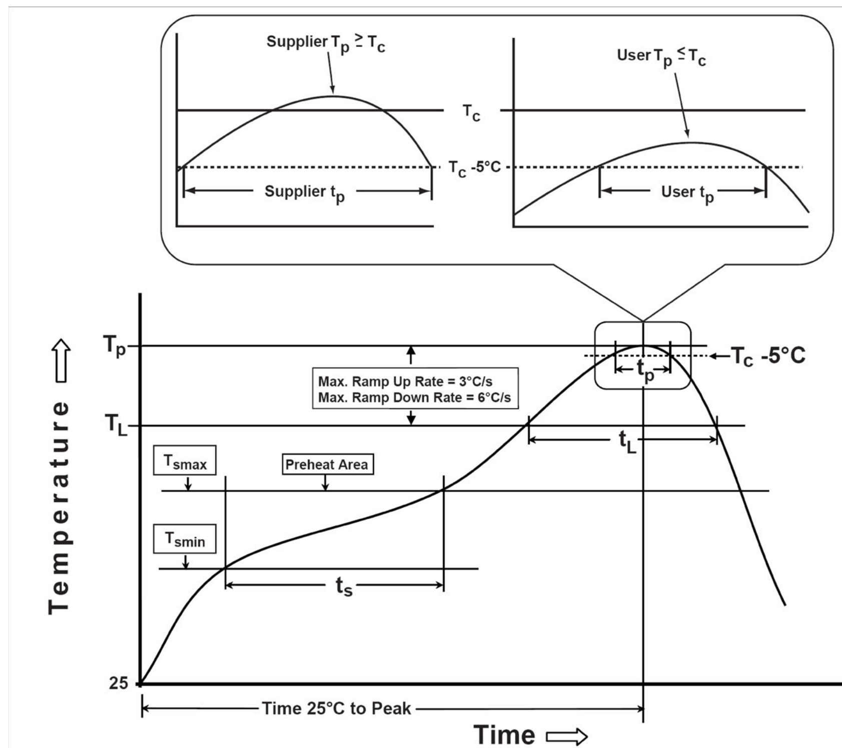

Figure 1. Peak Reflow Profile

4.1 PCBA Solder Joint Voiding Recommendations

- There are no IPC standards for solder joint voids for bottom-terminated components.
- Renesas recommends a 25% maximum solder void for small I/O pads and 50% maximum solder void for large epads.

5. Revision History

Revision	Date	Description
1.01	Jan 29, 2024	Updated Table 1.
1.00	Jun 12, 2023	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2024 Renesas Electronics Corporation. All rights reserved.