ISL70061SEH

PSpice Simulation Results

Abstract

The ISL70061SEH PSpice model is a nominal model of the ISL70061SEH load switch IC. It simulates the load switch functionality and the typical performance across temperature of the datasheet specification parameters. Basic ON/OFF control, Undervoltage Lockout (UVLO), Reverse Current Protection (RCP), selectable discharge MOSFET feature, and slow turn-on controlled rise time functions are modeled. The model simulations closely match the typical performance curves in the datasheet.

The first section of this document provides a brief explanation of using the model to generate a general functional test simulation.The simulation shows the functionality of ON/OFF control, UVLO, slow turn-on rise time, and the selectable discharge MOSFET feature.

The second section shows PSpice simulation results of the load switch compared to characterization test results using the ISL70061SEHEV1Z evaluation board. Parameters for r_{ON} vs V_{SWI} vs temperature, r_{ON} vs I_{SW} vs temperature, turn-on and turn-off waveforms, and I_{RCP} enter vs V_{SWO} vs temperature response are compared in this report.

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Related Literature

For a full list of related documents, visit our website:

- ISL70061SEH and ISL73061SEH device pages

1. PSpice General Functional Test Simulation

The simulation shown in Figure 3 shows how the ISL70061SEH PSpice model replicates the load switch functionality for basic on/off control, UVLO, the selectable discharge MOSFET feature, and slow turn-on controlled rise time.

1.1 ISL70061SEH.LIB and ISL70061SEH.OLB PSpice Files

The PSpice ISL70061SEH.LIB and ISL70061SEH.OLB files can be downloaded from the Renesas website at the ISL70061SEH and ISL73061SEH device pages on the **Download** tab. The file path to the ISL70061SEH.OLB sub-circuit (Figure 1) must be added to the Cadence parts placement tool. Then it can be used in simulation schematics. The ISL70061SEH.LIB file path must be added to the Cadence simulation profile as shown in Figure 2. The Renesas group uses Cadence Allegro Design Entry CIS 16.6-S071 (v16-6-112FZ).

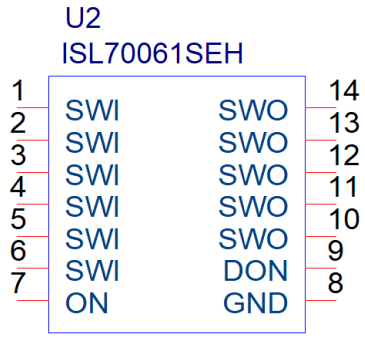

Figure 1. ISL70061SEH Sub-Circuit (ISL70061SEH.OLB)

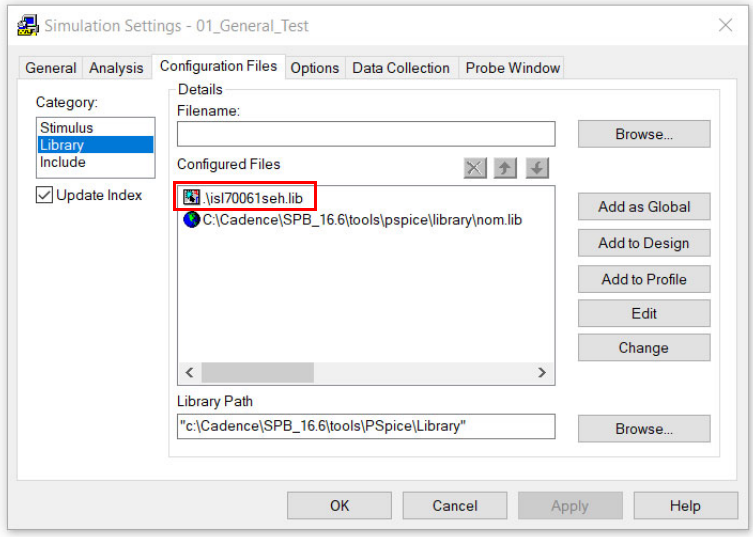

Figure 2. ISL70061SEH.LIB

1.2 Functional Simulation Schematic

Figure 3 below shows the PSpice simulation schematic used for the functional simulation test.

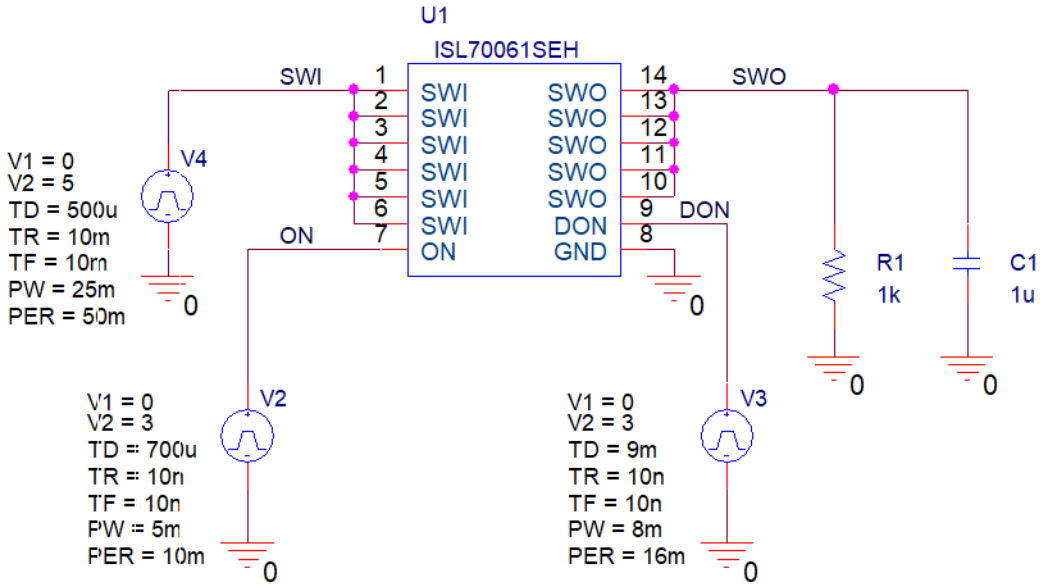

Figure 3. ISL70061SEH PSpice General Functional Test Schematic

1.3 Functional Simulation Results

The time-domain transient simulation results for the functional test is shown in Figure 4. There are plots for SWI (blue trace), DON (red trace), ON (green trace) and SWO (black trace) vs Time. The functional states of the load switch are indicated by the numbers 1-6 on the SWO plot. The functional state relates to the numbers 1-6 as follows:

1. The part is in the UVLO off state. Because SWI voltage is below the UVLO falling threshold of 2.2V, the switch is OFF even though ON = High.
2. When the SWI voltage reaches the UVLO rising threshold voltage of 2.3V, the part is no longer in the UVLO state and because ON = High the switch turns ON.
3. ON = Low and the switch turns OFF. The output slowly decays to ground. The 1kΩ load resistor with the 1µF load capacitance connected at the output slowly decays the output to ground.
   Note: DON = Low (discharge MOSFET circuitry is disabled).
4. ON = High and the switch turns ON with a controlled rise time of ≈ 600µs.
5. DON = High (discharge MOSFET circuitry is enabled), ON = Low: The switch turns OFF. The internal 122Ω discharge resistor quickly discharges the output to ground.
6. The part enters the UVLO off state. Because SWI voltage is below the UVLO falling threshold voltage of 2.2V, the switch is OFF even though ON = High.

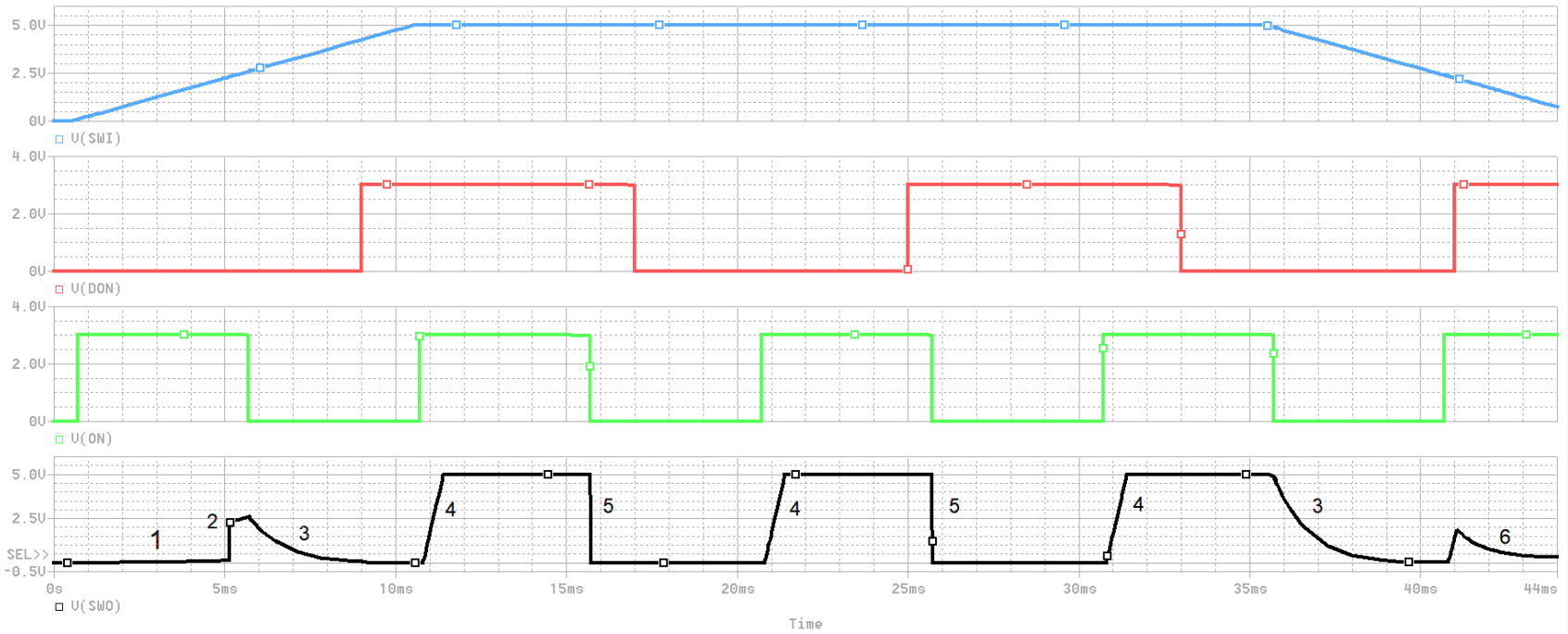

Figure 4. ISL70061SEH PSpice General Functional Simulation Results

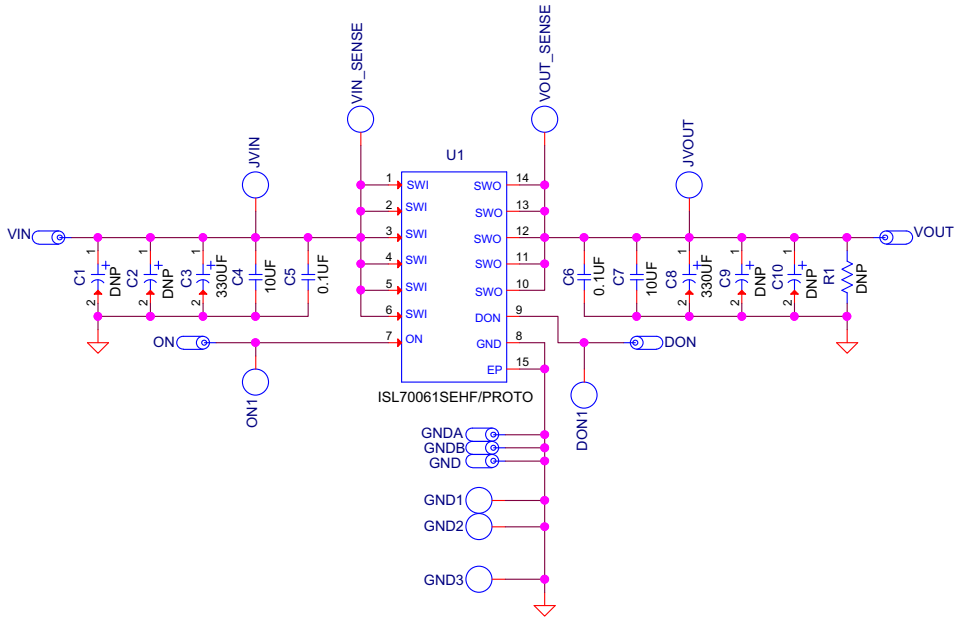

Figure 5. ISL70061SEHEV1Z Rev. A Evaluation Board Schematic

2. PSpice Simulation Results Verses Characterization Test Results

The ISL70061SEH PSpice model is designed to meet the typical values across temperature of the specification parameters in the ISL70061SEH datasheet. PSpice simulations closely match the typical performance curves in the datasheet. This section, for a few parameters, provides a comparison between the PSpice simulation results and actual part characterization test results.

Figure 6 through Figure 31 shows the PSpice simulation results vs the load switch characterization test results for r_{ON} vs V_{SWI}, r_{ON} vs I_{SW}, turn-on and turn-off timing, and the RCP enter response.

For a particular parameter, the graph on the left is the PSpice simulation result and the graph on the right is the characterization result. For example, Figure 6 is the PSpice result and Figure 7 is the characterization result for r_{ON} vs V_{SWI} vs temperature with I_{SWO} = 1A. You can quickly compare the graphs to see how the PSpice simulation result correlates with the characterization test result.

2.1 r_{ON} vs V_{SWI} vs Temperature

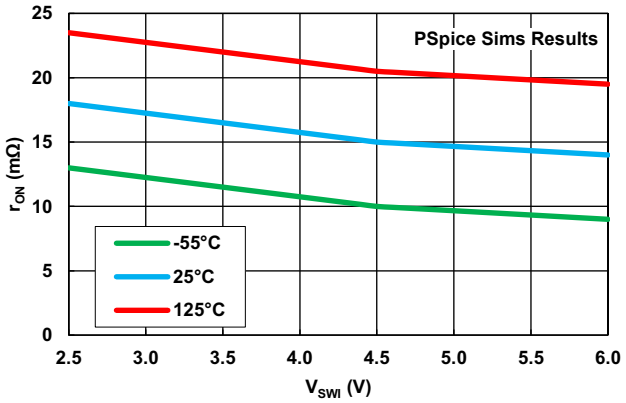

Figure 6. r_{ON} vs V_{SWI} vs Temperature, I_{SW} = 1A (PSpice Results)

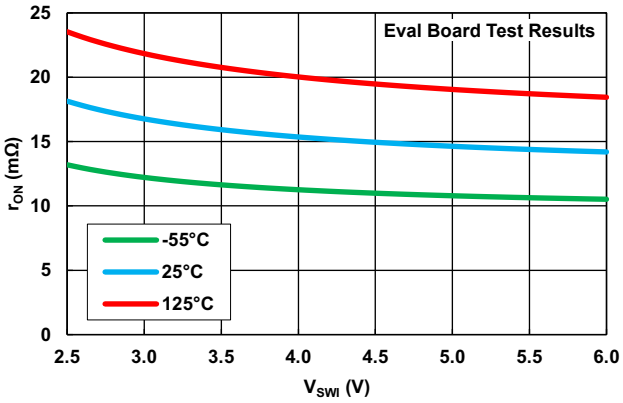

Figure 7. r_{ON} vs V_{SWI} vs Temperature, I_{SW} = 1A (Characterization Results)

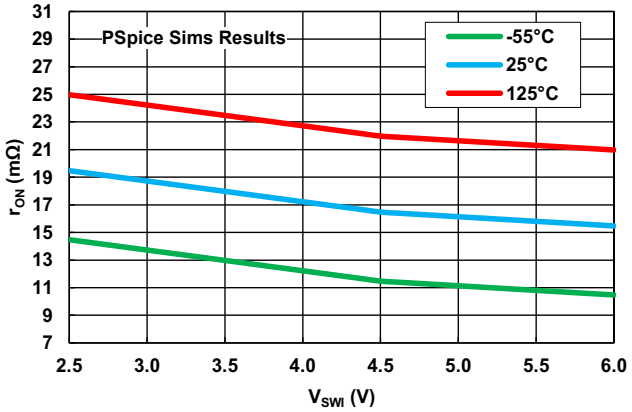

Figure 8. r_{ON} vs V_{SWI} vs Temperature, I_{SW} = 3A (PSpice Results)

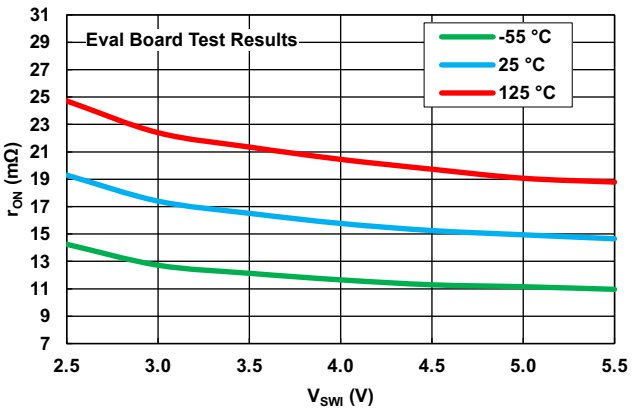

Figure 9. r_{ON} vs V_{SWI} vs Temperature, I_{SW} = 3A (Characterization Results)

2.2 r_{ON} vs I_{SWO} vs Temperature

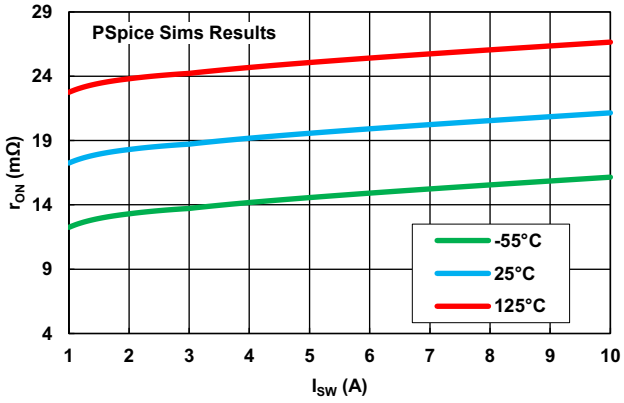

Figure 10. r_{ON} vs I_{SW} vs Temperature, V_{SWI} = 3V (PSpice Results)

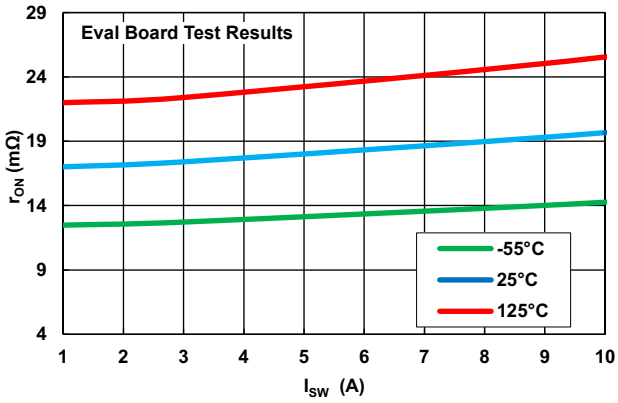

Figure 11. r_{ON} vs I_{SW} vs Temperature, V_{SWI} = 3V (Characterization Results)

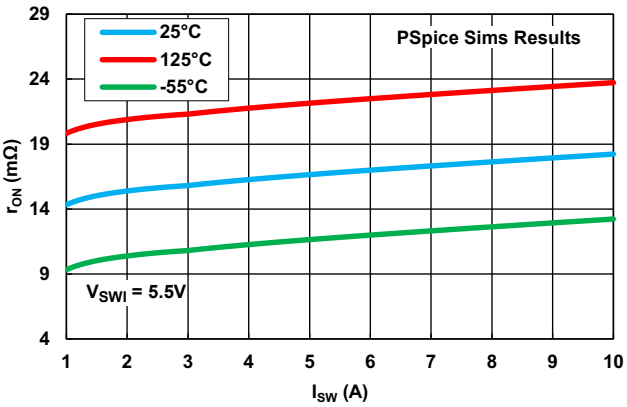

Figure 12. r_{ON} vs I_{SW} vs Temperature, V_{SWI} = 5.5V (PSpice Results)

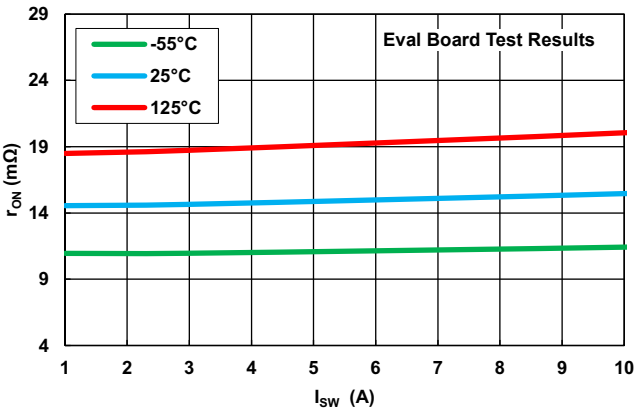

Figure 13. r_{ON} vs I_{SW} vs Temperature, V_{SWI} = 5.5V (Characterization Results)

2.3 Turn-ON and Turn-OFF Waveforms

The ISL70061SEHEV1Z evaluation board schematic (Figure 5) has 300µF//10µF//0.1µF capacitors at the SWI input and has 0.1µF//10µF//300µF at the SWO output. Figure 14 through Figure 21 show the PSpice simulation vs evaluation board turn-on and turn-off test results with the 300µF//10µF//0.1µF capacitors. Figure 22 through Figure 29 show the PSpice simulation vs evaluation board test results with the 300µF capacitor removed leaving the 10µF//0.1µF capacitors installed at both the SWI input and SWO input.

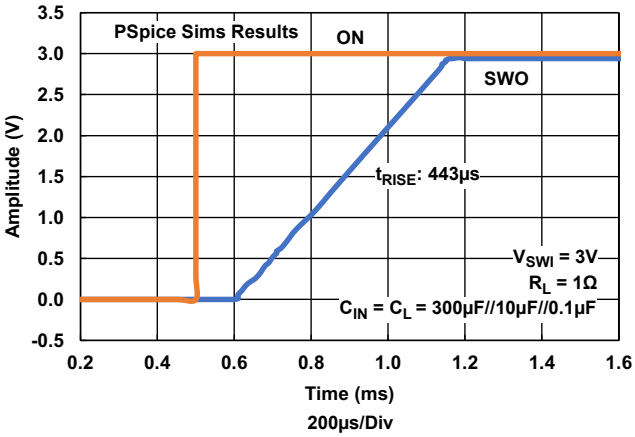

Figure 14. Turn-On Waveform, 3V, C_L = 310.5µF (PSpice Results)

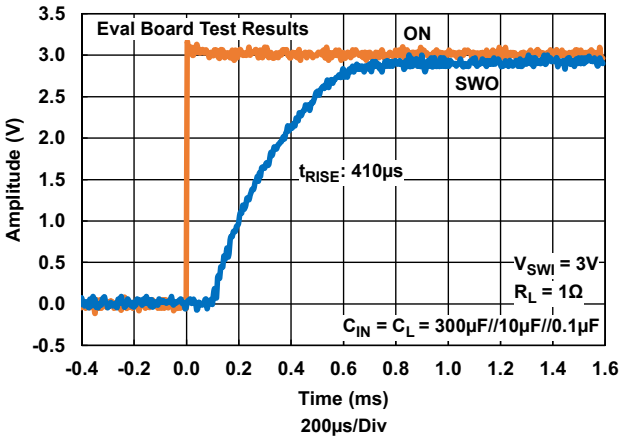

Figure 15. Turn-On Waveform, 3V, C_L = 310.5µF (Characterization Results)

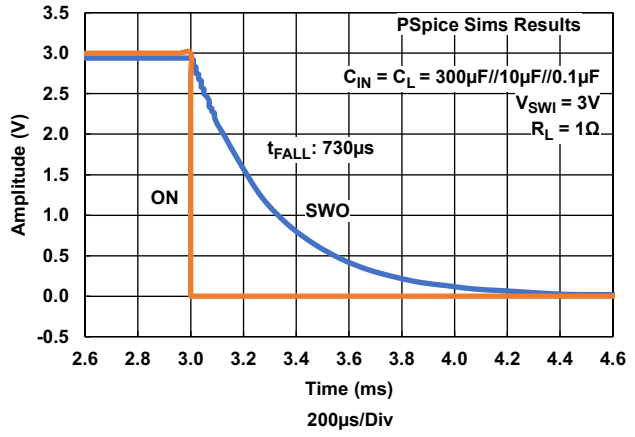

Figure 16. Turn-Off Waveform, 3V, C_L = 310.5µF (PSpice Results)

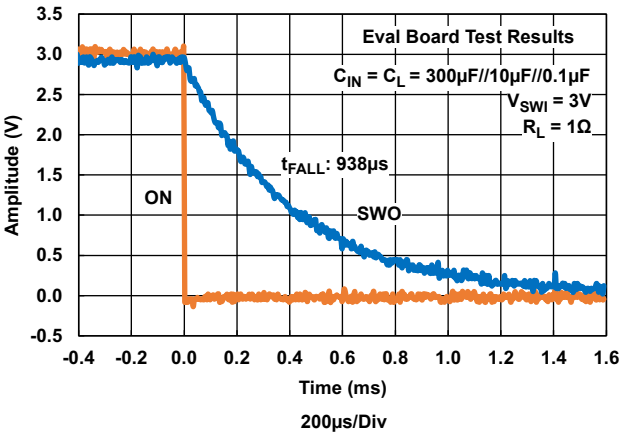

Figure 17. Turn-Off Waveform, 3V, C_L = 310.5µF (Characterization Results)

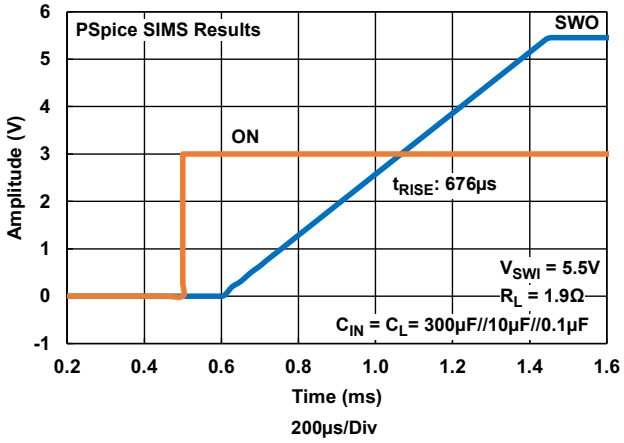

Figure 18. Turn-On Waveform, 5.5V, C_L = 310.5µF (PSpice Results)

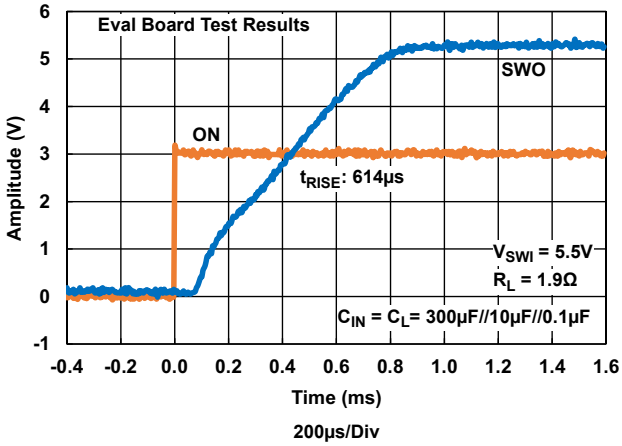

Figure 19. Turn-On Waveform, 5.5V, C_L = 310.5µF (Characterization Results)

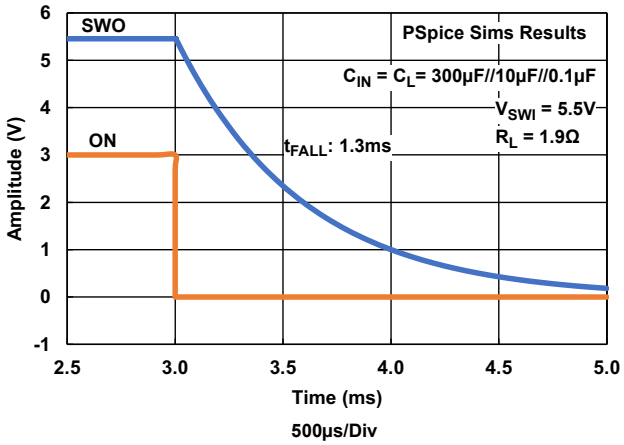

Figure 20. Turn-Off Waveform, 5.5V, C_L = 310.5µF (PSpice Results)

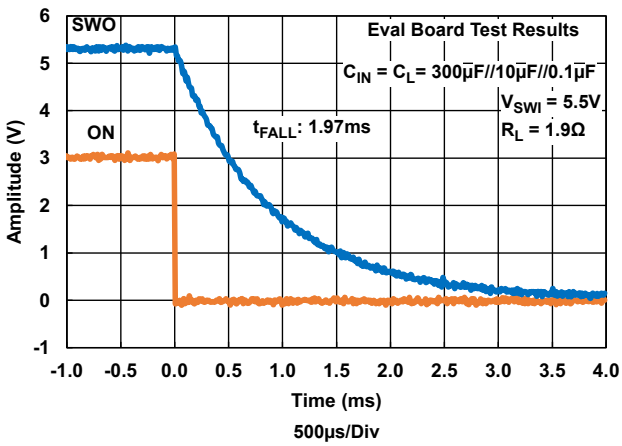

Figure 21. Turn-Off Waveform, 5.5V, C_L = 310.5µF (Characterization Results)

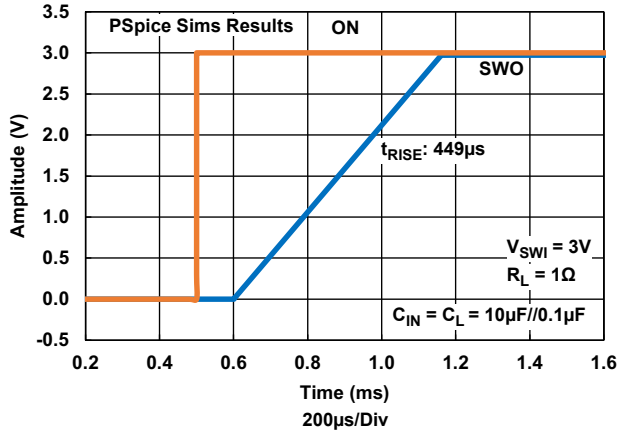

Figure 22. Turn-On Waveform, 3V, C_L = 10.1µF (PSpice Results)

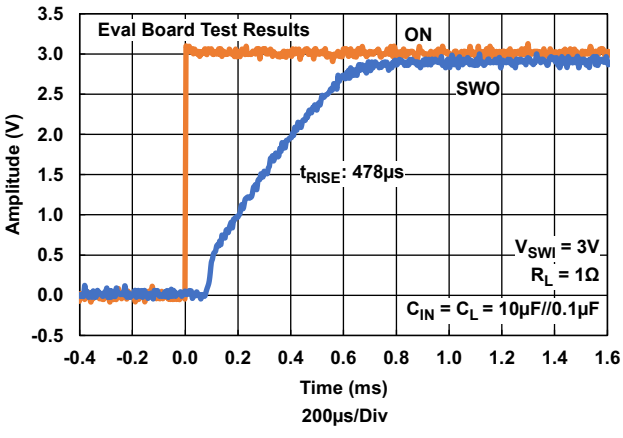

Figure 23. Turn-On Waveform, 3V, C_L = 10.1µF (Characterization Results)

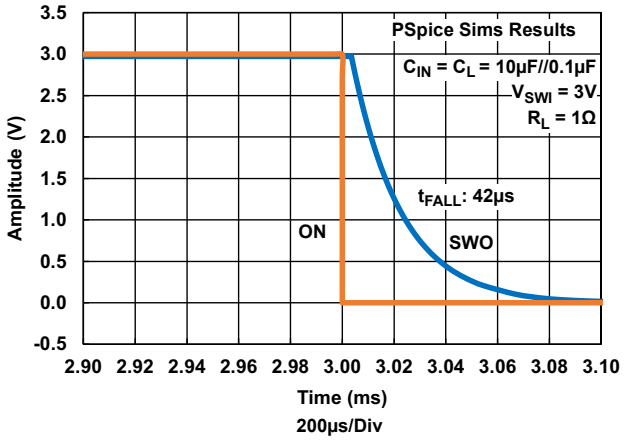

Figure 24. Turn-Off Waveform, 3V, C_L = 10.1µF (PSpice Results)

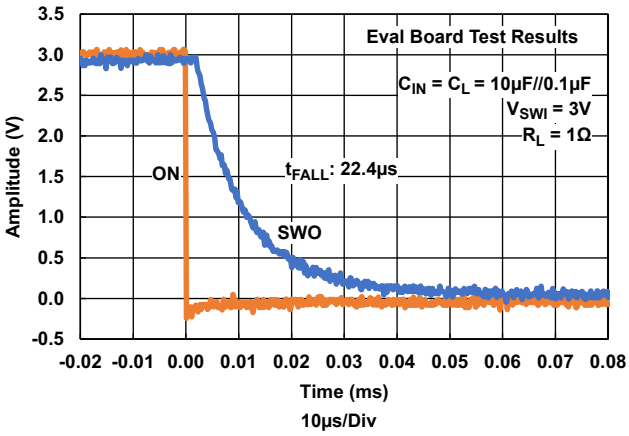

Figure 25. Turn-Off Waveform, 3V, C_L = 10.1µF (Characterization Results)

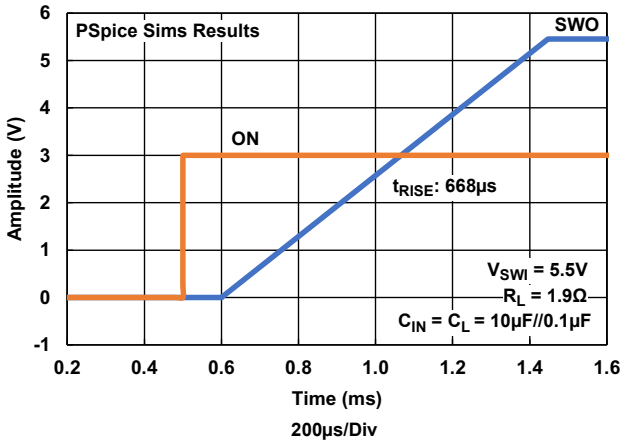

Figure 26. Turn-On Waveform, 5.5V, C_L = 10.1µF (PSpice Results)

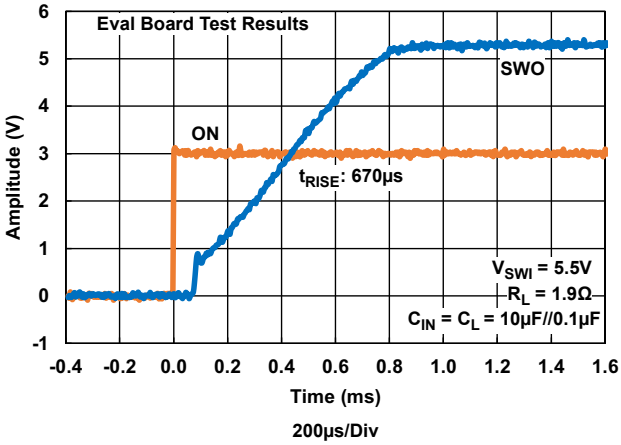

Figure 27. Turn-On Waveform, 5.5V, C_L = 10.1µF (Characterization Results)

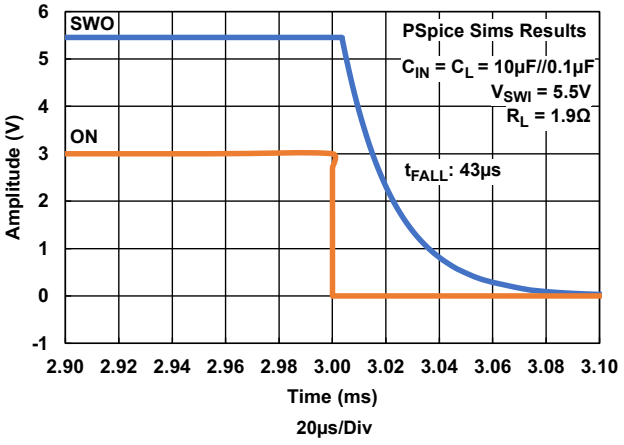

Figure 28. Turn-Off Waveform, 5.5V, C_L = 10.1µF (PSpice Results)

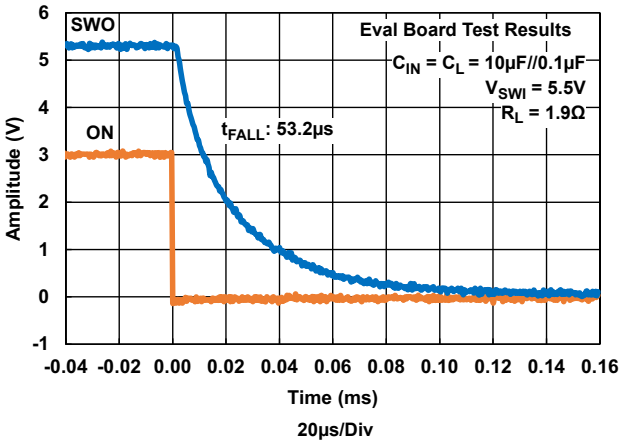

Figure 29. Turn-Off Waveform, 5.5V, C_L = 10.1µF (Characterization Results)

2.4 Reverse Current Protection (RCP) Waveforms

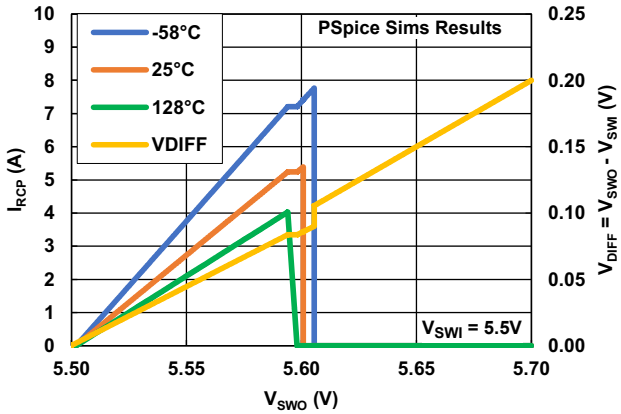

Figure 30. I_{RCP} Enter vs V_{SWO} vs Temperature, 5.5V (PSpice Results)

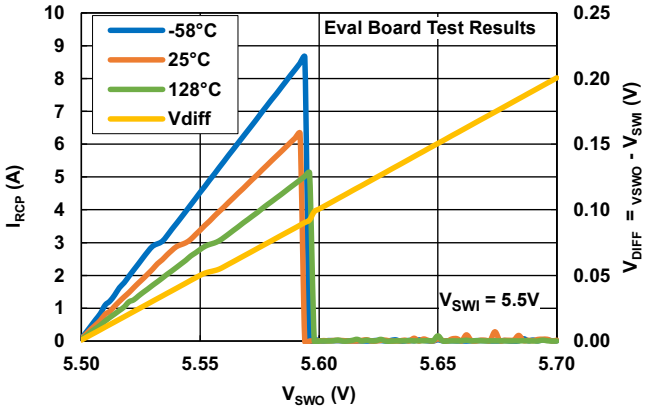

Figure 31. I_{RCP} Enter vs V_{SWO} vs Temperature, 5.5V (Characterization Results)

2.5 Conclusion

The ISL70061SEH PSpice model replicates the functionality of the ISL70061SEH load switch. It closely matches the characterization curves in the ISL70061SEH datasheet and meets the typical values across temperature of the parameters in the datasheet specification table.

3. Revision History

Rev.	Date	Description
1.00	Jan.6.20	Initial release

Notice

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