Designing with Renesas High-Voltage GaN Devices

Introduction

Renesas D-Mode GaN (Depletion-Mode Gallium Nitride) devices provide significant advantages in power converter designs by offering lower gate charge, faster switching speeds, and lower body-diode reverse recovery charge. GaN devices exhibit in-circuits switching much higher than that of other switch technologies. The inherent rapid switching of GaN devices reduces voltage or current cross-over power losses, enabling high frequency operation while simultaneously achieving high efficiency. However, the accompanying high voltage and current transient during the switching due to fast switching nature of GaN may provide some design challenges if attention is not made to fundamental design practices.

Renesas high-voltage GaN devices are designed to be compatible with standard silicon gate drivers, eliminating the need for specialized driver circuitry and simplifying system integration. To fully leverage the benefits of Renesas GaN technology, adherence to proven design practices is strongly recommended.

This document outlines the following key considerations:

- Designing robust gate drive circuits and optimal gate resistor selection
- Strategic placement of critical components to minimize parasitic effects
- Optimizing PCB layout to reduce inductance in gate and power loops
- Validating switching performance through targeted measurements and analysis

By following these guidelines, designers can unlock the full potential of Renesas GaN devices to build high-efficient, high-power-density converters suited for demanding applications.

Contents

Figures

1. Drive Circuit Configurations

Renesas High-Voltage GaN devices are high-performance, normally-off devices that do not need a negative gate drive voltage like other wideband gap switch technologies. This makes it easier to implement simple and conventional gate drive circuits using just a gate resistor and a diode.

- Gate resistors (Rg) – A gate resistor (Rg) is essential for all switching devices to control the switching speed of a device. The value of Rg should be optimized based on the desired slew rate, voltage overshoot, and electromagnetic interference (EMI) considerations to ensure reliable operation and minimize switching noise.
- Schottky diodes – Used to direct current through different resistors during turn-on and turn-off events, enabling separate control of turn and turn off slew rates and typical use fast switching diode minimum 300mA forward continuous current.

Figure 1 shows three common drive circuit configurations:

- Figure 1(a) shows a single resistor controlling both the turn on and turn off slew rates.
- Figure 1(b) shows a configuration where separate resistors are used to tune the turn-on and turn-off slew rates. A separation in turn-on and turn-off slew rate setting is achieved by using a Schottky diode to control the direction of the gate current.
- Figure 1(c) shows a configuration that can be implemented with a gate driver which provides separate source and sink outputs. This allows the use of dedicated R_{GON} and R_{GOFF} to independently control rise and fall slew rates to optimize system performance.

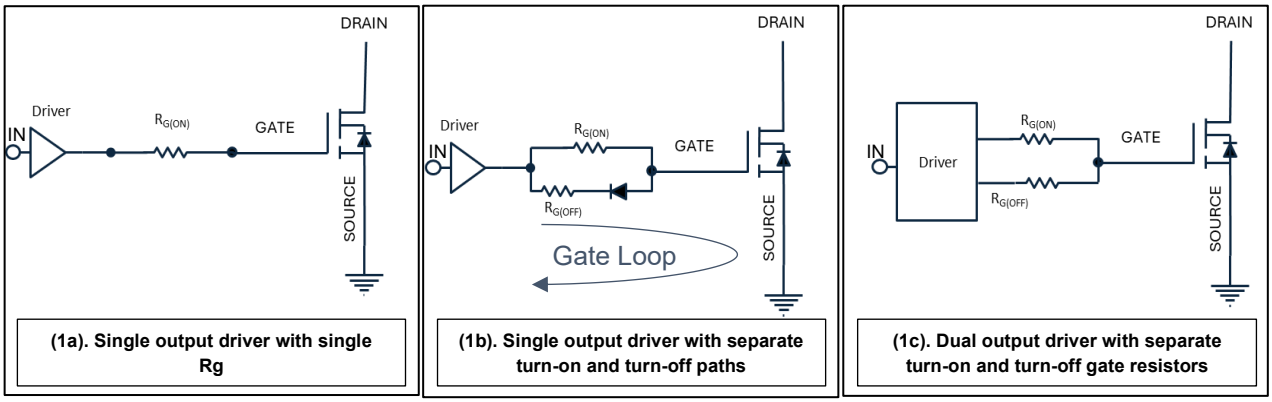

Figure 1. Driving Circuit Configurations

2. Critical Component Placement

In GaN-based power converter designs, precise placement of critical components is essential to fully leveraging the fast-switching capabilities of GaN devices while minimizing parasitic effects that can degrade performance or cause reliability issues. Here are key considerations:

- In Figure 1(a) single driver with single Rg configuration, the drain of the GaN switch must be intricately connected to the inductor or transformer terminal.
- In Figure 1(b), place the gate driver as closed as possible to the GaN device to minimize the gate loop inductance and delay.

3. PCB Layout for Low Inductance Design

Due to fast switching nature of GaN devices, minimizing parasitic inductance in the PCB layout is critical to ensuring reliable operation, reducing EMI, and maximizing efficiency (for more information on layout guidelines, see Figure 4). Key strategies include the following:

- Create source shield planes on the layer immediately below the gate driver connected to source or the kelvin source, when available.
- Ensure the source shield plane covers the gate and source terminals (kelvin source if available) and all the gate circuitry components.
- Power loop between high side and low side of a GaN device and the DC bus decoupling capacitor should be as close as possible.
- Use tight component placement and short, wide traces to reduce loop inductance.
- Use a solid ground plane under the half bridge to create a low-inductance return path for switching currents and use flux cancellation techniques.
- Avoid split planes under high-speed switching sections.
- For half-bridge and full-bridge configuration, keep symmetry to balance current paths and reduce EMI.

4. Validation and Optimization of Design Through Switching Test

To ensure robust operation and to suppress unwanted oscillations, it is essential to evaluate the drain-source voltage (V_{DS}) switching waveforms at both turn-on and turn-off transitions under the most demanding dynamic conditions (that is, typically at the highest expected load current as specified in the GaN device datasheet).

A Double Pulse Test (DPT) performed on the final PCB layout is strongly recommended to capture the influence of layout-dependent parasitic. The V_{DS} waveform should be carefully analyzed for overshoot, ringing, and damping behavior at each switching edge. Proper high-bandwidth test equipment and probing techniques are highly recommended to ensure signal integrity of captured waveforms.

To optimize the trade-off between switching efficiency and waveform integrity, the gate resistor (Rg) should be empirically adjusted based on test results. This tuning directly affects the gate-drive slew rate, which in turn influences switching losses, voltage stress, and EMI performance. The process should begin with the gate resistance recommended in the device datasheet and be iteratively increased or decreased to match the specific parasitic characteristics of the PCB layout and system topology.

5. Solutions to Suppress Oscillation

Wide-bandgap semiconductors such as Gallium Nitride (GaN) and Silicon Carbide (SiC) have enabled significant advancements in high-voltage power conversion, offering faster switching speeds, higher efficiency, and increased power density. However, these benefits come with increased sensitivity to parasitic elements, particularly those introduced by PCB layout.

5.1 Root Causes of Oscillation

Oscillations typically arise from parasitic inductance and capacitance in the power and gate drive loops. Suboptimal PCB layout – characterized by large loop areas, poor return path integrity, and insufficient decoupling – can amplify these effects. Fast switching transitions in wide bandgap (WBG) devices generate high dv/dt and di/dt, which interact with parasitics to produce voltage overshoot, ringing, and potential EMI issues.

5.2 Circuit-Level Mitigation Techniques

When layout optimization alone is insufficient, circuit-level mitigation becomes essential. One of the most effective techniques is the use of snubber networks across the drain-source terminals of the switching device. These networks absorb resonant energy and clamp voltage overshoot, reducing ringing and improving waveform integrity. Snubber design should be tailored to the switching frequency, device characteristics, and parasitic profile of the layout.

These mitigation strategies are applicable across Si, SiC, and enhancement-mode GaN devices. However, due to the ultra-fast switching speeds of wide-bandgap devices, GaN and SiC require more stringent layout and validation practices.

5.3 Validation Through Empirical Testing

All mitigation techniques must be validated through rigorous empirical testing. The Double Pulse Test (DPT) is a widely accepted method for characterizing switching behavior under worst-case conditions. This test should be conducted on the final PCB layout to capture layout-dependent parasitic effects. Key parameters to evaluate include:

- Voltage overshoot and ringing on the drain-source waveform
- Damping behavior across switching transitions
- Required slew rate to pass EMI regulations

5.4 Design Principles for Oscillation Suppression

Switched mode power supplies have always had to use mitigation techniques for voltage oscillations caused by high dv/dt and system parasitic. To effectively suppress oscillation, designers should adopt a holistic approach that includes:

- Minimizing noise generation through optimized component placement and trace routing
- Reducing noise feedback by ensuring clean return paths and proper grounding
- Damping residual energy using R-C or RCD snubbers, ferrite beads, or resistive elements where appropriate

By combining an optimized PCB layout, targeted circuit-level mitigation, and thorough validation, designers can ensure stable, efficient, and reliable operation across the full operating envelope of the power system.

6. Design Example

6.1 Drive Circuit Configuration

As shown in Figure 2, a half-bridge topology is implemented using Renesas GaN devices, specifically the TP65H030G4PRS. In this setup, two GaN devices – QA (high-side) and QB (low-side) – form the half-bridge structure. Gate resistors of 30Ω and 15Ω are used for turn-on and turn-off control on the high-side and low-side devices, respectively. However, R_{GOFF} and the diode are marked as DNP (Do Not Populate) as shown in the reference markings below. For the Double Pulse Test (DPT), a single R_{GON} resistor is used to control both turn-on and turn-off transitions. This design leverages the high switching speed of GaN technology, enabling performance evaluation under practical conditions and achieving a high slew rate.

For detailed validation and optimization of switching performance, see section 7.

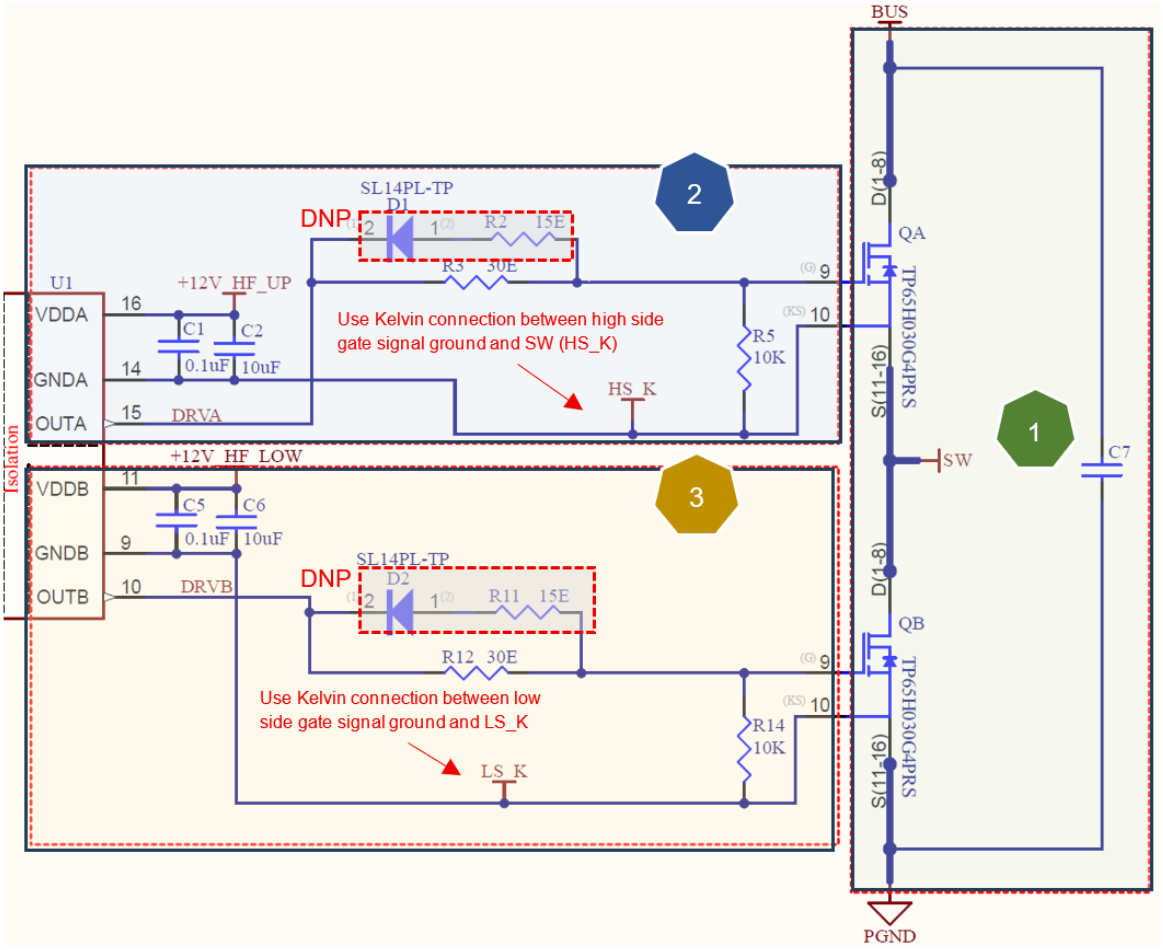

Figure 2. Drive Circuit Configuration

6.2 Critical Component Placement

Figure 3 shows a half-bridge GaN daughter card. At item 1, the highlighted area indicates the switching paths of GaN devices QA and QB. These devices are closely spaced and symmetrically arranged to minimize parasitic inductance – an essential design consideration for reducing voltage overshoot and enhancing switching efficiency.

Decoupling capacitors (C7) placed near the power devices provide an excellent low-inductance power loop.

Items 2 and 3 emphasize the optimized placement of gate drive components, ensuring they are positioned as close as possible to the GaN devices. This proximity minimizes gate loop inductance, which improves switching speed and reduces gate ringing.

Overall, the thoughtful placement of components contributes to maintaining signal integrity, reducing EMI, and ensuring reliable high-speed switching operation.

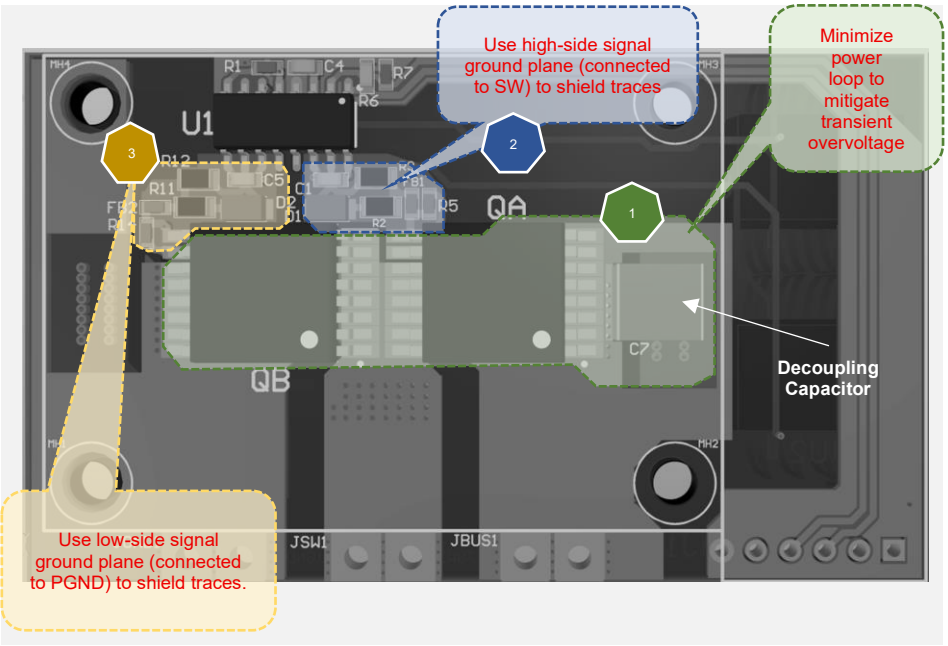

Figure 3. Critical Component Placement

6.3 Layout Guidelines

Renesas High-Voltage GaN devices offer very low output capacitance and enable high-speed switching with high dv/dt, resulting in minimal switching losses. To maintain these low losses, it is critical to avoid adding extra capacitance at the switch node.

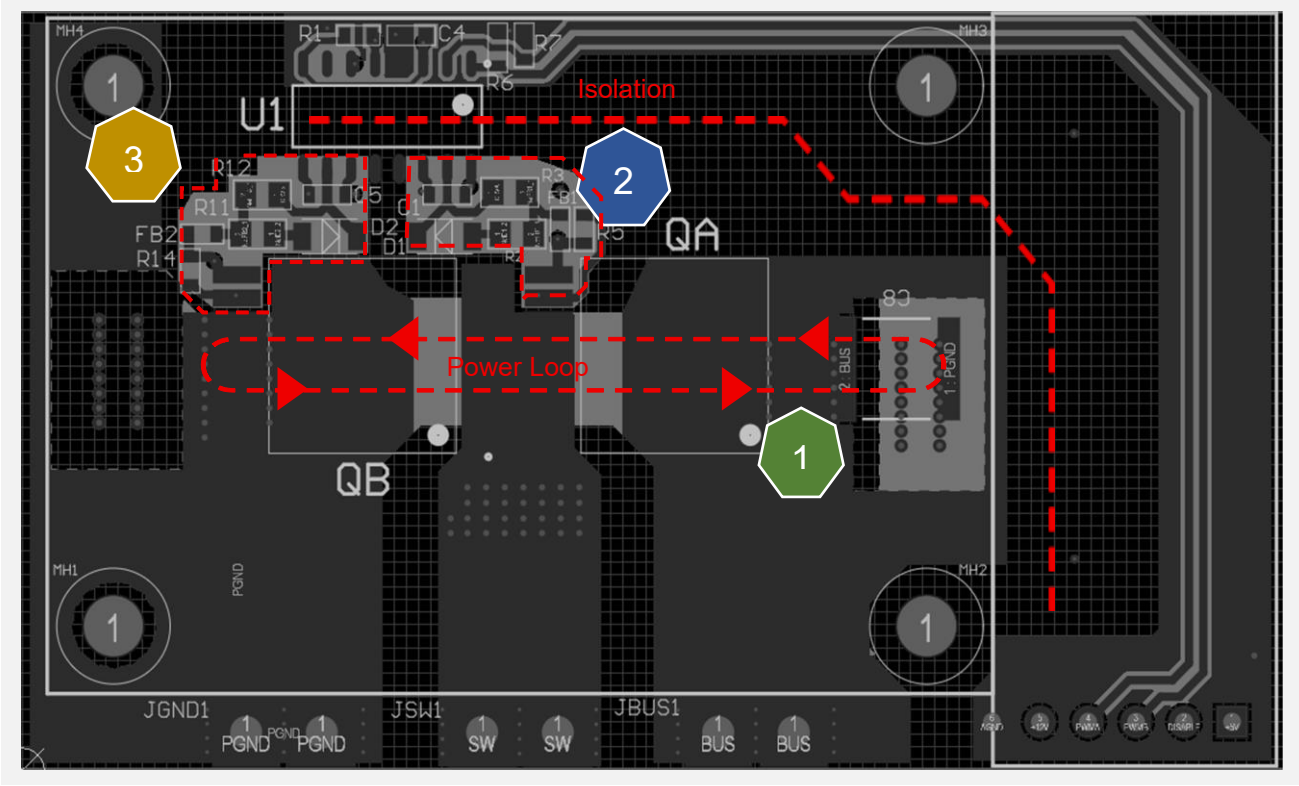

Figure 4. Top (Dark Gray and Mid-Two Layers (Light Gray)

Key layout practices include:

Compact Power Loop: Figure 4 and Figure 5 show a half-bridge GaN daughter card. In Figure 4, item 1 highlighted the power loop is highlighted with a red dotted ellipse. The loop is designed to be compact and symmetrical to minimize parasitic inductance, reducing voltage spikes, and improving switching efficiency. A solid ground plane on the mid 2 layer (light gray) placed right under the half bridge and the decoupling capacitor providing an extremely low impedance return path for high di/dt currents.

In Figure 4, items 2 and 3 emphasize the separation of power and gate signal return paths, along with the provision of a dedicated ground shielding plane beneath the gate driver and associated components. This ensures a low-impedance return path, effectively eliminating common-source inductance, enhancing signal integrity, and reducing electromagnetic interference.

Overall, the PCB layout emphasizes minimizing loop areas in both power and gate-drive paths, reducing parasitic elements, and ensuring robust, high-efficiency electrical performance for reliable high-frequency GaN operation.

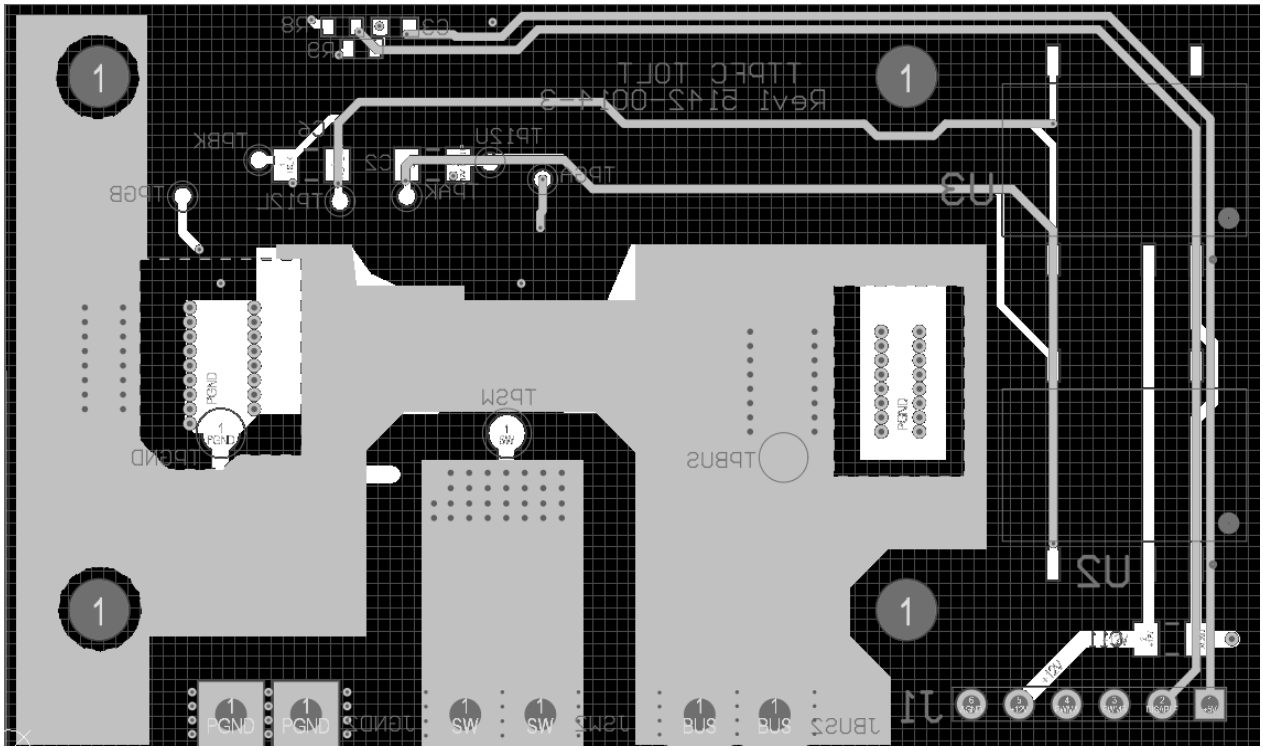

Figure 5. Mid-Three (Light Gray) and Bottom Layers (White)

7. Validation and Optimization of Design Through Switching Test Results

Figure 6 shows a standard Double Pulse Test (DPT) setup, commonly used to evaluate the switching performance of power devices under realistic operating conditions. In this configuration, only a 30Ω gate resistor (R12) was used to control both turn-on and turn-off of the DUT, demonstrating the simplicity of driving TP65H030G4PRS.

Figure 7 presents the captured waveforms, including V_{DS_QB} which represents the drain-to-source voltage, the inductor current (I_L), and V_{DS_QB} which represents the gate-to-source voltage. These waveforms provide critical insight into the switching behavior and performance of the GaN device during operation.

At a load current of 30A, the GaN device demonstrated fast and clean switching behavior, achieving voltage slew rates of 100 V/ns during turn-on (Figure 8) and 66V/ns during turn-off (Figure 9) without the need for circuit level overshoot or ringing mitigation techniques.

The switching waveforms demonstrate clean transitions with minimal overshoot and undershoot during both events, indicating effective control of switching dynamics and low parasitic interference. For more information, see the switching waveforms shown below.

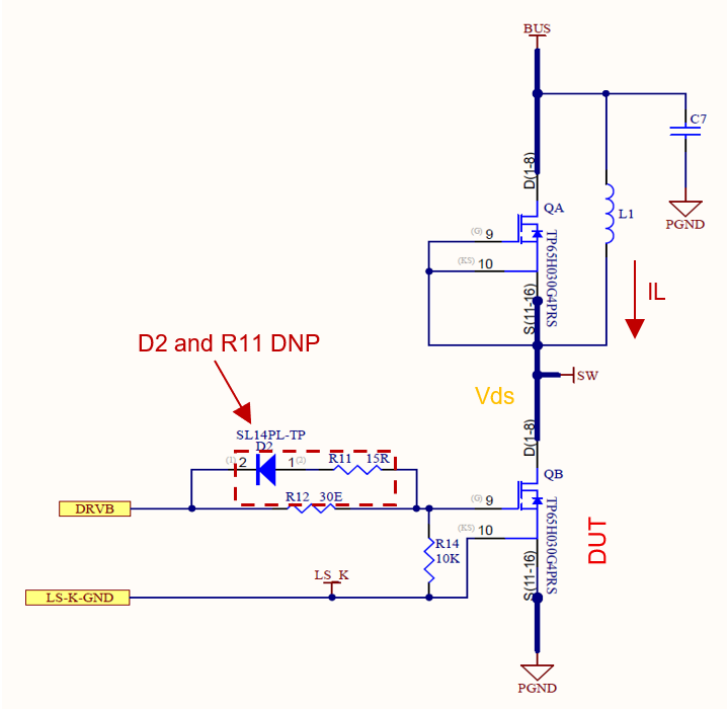

Figure 6. Double Pulse Test Setup

7.1 Double Pulse Switching Test Waveform Example

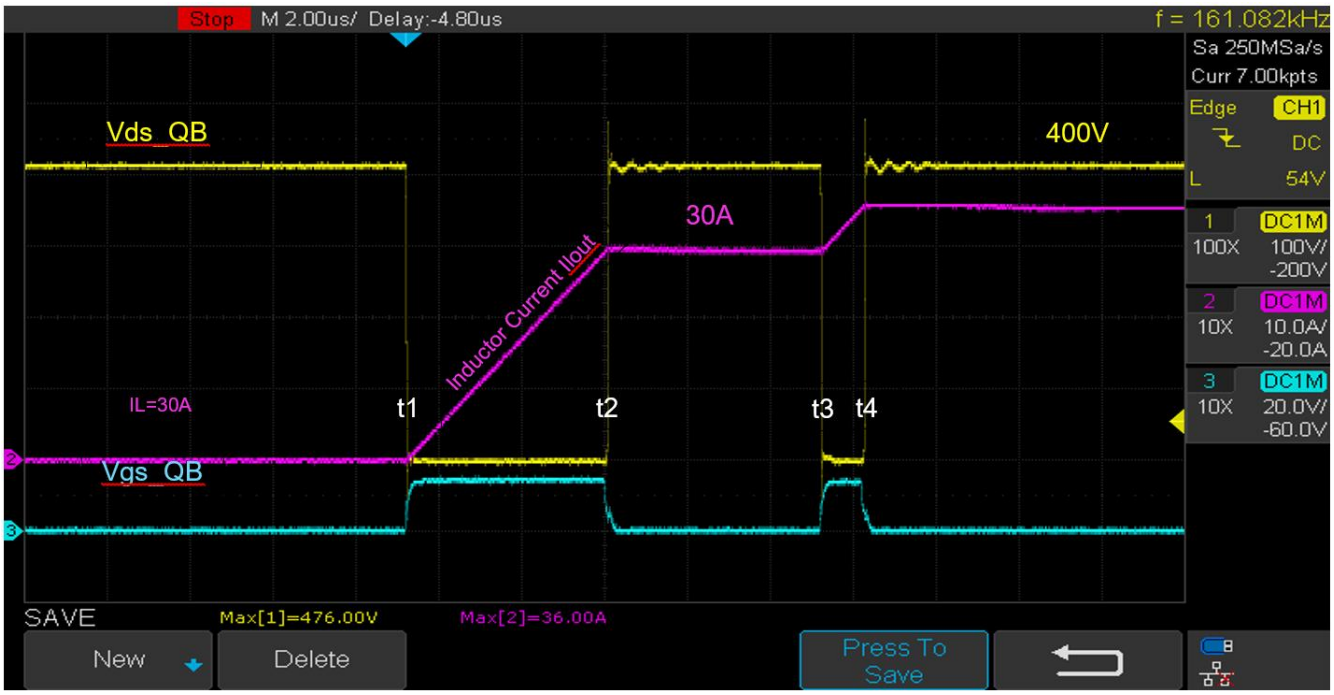

Figure 7. V_{ds} = 400V, I_d = 30A, $R_{g\ (R12)}$ = 30Ω

T1: Turn ON – Charge inductor to 30A.

T2: Turn OFF – Inductor current freewheels in QA; measure dv/dt and t_rise.

T3: Turn ON – Measure dv/dt and t_fall.

T4: Turn OFF – End of cycle.

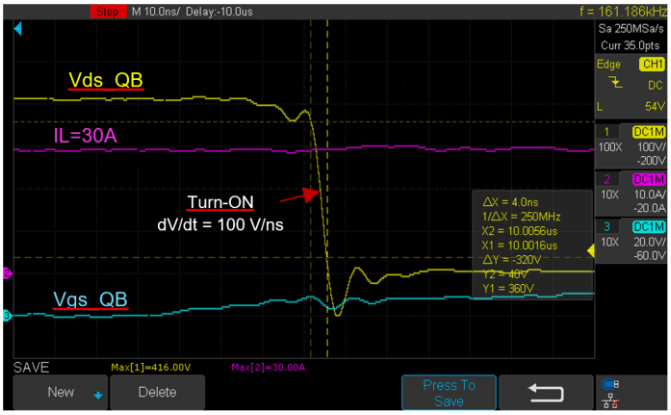

Figure 8. V_{ds} = 400V, I_d = 30A, $R_{g\ (R12)}$ = 30Ω Hard Switching Turn-On

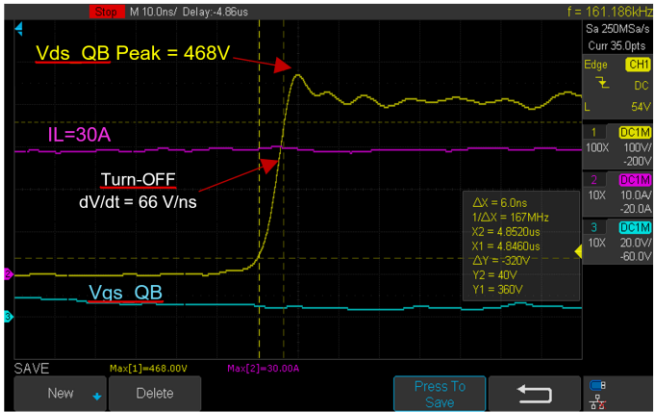

Figure 9. V_{ds} = 400V, I_d = 30A, $R_{g\ (R12)}$ = 30Ω Hard Switching Turn-Off

8. Conclusion

Realizing the fast-switching and high-efficiency performance of Renesas High-Voltage GaN devices requires attention to design details and careful test methodologies. This document discussed recommended design steps and presented results from a key characterization technique – the Double Pulse Switching Test. These insights enable power electronics engineers to precisely evaluate GaN device behavior and design power systems that deliver superior efficiency and differentiated performance.

The Renesas High-Voltage GaN solution implements a half-bridge configuration using TP65H030G4PRS GaN devices, achieving exceptional switching speeds through optimized gate resistance and carefully engineered PCB layout practices. Critical design considerations – such as minimizing power loop dimensions, positioning gate driver components close to the GaN devices, and incorporating ground shielding – significantly reduce parasitic inductance and EMI, thereby improving overall system reliability.

Double Pulse Testing validates these design principles by demonstrating rapid switching transitions with high slew rates and minimal waveform distortion, confirming suitability for high-frequency power conversion applications. Additionally, Renesas GaN devices exhibit clean and fast V_{DS_QB} waveforms without requiring supplemental components such as ferrite beads or snubbers, provided the recommended design rules and methods outlined in this document are followed.

9. Revision History

Revision	Date	Description
1.00	Dec 2, 2025	Initial release.

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