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1 Purpose of Document

This document summarizes the changes between the previous ASI4U silicon revision C and the current silicon revision E. These include requested UART design changes. The purpose of the redesign was to correct reported timing errors by the UART in the following modes: Master, Monitor, and Repeater. A problem with slave communication in special network constellations was also fixed.

2 Indication of the *End_Bit* Transmission Error

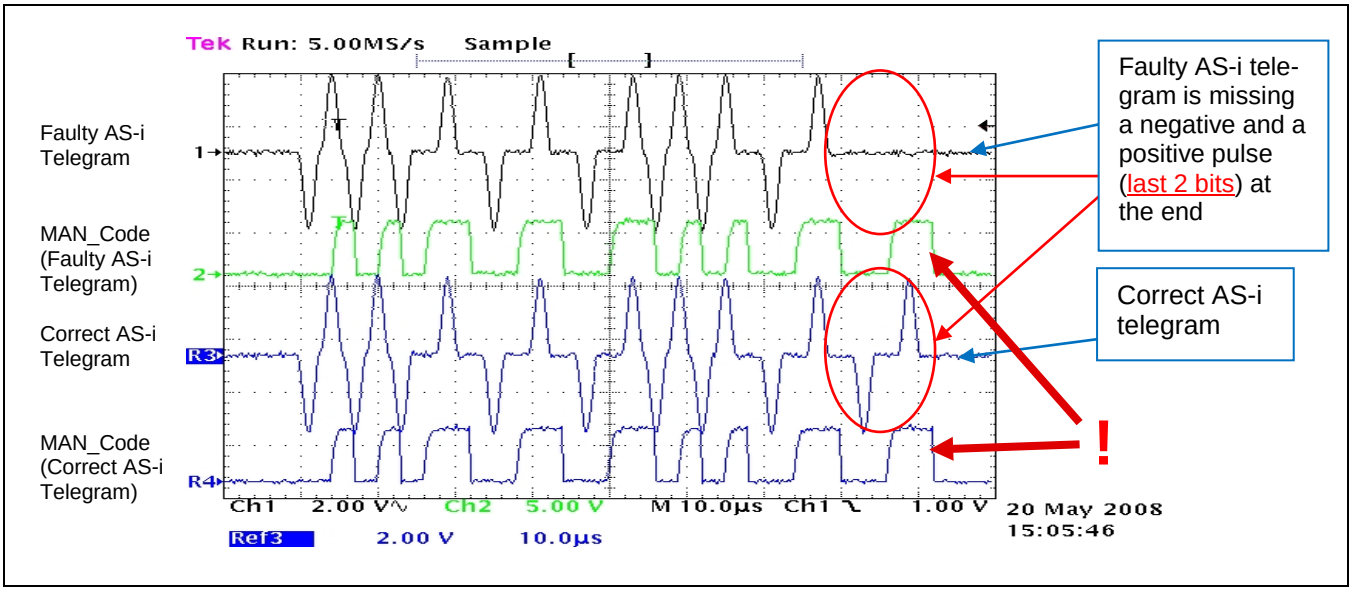
2.1. Problem Description

If the ASI4U revision C operates in Master Mode, Monitor Mode or Repeater Mode, the error signaling for an *End_Bit_Error* does not work correctly. In some special cases, the generated MAN-Code of a signal with an *End_Bit _Error* looks similar to the MAN-Code of a signal without any errors as demonstrated in Figure 2.1.

This malfunction of the ASI4U revision C results in an MAN-coded output signal that does not allow distinction between correct AS-I pulse sequences and pulse sequences that are shortened (missing one negative and one positive pulse). It occurs only under the following conditions:

- The parity of the signal is even.
- The last bit of the corrupt telegram is equal to binary 1.
- The *Stop_Bit* and the *Parity_Bit* or the *Start_Bit* and the *Control_Bit* are missing.
- If the *Start_Bit* and the *Control_Bit* are missing, the first pulse must have a negative polarity.

Figure 2.1 Comparison of Valid MAN-Code Signal to Faulty MAN-Code Signal



2.2. Design Corrections in the UART

The following changes in the UART block were implemented in ASI4U silicon revision E:

1. The last pulse of the MAN-coded LED1 output signal is now always kept in ACTIVE state for 9µs if an ASI telegram with an *Endbit_error* is received.

   The polarity of the ACTIVE State depends on the signal setting at the DI ports in Master Mode, Monitor Mode, and Repeater Mode. If DI2 and DI3 are driven by equal input signals, the MAN output signal at LED1 is configured ACTIVE LOW. If DI2 and DI3 are driven by unequal input signals, LED1 becomes inverted and is configured ACTIVE HIGH.

   Since a 9µs-wide MAN pulse is an out-of-specification event for the AS-I MAN signal, it will allow the connected microcontroller to recognize the error in the AS-I pulse signal on the AS-I line.

2. The internal computation of *No_info_error, Timing_error* and *Length_error* was reviewed and corrected to comply with the *AS-I Complete Specification V3.0*. The mapping of the *Length_error* signal was changed from DO0 to DO1 to comply with the *ASI4U Data Sheet*. The DO error signals are now always cleared at the beginning of new ASI and IRD telegrams in Monitor Mode.

3 Master Pause Detection in Slave Mode

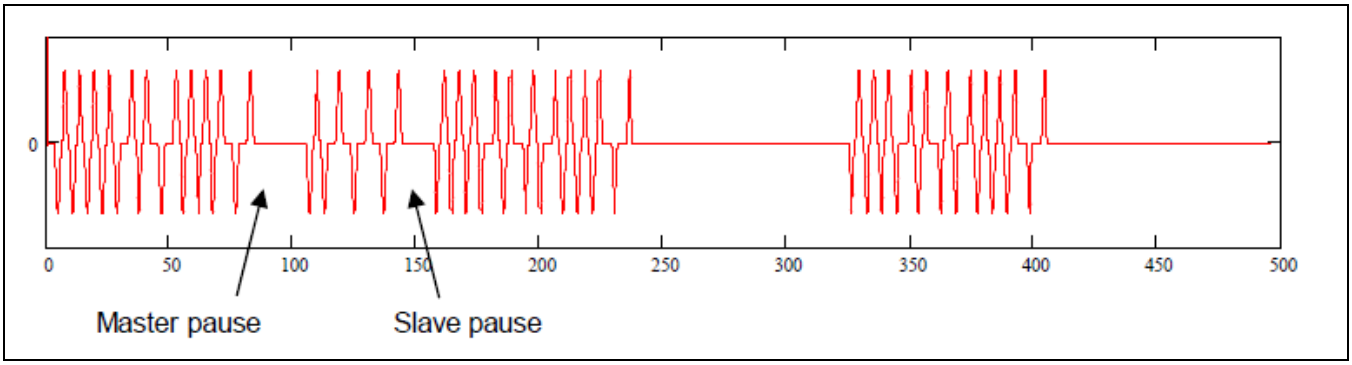
3.1. Problem Description

If the previous ASI4U revision C is operated in Slave Mode, the UART Master Pause detection does not always function correctly when the UART must listen to slave responses from a different slave. Depending on the actual AS-I line pulse timing, a slave response from a different slave is sometimes not recognized correctly, which results in a UART communication error. This prevents the Slave from understanding the next Master telegram correctly. If the Master telegram addresses the Slave itself, the error leads to a missing slave response and the Slave replies on a second repetition of the Master Call to its own address in asynchronous mode.

This behavior was mostly observed in mixed networks that used modules with the ASI4U, SAP5, and SAP4.1.

Figure 3.1 shows a telegram test case to reproduce the error. The AS-I signals shown in Figure 3.1 were generated by a signal generator that allowed sweeping the Master Pause and Slave Pause duration over the allowed specification limit. The first Master Call contains a different slave address than the tested slave. The second and third master calls address the tested slave. The tested slave replied with the erroneous behavior for certain Master pause and Slave pause scenarios only. The majority of the test cases were passed without error.

Figure 3.1 Test for ASI4U Revision C Error in Master Pause Detection



3.2. Design Correction

A new principle of AS-i telegram pause detection was implemented in ASI4U silicon revision E that is more precise and able to cover all valid timing scenarios for Master and Slave pauses. The new principle is now independent of the internal timing constraints of the UART state machine.

4 Related Documents

Document
ASI4U/ASI4U-E/ASI4U-F Feature Sheet
ASI4U/ASI4U-E/ASI4U-F Data Sheet
ASI4U/ASI4U-E Errata Sheet

Visit the ASI4U product page www.IDT.com/ASI4U or contact your nearest sales office for the latest version of these documents.

5 Document Revision History

Revision	Date	Description
1.10	October 20, 2011	Previous release.
1.11	January 30, 2015	Update for template. Minor edits for clarity. Addition of “Related Documents” section.
	April 13, 2016	Changed to IDT branding.

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