

TP65H020G4PLSGBD

650V SuperGaN® GaN FET in PQFN 8x8 Dual Side Cooled Package (Source Tab)

Description

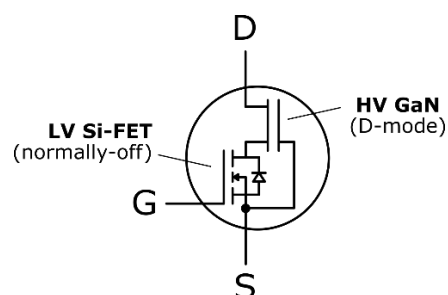
The TP65H020G4PLSGBD 650V, 20mΩ Gallium Nitride (GaN) FET is a normally-off switch that uses Renesas' Gen IV Plus platform. It combines a high-voltage depletion-mode GaN HEMT for high switching speed and high reliability with a low-voltage silicon MOSFET for normally-off operations and compatibility with standard drivers.

It is packaged in a thin QFN package with double-side cooling for superior thermal performance and highest power density.

Benefits

- Compatible with standard silicon drivers and E-mode gate drivers
- Enhanced noise immunity with no negative gate drive requirement
- High efficiency and high frequency in both hard- and soft-switched circuits
- Superior thermal performance
- Thin package for high power density applications.
- Facilitates cost-effective GaN adoption reducing system size, weight, and costs

Block Diagram



Features

- Insulated gate with high-threshold and high-gate margin
- Built-in freewheeling diode for low V_{sd} drop during deadtime
- Negligible reverse recovery charge
- Low Q_g and low Q_{oss}
- High dv/dt immunity
- Soft and hard-switching capability
- Transient overvoltage capability
- Dual-side cooled thin package
- JEDEC qualified
- RoHS compliant and Halogen-free packaging

Applications

- AI datacenter and telecom power supplies
- PV inverter
- UPS
- E-mobility charging
- BESS



Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$ (V) maximum	900
$R_{DS(on)}$ (mΩ) typical	20
Q_{OSS} (nC) typical	221
Q_g (nC) typical	19.6

1. Specifications

1.1 Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$ unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Unit	Test Condition
VDSS	Drain to source voltage	-	650	V	$V_{GS}=0V$, test as per as per JEDEC11-A108
VDSS(TR)	Transient drain to source voltage	-	900		$V_{GS} = 0V$, $< 10\mu s$, cumulative $\leq 60s$ (6 million pulses)
VDSS(TR) , pulsed	Drain to source voltage, pulsed	-	750		$V_{GS} = 0V$, $< 1\mu s$, cumulative $\leq 10h$ (36 billion pulses)
VGSS	Gate to source voltage	-20	+20		-
PD	Maximum power dissipation	-	347	W	$T_c = 25^\circ\text{C}$
ID	Continuous drain current at $T_c = 25^\circ\text{C}$	-	92	A	$V_{GS} = 9V$, V_{DS} can be forward and reverse conduction
	Continuous drain current at $T_c = 100^\circ\text{C}$	-	58		
ID(PULSE)	Pulsed drain current at $T_c = 25^\circ\text{C}$	-	328		$V_{GS} = 9V$, pulse width= $10\mu s$ forward and reverse conduction
	Pulsed drain current at $T_c = 100^\circ\text{C}$	-	267		
ISD(PULSE)	Pulsed reverse drain current at $T_c = 25^\circ\text{C}$	-	328		$V_{GS}=0V$, pulse width= $10\mu s$, $V_{DS} < 0$
	Pulsed reverse drain current at $T_c = 100^\circ\text{C}$	-	267		
TJ	Operating temperature junction	-55	+150	$^\circ\text{C}$	-
TS	Storage temperature	-55	+150	$^\circ\text{C}$	Max shelf life depends on storage conditions
TSOLD	Reflow soldering temperature ^[1]	-	260	$^\circ\text{C}$	-

1. Reflow MSL3.

1.2 Recommended Operating Conditions

Symbol	Parameter		Minimum	Recommended	Maximum	Unit
VGS,off	Off-State Gate Voltage		-	0	0	V
VGS,on	On-State Gate Voltage		8	9	-	

1.3 Thermal Specifications

Symbol	Parameter	Typical Value	Unit	Test Condition
RθJC	Junction-to-case, top	0.36	$^\circ\text{C/W}$	-
RθJC	Junction-to-case, bottom	2.8		-
RθJA	Junction-to-ambient	53		Device on 40 mm * 40 mm * 1.5 mm epoxy PCB FR4 with 6 cm ² (one layer, 70 μm thickness) copper area for tab (source) connection and cooling. PCB is vertical without air stream cooling.

1.4 Electrical Specifications – Forward Device

$T_J = 25^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	$V_{GS} = 0V$	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 0.25\text{ mA}$	3.3	4	4.8	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	-	-	-6.8	-	mV/ $^\circ\text{C}$
$R_{DS(on)eff}$	Drain-source on-resistance	$V_{GS} = 9V$, $I_D = 20A$, $T_J = 25^\circ\text{C}$	-	20	25	m Ω
		$V_{GS} = 9V$, $I_D = 20A$, $T_J = 150^\circ\text{C}$	-	41	-	
I_{DSS}	Drain-to-source leakage current	$V_{DS} = 650V$, $V_{GS} = 0V$, $T_J = 25^\circ\text{C}$	-	2	10	μA
		$V_{DS} = 650V$, $V_{GS} = 0V$, $T_J = 150^\circ\text{C}$	-	20	-	
I_{GSS}	Gate-to-source forward leakage current ^[1]	$V_{GS} = 20V$	-	-	0.1	μA
	Gate-to-source reverse leakage current ^[1]	$V_{GS} = -20V$	-	-	-0.1	
C_{ISS}	Input capacitance	$V_{GS} = 0V$, $V_{DS} = 400V$, $f = 1\text{MHz}$	-	1439	-	pF
C_{OSS}	Output capacitance		-	196	-	
C_{RSS}	Reverse transfer capacitance		-	5.7	-	
$C_{O(er)}$	Output capacitance, energy related ^[2]	$V_{GS} = 0V$, $V_{DS} = 0V$ to $400V$	-	309	-	pF
$C_{O(tr)}$	Output capacitance, time related ^[3]		-	552	-	
Q_G	Total gate charge	$V_{DS} = 400V$, $V_{GS} = 0V$ to $9V$, $I_D = 20A$	-	19.6	-	nC
Q_{GS}	Gate-source charge		-	7.6	-	
Q_{GD}	Gate-drain charge		-	6.0	-	
Q_{OSS}	Output charge	$V_{GS} = 0V$, $V_{DS} = 0V$ to $400V$	-	221	-	nC
$t_{D(on)}$	Turn-on delay	$V_{DS} = 400V$, $V_{GS} = 0$ to $9V$, $R_{G(on)} = 20\Omega$, $R_{G(off)} = 2\Omega$, $I_D = 30A$ (see Figure 16)	-	46.4	-	ns
t_R	Rise time		-	9.4	-	
$t_{D(off)}$	Turn-off delay		-	15.5	-	
t_F	Fall time		-	8.8	-	

1. Equivalent capacitance to give same stored energy from 0V to 400V.

2. Equivalent capacitance to give same charging time from 0V to 400V.

1.5 Electrical Specifications – Reverse Device

$T_J = 25^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{SD}	Reverse voltage	$V_{GS} = 0V$, $I_S = 20A$	-	1.3	-	V
		$V_{GS} = 0V$, $I_S = 10A$	-	1.1	-	

1. Reverse recovery charge is negligible, and is enabled by the LV Si FET technology.

2. Revision History

Revision	Date	Description
1.00	Sep 11, 2026	Initial release.

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