

RRG5102X-B10

Gen-2 DDR5 Multiplexing Data Buffer (MDB)

Description

The RRG5102X-B10 is a DDR5 Multiplexing Data Buffer (MDB). Its primary function is to demultiplex and buffer data from the Host CPU to DRAMs.

The Host-side can operate as x4, with two strobes, or x8, with one. There are two separate DRAM interfaces, each of which can operate as x4 or x8.

The RRG5102X-B10 supports both Mux Mode and Rank Mode. In Mux Mode, the Host interface runs at twice the speed of the DRAM interfaces and carries up to two ranks for each of two multiplexed pseudo-channels, which can transmit and receive in the same direction simultaneously. In Rank Mode, the Host and DRAM interfaces run at the same speed, and up to four ranks are supported.

The RRG5102X-B10 also has an input-only control bus interface that is connected to a DDR5MRCD02, as well as a dedicated pin for ZQ Calibration and loopback outputs for test purposes.

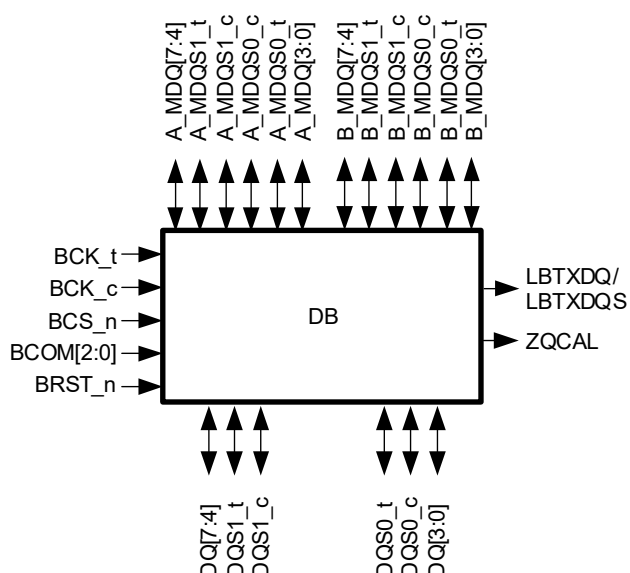
Applications

MRDIMM modules for Enterprise Servers

Features

- Pinout optimized MRDIMM PCB layout
- DDR5 Server speeds up to 12800 MT/s
- x4 or x8 operation on both Host and DRAM interfaces
- Rank and Mux Modes
- Supports up to 2 ranks per pseudo-channel in Mux Mode
- Supports up to 4 ranks in Rank Mode
- Link CRC
- Dual Frequency Contexts
- DFE/CTLE Self-Training mode
- Supports SDP, DDP, and 3DS DRAM types
- Provides access to internal control words for configuring device features and adapting to different MRDIMM and system applications
- Loopback and pass-through modes
- Training support features for DQ and MDQ interfaces

Block Diagram



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