

RRG5012X-A00

Gen-2 DDR5 Multiplexing Registering Clock Driver

Description

The RRG5012X-A00 is a second generation Multiplexing Registering Clock Driver (MRCD) used on DDR5 MRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the Host Controller and the DRAMs. It also creates a BCOM bus which controls the data buffers.

The RRG5012X-A00 contains two separate channels with some common logic such as clocking, but which otherwise operate independently of each other. For each channel, the Host interface is a 7-bit + parity/CRC CA bus with two chip-select inputs, running at single or double data rate and 1x or 2x the DRAM frequency.

Both Mux Mode and Rank Mode are supported. In Mux Mode, up to two ranks per each of two multiplexed pseudo-channels are supported, allowing simultaneous operation in the same direction. The RRG5012X-A00 demultiplexes the pseudo-channels and transmits each to a separate DRAM output interface. Rank Mode does not use pseudo-channels and operates as a four-rank LRDIMM.

Each DRAM interface is a 14-bit single data rate CA bus output with a chip-select. The RRG5012X-A00 also transcodes commands from the CA bus onto a per-channel BCOM bus for Data Buffer control.

The RRG5012X-A00 has a common clock input and PLL, but produces eight separate clock pairs to the DRAM channels.

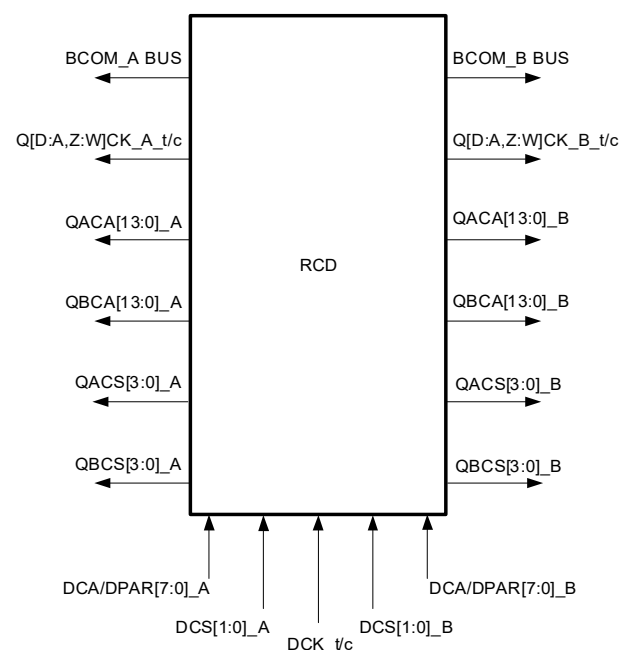
Applications

- MRDIMM modules for Enterprise Servers

Features

- DDR5 MRDIMM server speeds up to 12800MT/s
- Supports 1 or 2 ranks per pseudo-channel in both x4 and x8 Mux mode
- Supports up to 4 ranks in Rank Mode
- Supports SDP, DDP, 3DS DRAM types
- Provides access to internal control words for configuring device features and adapting to different system applications
- Link CRC protection and descrambling of DCA bus
- DfE/CTLE Self Training mode
- I²C/I³C Sideband access for asynchronous register access control
- BCOM data buffer control
- Loopback and pass-through modes
- Package: 8.7 × 14.4 mm, 264-FCBGA

Block Diagram



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