

FEATURES

HIGHLIGHTS

- Digital PLL locks to GPS or Ethernet physical layer clocks
- Provides clocks for 1 Gigabit and 10 Gigabit Ethernet, QSGMII and XAUI
- Internal Digitally Controlled Oscillator supports IEEE 1588 clocks generation
- Jitter generation <0.3ps RMS (10 kHz to 20 MHz), meets jitter requirements of leading PHYs supporting 10GBASE-R, QSGMII and XAUI

MAIN FEATURES

- Digital PLL synchronizes with GPS or Ethernet connected synchronization sources
- DPLL bandwidth is selectable to be 15 mHz or 1.2 Hz
- DPLL holdover accuracy is 1.1×10^{-5} ppm and instantaneous holdover accuracy is 4.4×10^{-8} ppm
- Input references are monitored for frequency offset and activity
- DPLL holdover, free run and hitless reference switching can be forced by the host processor or can be automatically controlled by an internal state machine

- Internal DCO has resolution of 0.01105 ppb and can be controlled by an external processor via I2C interface for IEEE 1588 clock generation
- Two Analog PLLs for jitter attenuation and frequency translation
- IN1, IN2 and IN3 accept single ended reference clocks whose frequencies can be 1PPS (1 Hz), 25 MHz, 125 MHz or 156.25 MHz
- OUT1 and OUT2 output differential clocks with frequencies of 125 MHz or 156.25 MHz
- OUT3 outputs a differential clock with frequency of 322.265625 MHz or 644.53125 MHz
- OUT4 outputs a free-running LVCMOS clock with frequency of 25 MHz

OTHER FEATURES

- I2C microprocessor interface mode
- IEEE 1149.1 JTAG Boundary Scan
- 1mm ball pitch CABGA green package

APPLICATIONS

- Industrial Automation
- Power Systems

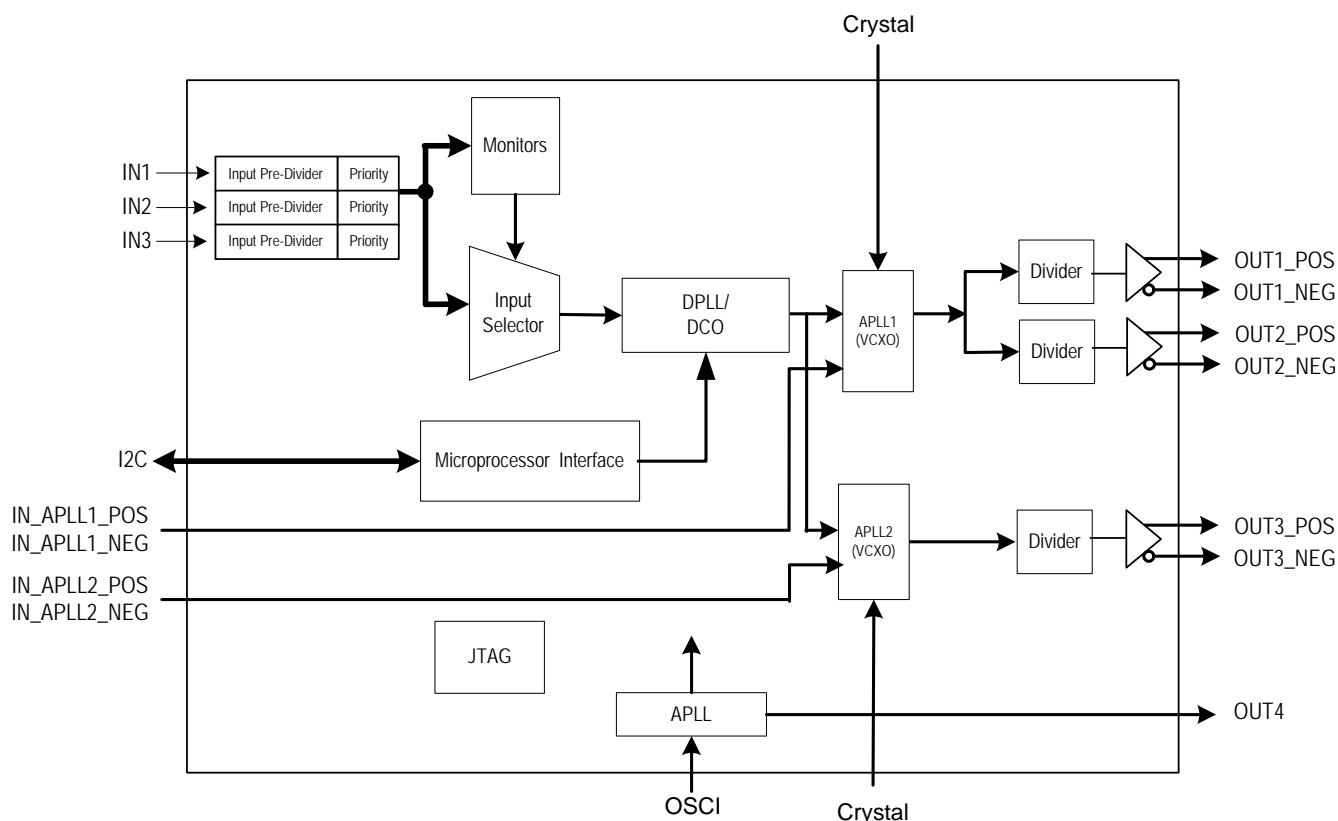


Figure 1. Functional Block Diagram

DESCRIPTION

The IDT8V89317 10G Ethernet PLL for Industrial Automation and Power Systems is used to synchronize equipment with synchronization sources using the Ethernet physical layer, or with a 1 PPS (1 Hz) GPS clock; it can also be used by external IEEE 1588 clock recovery servos to synthesize IEEE 1588 clocks. The IDT8V89317 ultra-low jitter output clocks can be used to directly synchronize 10GBASE-R Ethernet PHYs and XAUI or QSGMII devices.

The IDT8V89317 synchronization functions are provided by a Digital PLL (DPLL) with an embedded clock synthesizer. The DPLL accepts three single ended reference inputs that can operate at 1PPS (1 Hz), 25 MHz, 125 MHz or 156.25 MHz. The references are continually monitored for loss of signal and for frequency offset per user programmed thresholds. The active reference for the DPLL is determined by forced selection or by automatic selection based on user programmed priorities and locking allowances and based on the reference monitors.

The DPLL supports four primary operating modes: Free-Run, Locked, Holdover and Digitally Controlled Oscillator (DCO) Control. In Free-Run mode the DPLL generates a clock based on the master clock alone. In Locked mode the DPLL filters reference clock jitter with the selected bandwidth. In Locked mode the long-term DPLL frequency accuracy is the same as the long term frequency accuracy of the selected input reference. In Holdover mode the DPLL uses frequency data acquired while in Locked mode to generate accurate frequencies when input references are not available. In DCO Control Mode the DPLL control loop is opened and the DCO can be used by an algorithm (e.g. IEEE 1588 clock servo) running on an external processor to synthesize clock signals.

The IDT8V89317 requires a 12.8 MHz master clock for its reference monitors and other digital circuitry. The frequency accuracy of the master clock determines the frequency accuracy of the DPLL in Free-Run mode. The frequency stability of the master clock determines the frequency stability of the DPLL in Free-Run mode and in Holdover mode. The master clock must be sufficiently stable to support the selected DPLL filtering bandwidth; in particular, the 15 mHz bandwidth requires a very stable temperature compensated crystal oscillator (TCXO) or ovenized crystal oscillator (OCXO). Refer to the IDT application note "Recommended Crystal Oscillators for IDT's Network Synchronization WAN-PLL™" for guidance.

The DPLL can be configured with a filtering bandwidth of 15 mHz or 1.2 Hz. The 15 mHz bandwidth can be used to lock the DPLL directly to a 1 pulse per second (PPS) reference. 1.2 Hz bandwidth can be used to lock to Ethernet connected synchronization sources operating at 25 MHz, 125 MHz or 156.25 MHz.

The clock synthesized by the IDT8V89317 DPLL is passed through two independent voltage controlled crystal oscillator (VCXO) based jitter attenuating analog PLLs (APLLs). The APLLs drive independent dividers that have differential outputs. The APLLs use external crystal resonators with resonant frequencies equal to the APLL base frequency divided by 25. The output clocks generated by the APLLs exhibit jitter below 0.30ps RMS over the integration range 10 kHz to 20 MHz.

The IDT8V89317 generates a 25 MHz single ended output that is based on the free running 12.8 MHz master clock. The frequency accuracy and the frequency stability of this 25 MHz clock are determined by the master clock.

1 PIN ASSIGNMENT

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	IC1	VDDA	XTAL1_IN	CAP1	IN_APLL1_NEG	IC1	IC1	TDI	IC1	IC2	OSCI	TMS	IC1	TRST	A
B	IC1	VSSA	XTAL1_OUT	VSSA	IN_APLL1_POS	IC1	IC1	TDO	VSSA	TCK	VSSA	VSSA	VSSDO	VDDDO	B
C	IC1	VDDA	NC	CAP2	IC1	IC1	VDDDO	VSSDO	VDDA	VSSA	VDDA	VDDA	INT_REQ	IC1	C
D	VSSA	VSSA	CAP3	VSSA	VDDA	IC1	VSSD	VDDD	IC1	VDDA	VSSA	VDDA	IC1	IC1	D
E	IC1	IC1	VSSA	VSSA	VSSA	IC3	VSSD	VDDD	IC1	VSSA	VDDA	VSSA	IC1	IC1	E
F	VDDD	VSSD	VSSA	VSSA	VDDA	VSSA	VSSD	VDDD	VSSD	VDDD	IC1	VDDDO	OUT4	VSSDO	F
G	VSSD	VDDD	VSSA	VSSA	VSSA	VSSD	VDDD	IC1	VDDD	VSSD	IC1	IC1	IC1	IC1	G
H	VDDAO	VSSAO	VDDAO	VSSAO	VSSAO	VSSAO	VSSD	VDDD	VSSD	VDDD	IC1	IC1	RST	IN1	H
J	OUT1_NEG	OUT1_POS	VDDAO	VSSAO	VDDAO	VSSAO	VDDAO	VSSA	VSSA	VDDA	DPLL_LOCK	IC1	IN2	IN3	J
K	VSSAO	VSSAO	VSSAO	VDDAO	VSSAO	VDDAO	VSSAO	VSSD	VDDD	VSSD	IC1	IC1	I2C_SCL	I2C_SDA	K
L	OUT2_NEG	OUT2_POS	VDDAO	VSSAO	VSSAO	VSSAO	VSSAO	I2C_AD1	I2C_AD2	CAP4	VSSA	CAP5	VSSA	CAP6	L
M	VDDAO	VSSAO	VSSAO	VSSAO	VDDAO	VSSAO	VDDAO	VSSA	VSSA	VSSA	VSSA	NC	IC	IC	M
N	VSSAO	OUT3_POS	VSSAO	IC1	VSSAO	IN_APLL2_POS	IC2	IC2	VSSA	XTAL2_OUT	VSSA	IC1	VSSA	VSSA	N
P	VDDAO	OUT3_NEG	VSSAO	IC1	VDDAO	IN_APLL2_NEG	IC2	IC2	VDDA	XTAL2_IN	VDDA	IC1	IC1	VDDA	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
Key:															
	Diff Outputs	Outputs	Inputs	Power	Ground										

Figure 2. Pin Assignment (Top View)

2 PIN DESCRIPTION

Table 1: Pin Description

Name	Pin No.	I/O	Type	Description ¹
Global Control Signal				
OSCI	A11	I	CMOS	OSCI: Crystal Oscillator Master Clock A nominal 12.8000 MHz clock provided by a crystal oscillator is input on this pin. It is the master clock for the device.
RST	H13	I pull-up	CMOS	RST: Reset A low pulse of at least 50 μ s on this pin resets the device. After this pin is high, the device will still be held in reset state for 500 ms (typical).
Input Clock				
IN1	H14	I pull-down	CMOS	IN1: Input Clock 1 Either a 1 PPS, 25 MHz, 125 MHz or 156.25 MHz is input on this pin.
IN2	J13	I pull-down	CMOS	IN2: Input Clock 2 Either a 1 PPS, 25 MHz, 125 MHz or 156.25 MHz is input on this pin.
IN3	J14	I pull-down	CMOS	IN3: Input Clock 3 Either a 1 PPS, 25 MHz, 125 MHz or 156.25 MHz is input on this pin.
IN_APLL1_POS IN_APLL1_NEG	B5 A5	I pull-down I pull-up/ pull-down	LVPECL/ LVDS	IN_APLL1_POS / IN_APLL1_NEG: Input Clock to APLL1 Direct input clock to APLL1.
IN_APLL2_POS IN_APLL2_NEG	N6 P6	I pull-down I pull-up/ pull-down	LVPECL/ LVDS	IN_APLL2_POS / IN_APLL2_NEG: Input Clock APLL2 Direct input clock to APLL2.
Output Clock				
OUT1_POS OUT1_NEG	J2 J1	O	LVPECL	OUT1_POS / OUT1_NEG: Positive / Negative Output Clock 1 A clock is differentially output on this pair of pins. It outputs either 125 MHz or 156.25 MHz
OUT2_POS OUT2_NEG	L2 L1	O	LVPECL	OUT2_POS / OUT2_NEG: Positive / Negative Output Clock 2 A clock is differentially output on this pair of pins. It outputs either 125 MHz or 156.25 MHz
OUT3_POS OUT3_NEG	N2 P2	O	LVPECL	OUT3_POS / OUT3_NEG: Positive / Negative Output Clock 3 A clock is differentially output on this pair of pins. It outputs 322.265625 MHz or 644.53125 MHz
OUT4	F13	O	CMOS	OUT4: CMOS Output Clock 4 A free run 25 MHz clock is output on this pin.
Miscellaneous				
CAP1, CAP2, CAP3, CAP4, CAP5, CAP6	A4, C4, D3, L10, L12, L14	Output	Analog	CAP1 ~ CAP6: Analog Power Filter Capacitor connection 1 to 6 Connect a 10 μ F capacitor in parallel with a low ESR 100 nF capacitor between these pins and VSS1
XTAL1_IN	A3	Input	Analog	Crystal 1 oscillator input. Crystal oscillator input for APLL.
XTAL1_OUT	B3	Output	Analog	Crystal 1 oscillator output. Crystal oscillator output for APLL.
XTAL2_IN	P10	Input	Analog	Crystal 2 oscillator input. Crystal oscillator input for APLL.
XTAL2_OUT	N10	Output	Analog	Crystal 2 oscillator output. Crystal oscillator output for APLL.
Lock Indication Signals				

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description ¹
DPLL_LOCK	J11	O	CMOS	DPLL lock indicator. This pin goes high when DPLL is locked.
Microprocessor Interface				
INT_REQ	C13	O	CMOS	INT_REQ: Interrupt Request This pin is used as an interrupt request. The output characteristics are determined by the HZ_EN bit (b1, 0CH) and the INT_POL bit (b0, 0CH).
I2C_SCL	K13	I	Open Drain	I2C_SCL: Serial Clock Line In I2C mode, the serial clock is input on this pin.
I2C_SDA	K14	I/O	Open Drain	I2C_SDA: Serial Data Input/Output In I2C mode, this pin is used as the input/output for the serial data.
I2C_AD1	L8	I pull-up	CMOS	I2C_AD1: Device Address Bit 1 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
I2C_AD2	L9	I pull-up	CMOS	I2C_AD2: Device Address Bit 2 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
JTAG (per IEEE 1149.1)				
TRST	A14	I pull-down	CMOS	TRST: JTAG Test Reset (Active Low) A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.
TMS	A12	I pull-up	CMOS	TMS: JTAG Test Mode Select The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.
TCK	B10	I pull-down	CMOS	TCK: JTAG Test Clock The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.
TDI	A8	I pull-up	CMOS	TDI: JTAG Test Data Input The test data is input on this pin. It is clocked into the device on the rising edge of TCK.
TDO	B8	O	CMOS	TDO: JTAG Test Data Output The test data is output on this pin. It is clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning. This pin can indicate the interrupt of DPLL selected input clock fail, as determined by the LOS_FLAG_ON_TDO bit (b6, 0BH).
Power & Ground				
VDDD	D8, E8, F1, F8, F10, G2, G7, G9, H8, H10, K9	Power	-	Digital Core Power - +3.3V DC nominal
VDDDO	B14, C7, F12	Power	-	Digital Output Power - +3.3V DC nominal
VDDA	A2, C2, C9, C11, C12, D5, D10, D12, E11, F5, J10, P9, P11, P14	Power	-	Analog Core Power - +3.3V DC nominal
VDDAO	H1, H3, J3, J5, J7, K4, K6, L3, M1, M5, M7, P1, P5	Power	-	Analog Output Power - +3.3V DC nominal
VSSD	D7, E7, F2, F7, F9, G1, G6, G10, H7, H9, K8, K10	Ground	-	Ground
VSSDO	B13, C8, F14	Ground	-	Ground

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description ¹
VSSA	B2, B4, B9, B11, B12, C10, D1, D2, D4, D11, E3, E4, E5, E10, E12, F3, F4, F6, J9, G3, G4, G5, J8, L11, L13, M8, M9, M10, M11, N9, N11, N13, N14	Ground	-	Analog Ground
VSSAO	H2, H4, H5, H6, J4, J6, K1, K2, K3, K5, K7, L4, L5, L6, L7, M2, M3, M4, M6, N1, N3, N5, P3	Ground	-	Analog Output Ground
Others				
IC1	A1, A6, A7, A9, A13, B1, B6, B7, C1, C5, C6, C14, D6, D9, D13, D14, E1, E2, E9, E13, E14, F11, G8, G11, G12, G13, G14, H11, H12, J12, K11, K12, M13, M14, N4, N12, P4, P12, P13	-	-	IC1: Internal Connection Internal Use. These pins should be left open for normal operation.
IC2	A10, N7, N8, P7, P8	-	-	IC2: Internal Connection Internal Use. These pins should be left open for normal operation.
IC3	E6	-	-	IC3: Internal Connection Internal Use. This pin should be left open for normal operation.
NC	C3, M12	-	-	NC: Not Connected These pins should be left open for normal operation.
Note: 1. All the unused input pins should be connected to ground; the output of all the unused output pins are don't-care.				

2.1 RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

2.1.1 INPUTS

Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1 k Ω resistor can be used.

Single-Ended Clock Inputs

For protection, unused single-ended clock inputs should be tied to ground.

Differential Clock Inputs

For applications not requiring the use of a differential input, both *_POS and *_NEG can be left floating. Though not required, but for additional protection, a 1 k Ω resistor can be tied from _POS to ground.

XTAL Inputs

For applications not requiring the use of a crystal oscillator input, both _IN and _OUT can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from _IN to ground.

2.1.2 OUTPUTS

Status Pins

For applications not requiring the use of a status pin, we recommend bringing out to a test point for debugging purposes.

Single-Ended Clock Outputs

All unused single-ended clock outputs can be left floating, or can be brought out to a test point for debugging purposes.

Differential Clock Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

[illegible]

Figure 3. 196-Pin BAG Package Dimensions

ORDERING INFORMATION

XXXXXXX	XX	X	X		
Device Type			Process/ Temperature Range		
				Blank	Industrial (-40 °C to +85 °C)
				G	Green
				BA	196 ball 15mmx15mm CABGA package
				8V89317	

REVISION HISTORY

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