

Engineering Change Notice

The following table contains a list of engineering changes that are not reflected in the Tsi381 Evaluation Board Schematics.

Table 1: ECN for E2000_AS001_05 (Board order number Tsi381-RDK1 V2.0)

No.	Item(s)	Original	Change To
1	Tsi381 Device	Tsi381-66ILZ1	Tsi381-66ILZ2
2	3.3Vaux on J1, J2, J36, J37 ^a	No connection	Short pin A14 (3.3Vaux) to pin A16 (VIO_PCI) with 0-Ohm (0603) resistor

a. 3.3Vaux does not provide power to plug-in cards when the system is powered down.

Table 2: ECN for E2000_AS001_04 (Board order number Tsi381-RDK1 V2.1)

No.	Item(s)	Original	Change To
1	Tsi381 Device	Tsi381-66ILZ1	Tsi381-66ILZ2 ^a
2	3.3Vaux on J1, J2, J36, J37 ^b	No connection	Short pin A14 (3.3Vaux) to pin A16 (VIO_PCI) with 0-Ohm (0603) resistor

a. Ball K1 was removed from the Tsi381 device to allow the TEST_SPARE[2] signal to be detected as logic high. This version of the evaluation board is intended to support applications that require PCI bus parking on the Tsi381.

b. 3.3Vaux does not provide power to plug-in cards when the system is powered down.

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C		60E2000_SC001_03		1.0				
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1	2	3	4	5	6	7		

TSI381 PCIE/MISC INTERFACE

TSI381 STRAPS

RESET CONTROLLER

TI381 JTAG

TITLE :

Tsi381 PCIE/MISC

SIZE

DRAWING NUMBER :

Version:

DESIGNER :

LAST MODIFIED DATE :

7-24-2007_17:09

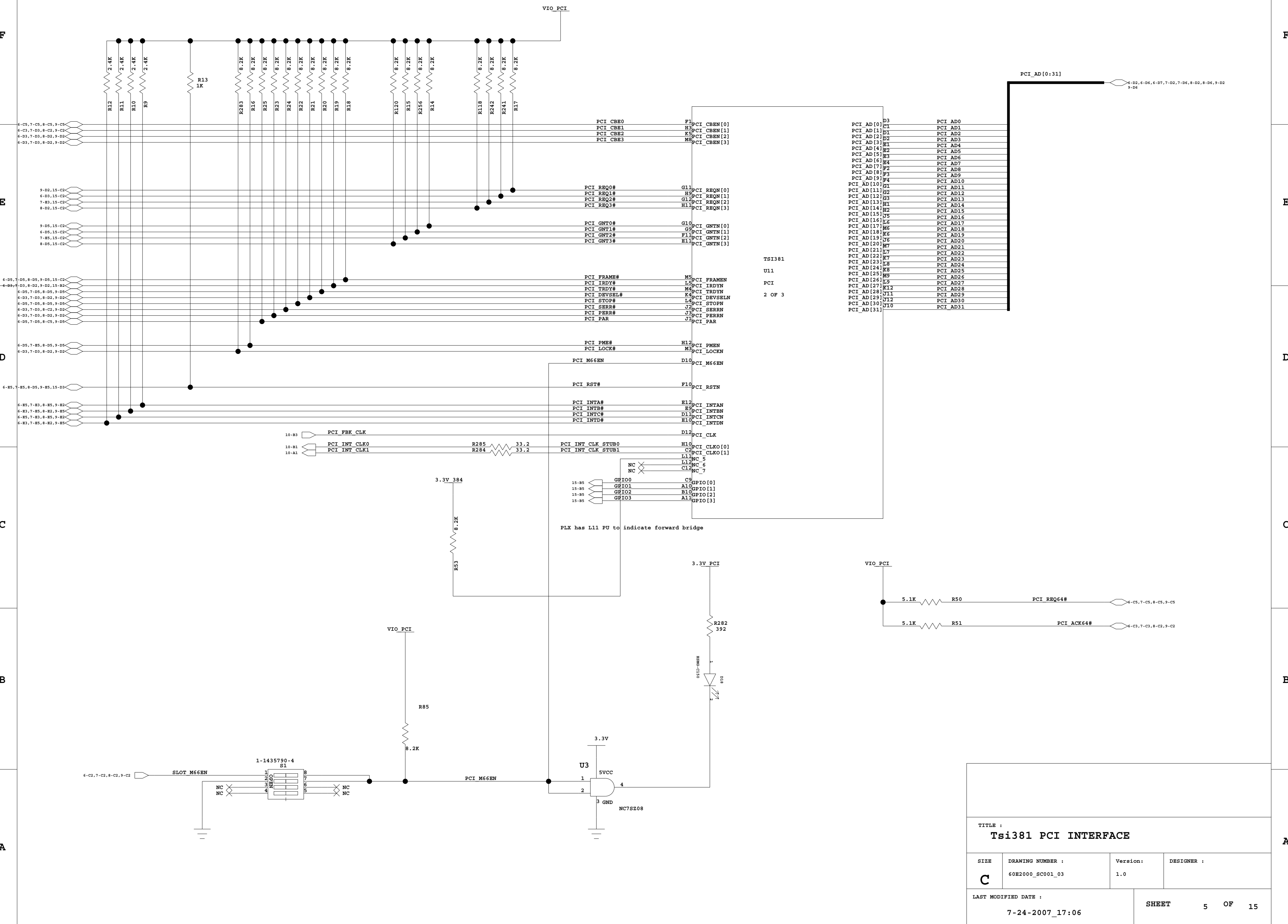
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TITLE :			
PCIE CONNECTORS			
SIZE C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 6-15-2007_14:56		SHEET 4 OF 15	

TSI381 PCI INTERFACE



TITLE : Tsi381 PCI INTERFACE			
SIZE C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
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PCI SLOT 0 (R/A)

IDSEL AD16

- Required Interrupt Routing

SLOT : BRIDGE

INTA -> INTA

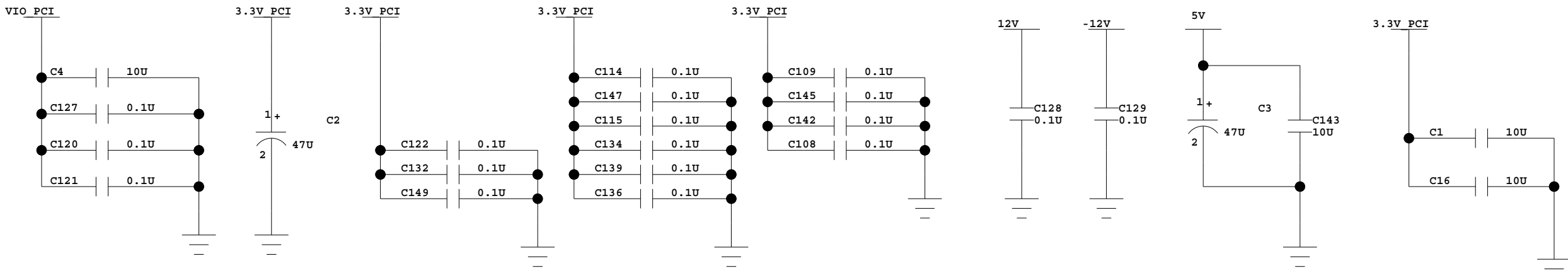
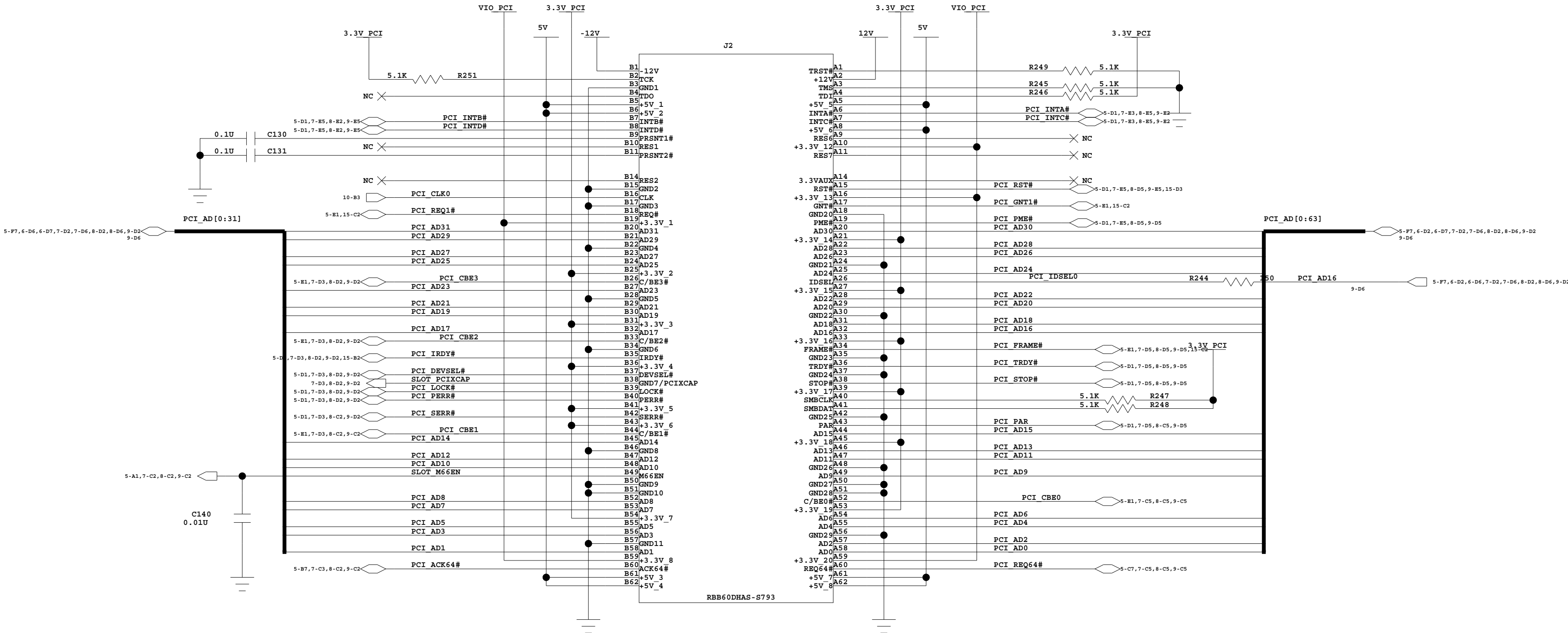
INTB -> INTB

INTC -> INTC

INTD -> INTD

- PCI Clock PCI_CLK0

- PCI Arbitration PCI_GNT#1/PCI_REQ#1



TITLE :			
PCI SLOT 0			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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IDSEL AD17

- Required Interrupt Routing

    SLOT : BRIDGE

    INTA -> INTB

    INTB -> INTC

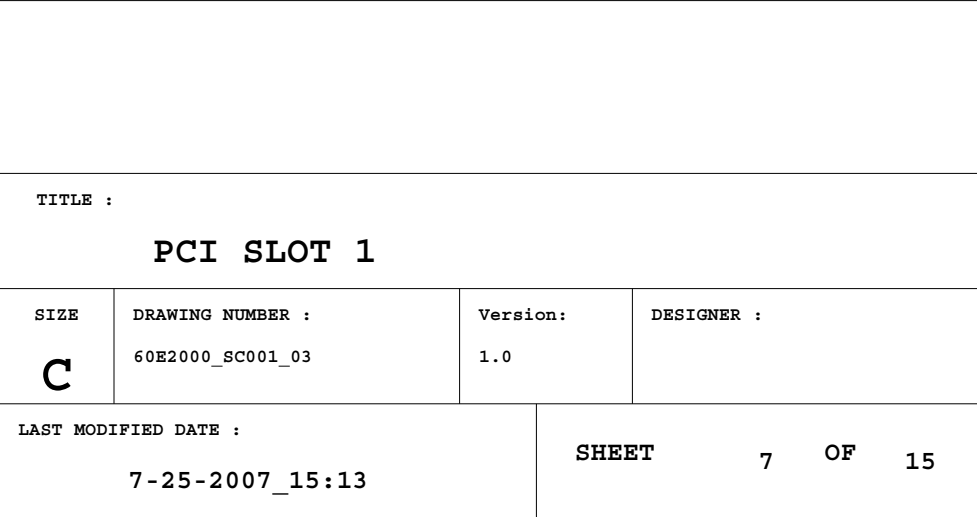
    INTC -> INTD

    INTD -> INTA

- PCI Clock PCI_CLK1

- PCI Arbitration PCI_GNT#2/PCI_REQ#2

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IDSEL AD18

- Required Interrupt Routing

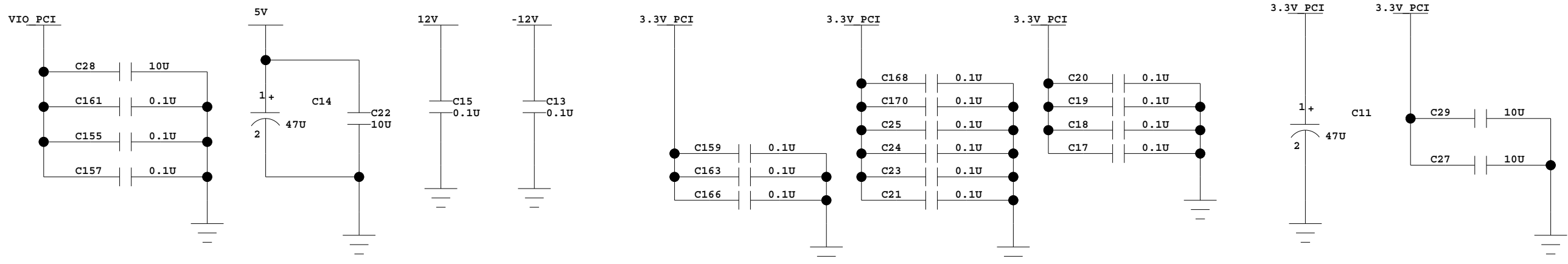
    SLOT : BRIDGE

    INTA -> INTC
    INTB -> INTD
    INTC -> INTA
    INTD -> INTB

- PCI Clock PCI_CLK2

- PCI Arbitration PCI_GNT#3/PCI_REQ#3

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TITLE :			
PCI SLOT 3			
SIZE C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
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F

E

D

C

B

A

F

E

D

C

B

A

PCI SLOT 2 (Vertical)

IDSEL AD19

- Required Interrupt Routing

SLOT : BRIDGE

INTA -> INTD

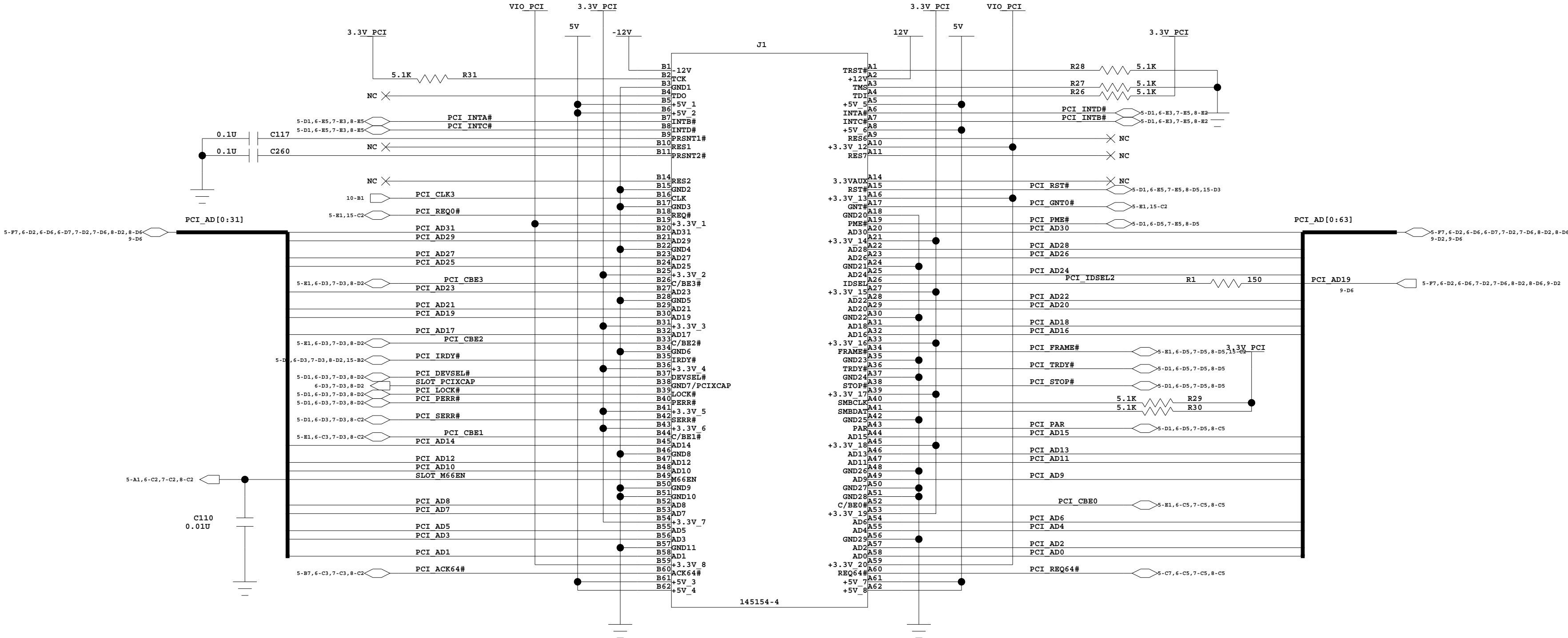
INTB -> INTA

INTC -> INTB

INTD -> INTC

- PCI Clock PCI_CLK3

- PCI Arbitration PCI_GNT#0/PCI_REQ#0



TITLE :			
PCI SLOT 2			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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CLOCK DISTRIBUTION

PCI EXTERNAL CLOCK

PCIe LOCAL CLOCKGEN

SYS/LOCAL PCIe CLOCK MULTIPLEXER

Frequency Select (ICS87604I)		
FBDIV_SEL[0:1]	DIV_SEL[0:1]	OUTPUT
0:0	0:0	100Mhz
0:0	1:0	50Mhz
0:0	1:1	25Mhz
0:1	0:0	133Mhz
0:1	1:0	66Mhz
0:1	1:1	33Mhz

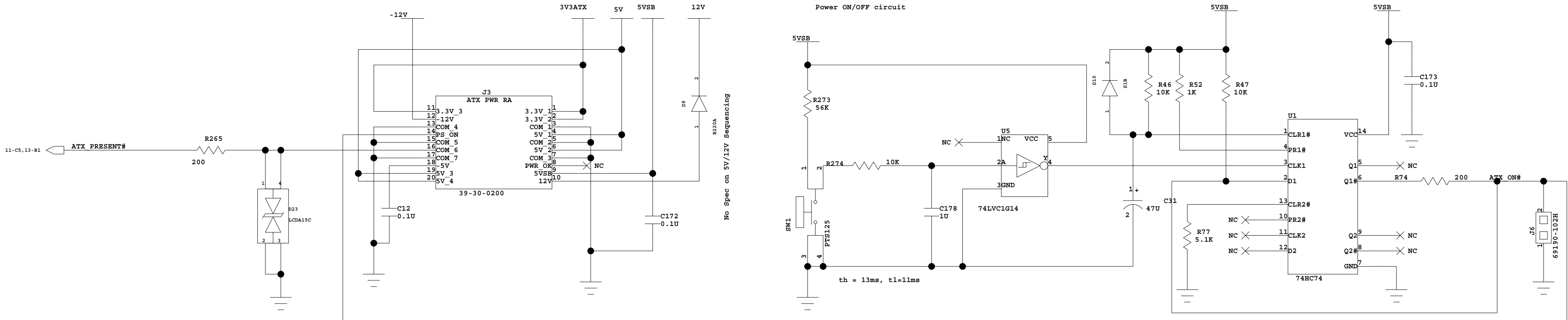
Place resistors near CY2305

TITLE :			
CLOCK DISTRIBUTION			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2000_SC001_03	1.0	
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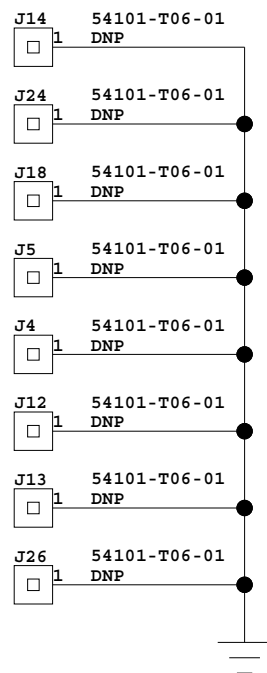
POWER SOURCES

ATX SUPPLY TOGGLE

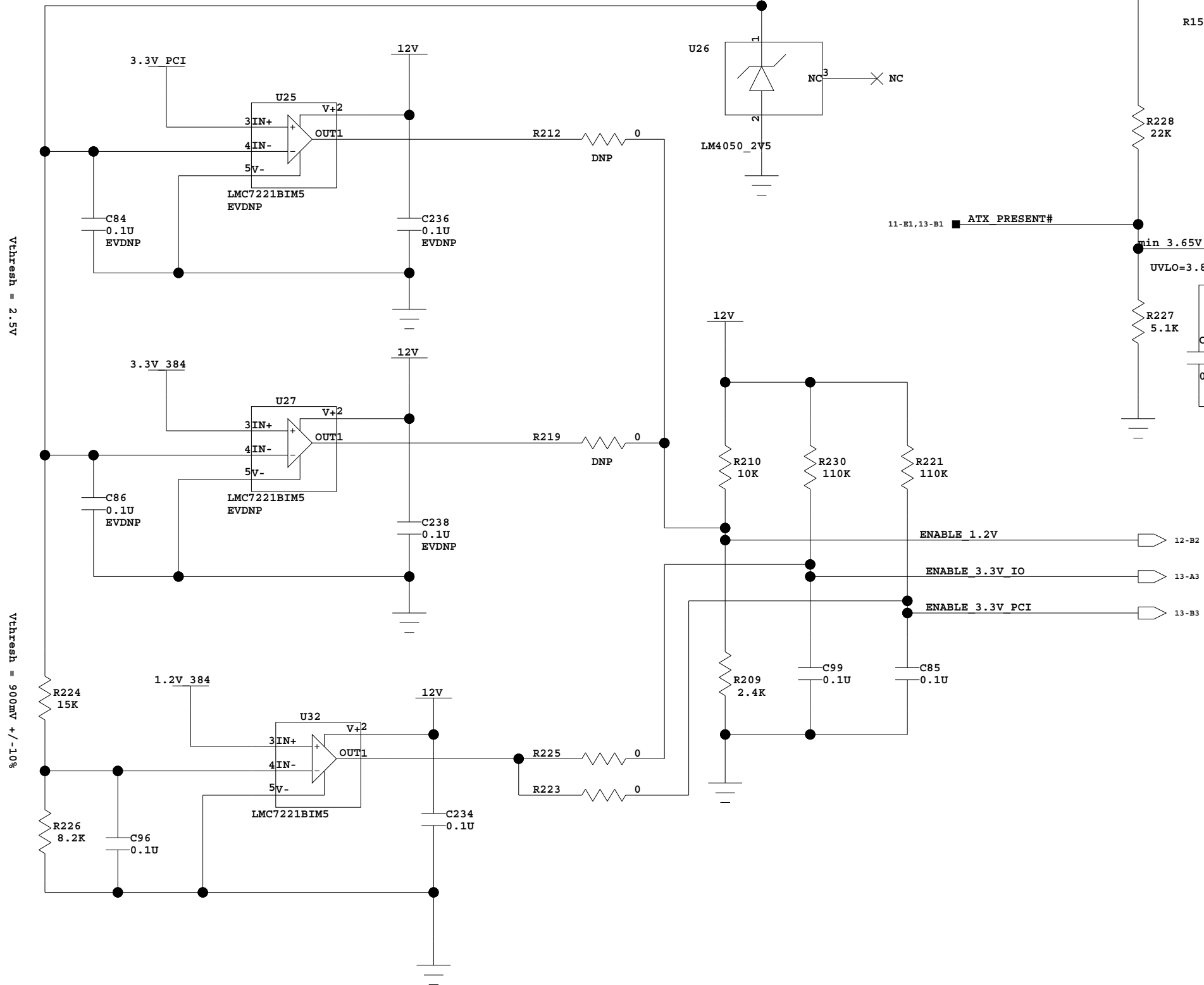
ATX



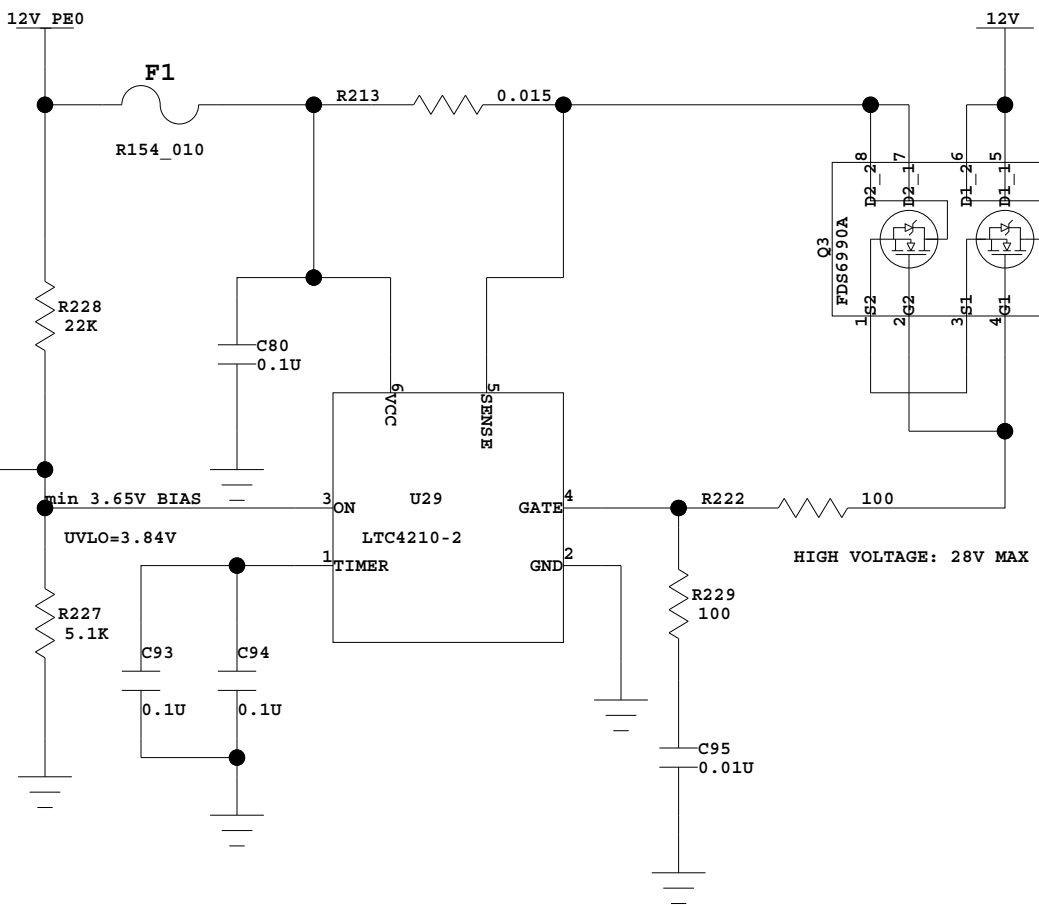
GND TESTPOINTS



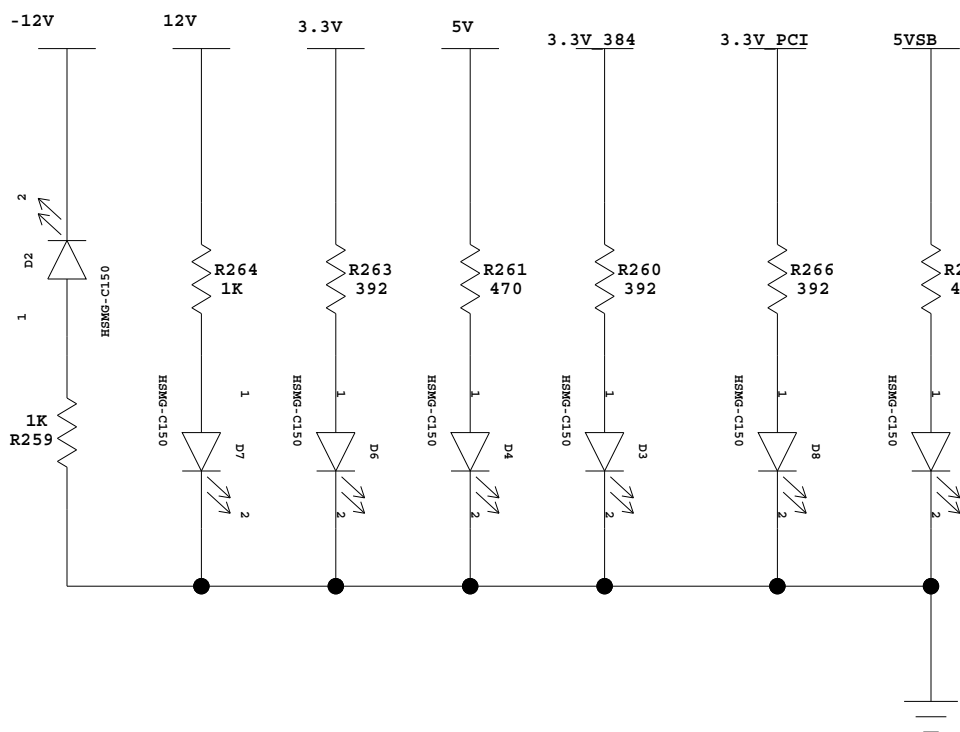
BOARD SEQUENCING



SYS SUPPLY SWITCH

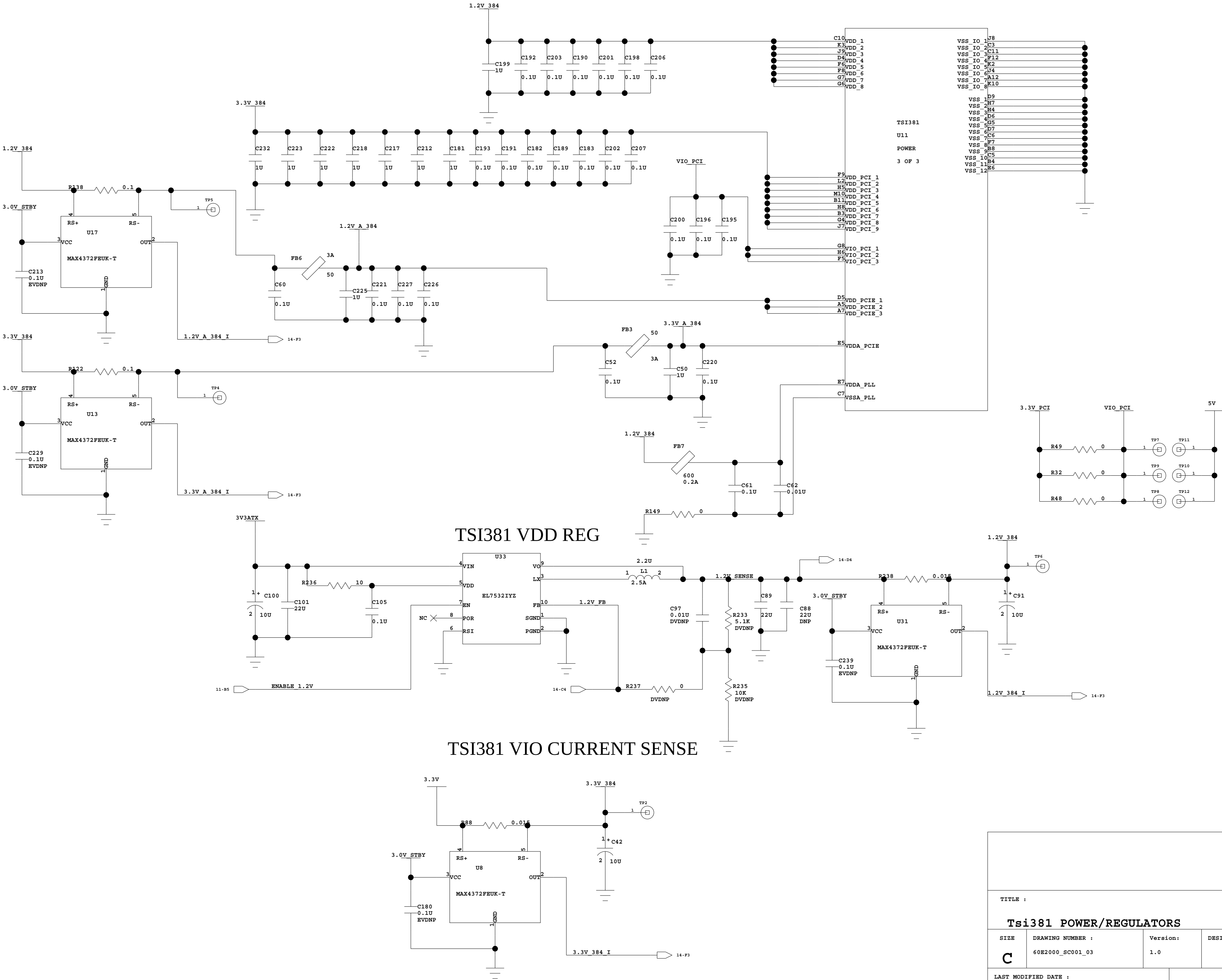


POWER STATUS



TITLE : POWER SOURCES			
SIZE C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
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TSI381 POWER/REGULATORS

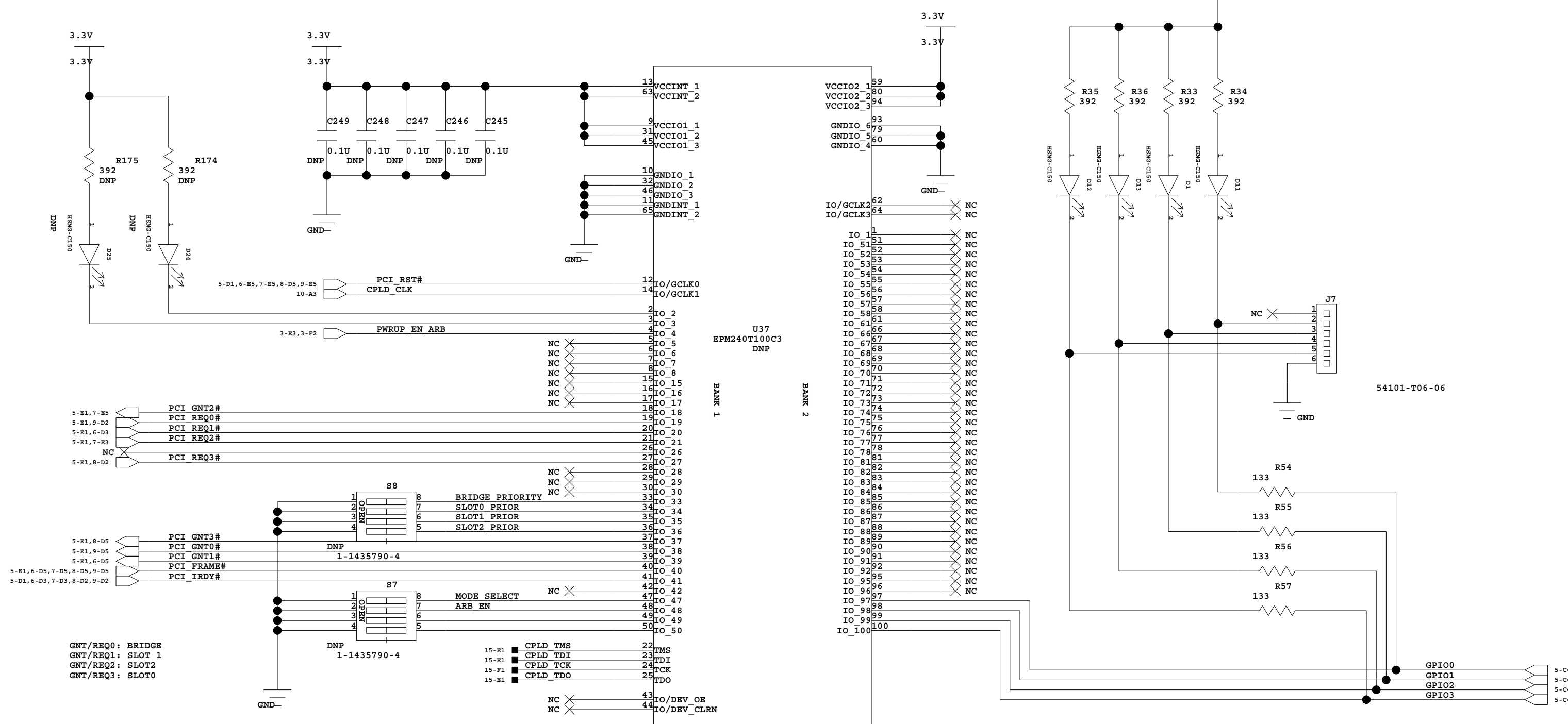
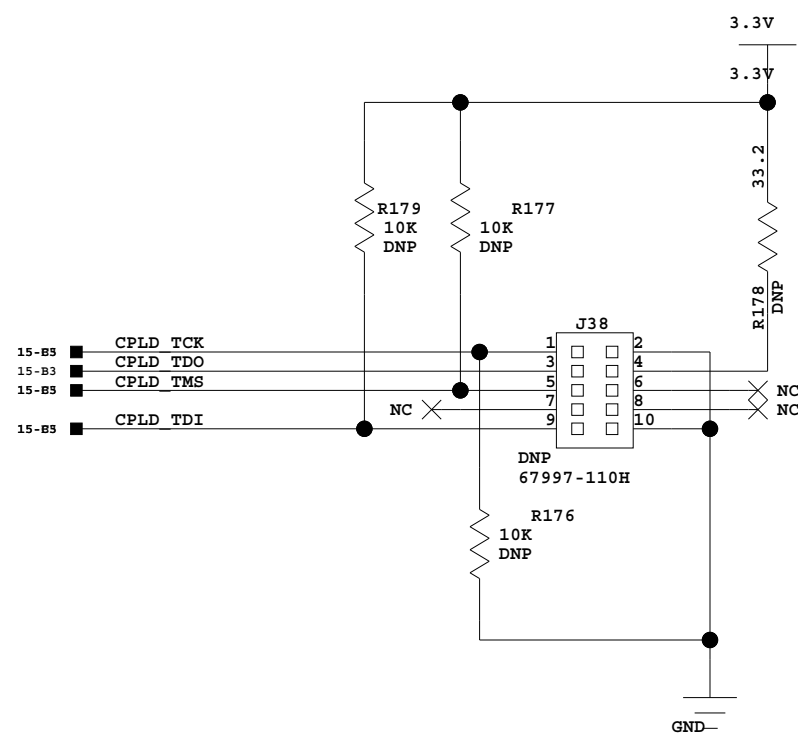


TITLE :			
Tsi381 POWER/REGULATORS			
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TITLE :			
PCI POWER REGULATORS			
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C	60E2000_SC001_03	1.0	
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TEST DEVICES CONT'D

PCIARBITER/GPIO CONTROL



TITLE :			
TEST DEVICES CONT'D			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2000_SC001_03	1.0	
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