

# Engineering Change Notice

The following table contains a list of engineering changes that are not reflected in the Tsi381 Evaluation Board Schematics.

**Table 1: ECN for E2000\_AS001\_05 (Board order number Tsi381-RDK1 V2.0)**

No.	Item(s)	Original	Change To
1	Tsi381 Device	Tsi381-66ILZ1	Tsi381-66ILZ2
2	3.3Vaux on J1, J2, J36, J37 <sup>a</sup>	No connection	Short pin A14 (3.3Vaux) to pin A16 (VIO_PCI) with 0-Ohm (0603) resistor

a. 3.3Vaux does not provide power to plug-in cards when the system is powered down.

**Table 2: ECN for E2000\_AS001\_04 (Board order number Tsi381-RDK1 V2.1)**

No.	Item(s)	Original	Change To
1	Tsi381 Device	Tsi381-66ILZ1	Tsi381-66ILZ2 <sup>a</sup>
2	3.3Vaux on J1, J2, J36, J37 <sup>b</sup>	No connection	Short pin A14 (3.3Vaux) to pin A16 (VIO_PCI) with 0-Ohm (0603) resistor

a. Ball K1 was removed from the Tsi381 device to allow the TEST\_SPARE[2] signal to be detected as logic high. This version of the evaluation board is intended to support applications that require PCI bus parking on the Tsi381.

b. 3.3Vaux does not provide power to plug-in cards when the system is powered down.

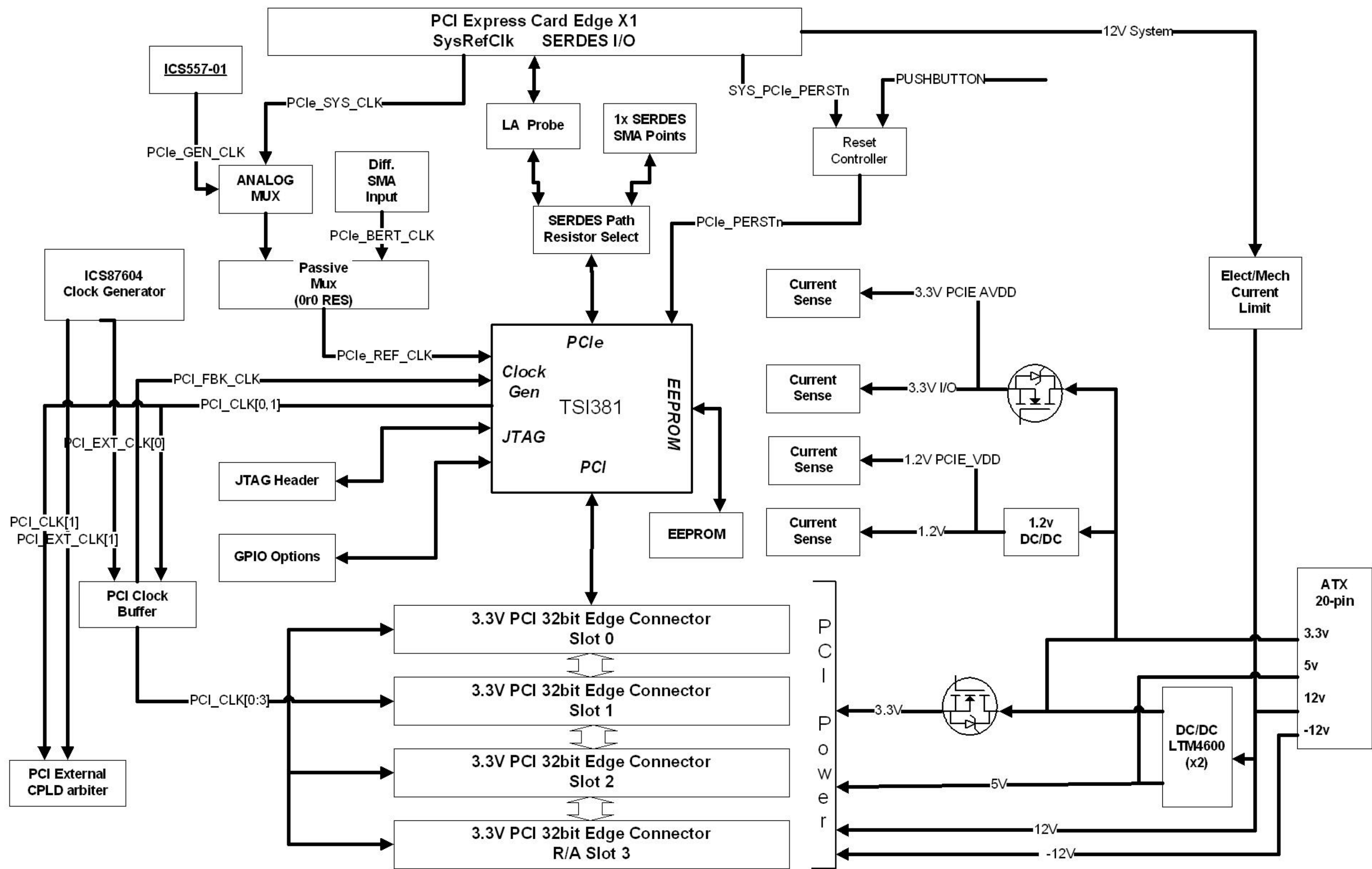
# Tsi381 Evaluation Board Schematic

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TITLE:			
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C	60E2000_SC001_03	1.0	
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7-24-2007_17:10			

# BLOCK DIAGRAM



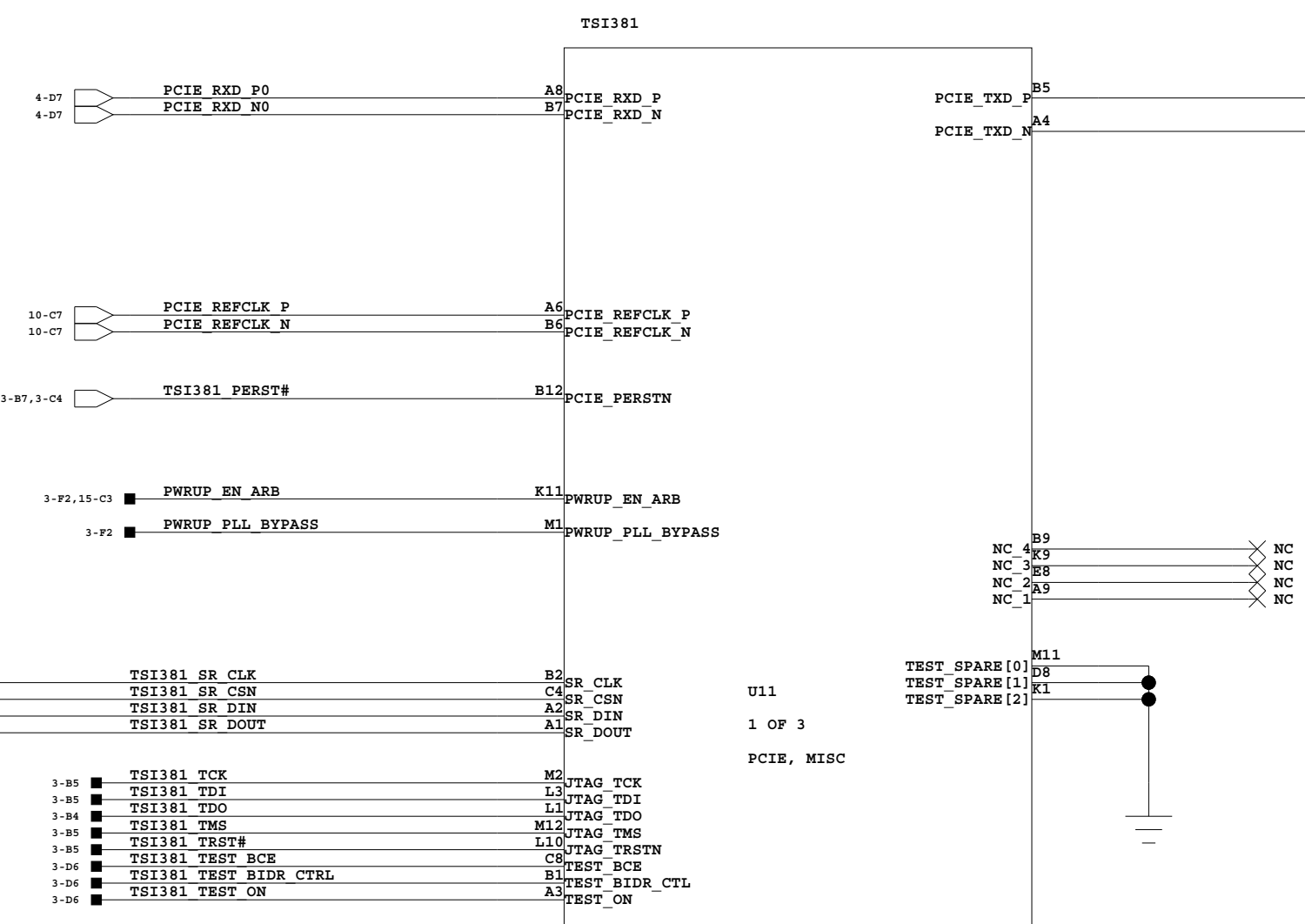
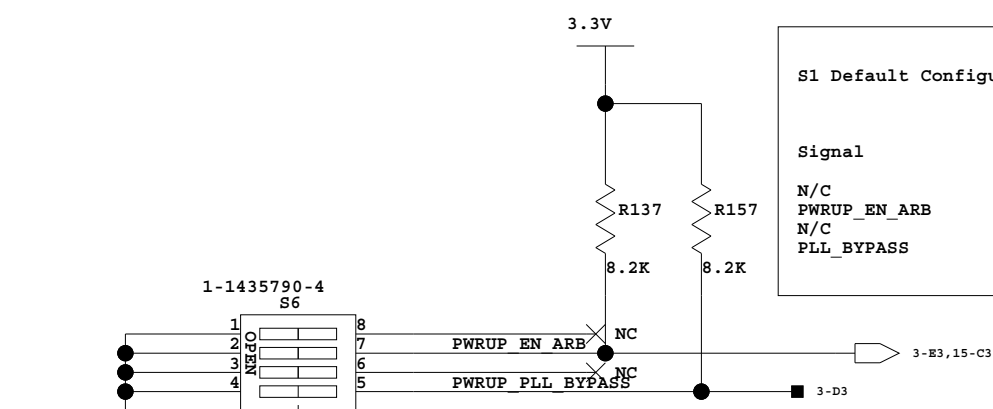
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SIZE <b>C</b>	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 5-3-2007_11:54		SHEET 2 OF 15	

# TSI381 PCIE/MISC INTERFACE

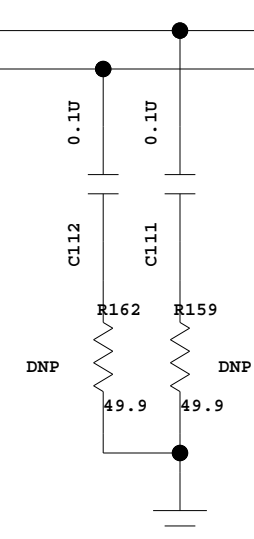
**S1 Default Configuration**

Signal	(1=High, 0=Low)
N/C	
PWRUP_EN_ARB	0
N/C	
PLL_BYPASS	0

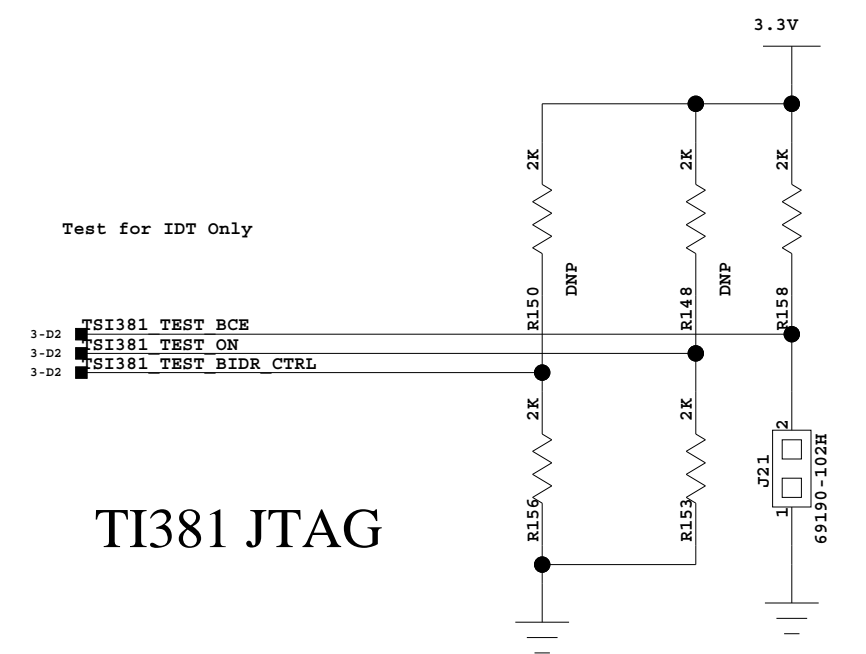
## TSI381 STRAPS



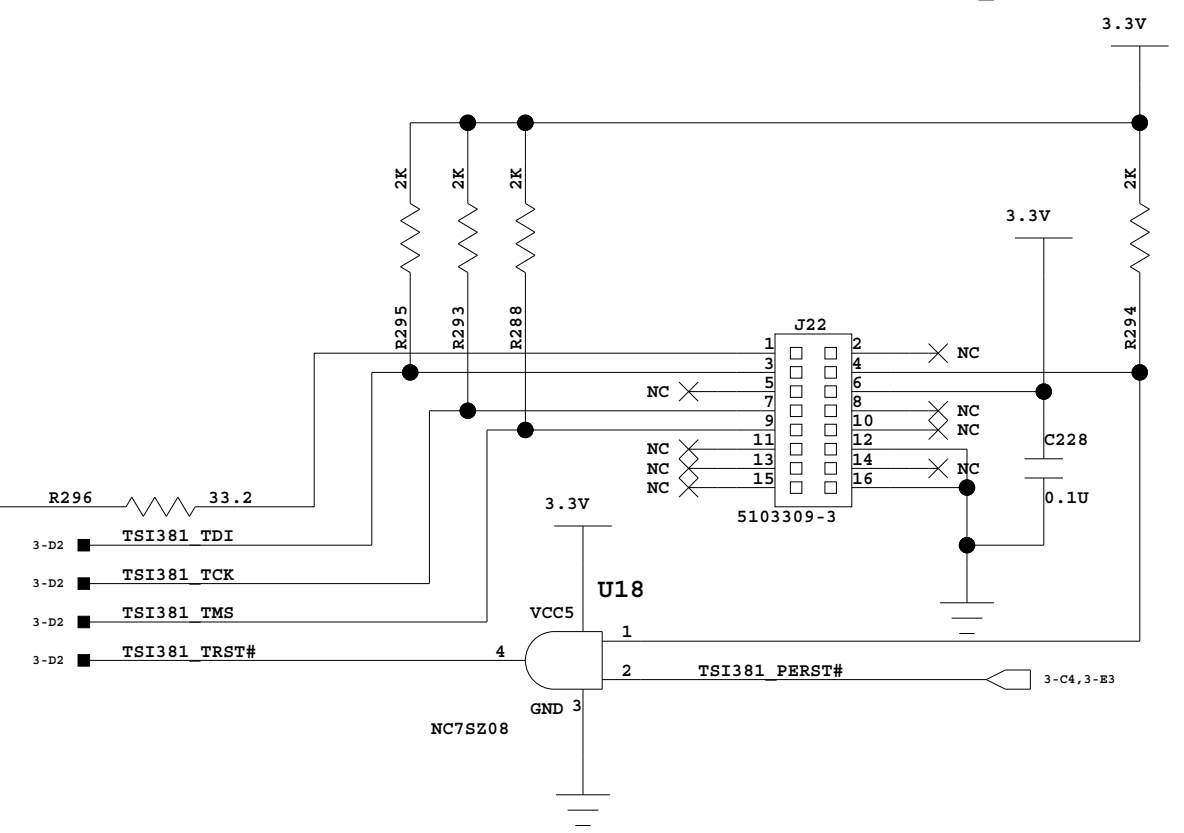
## TX Compliance Testing



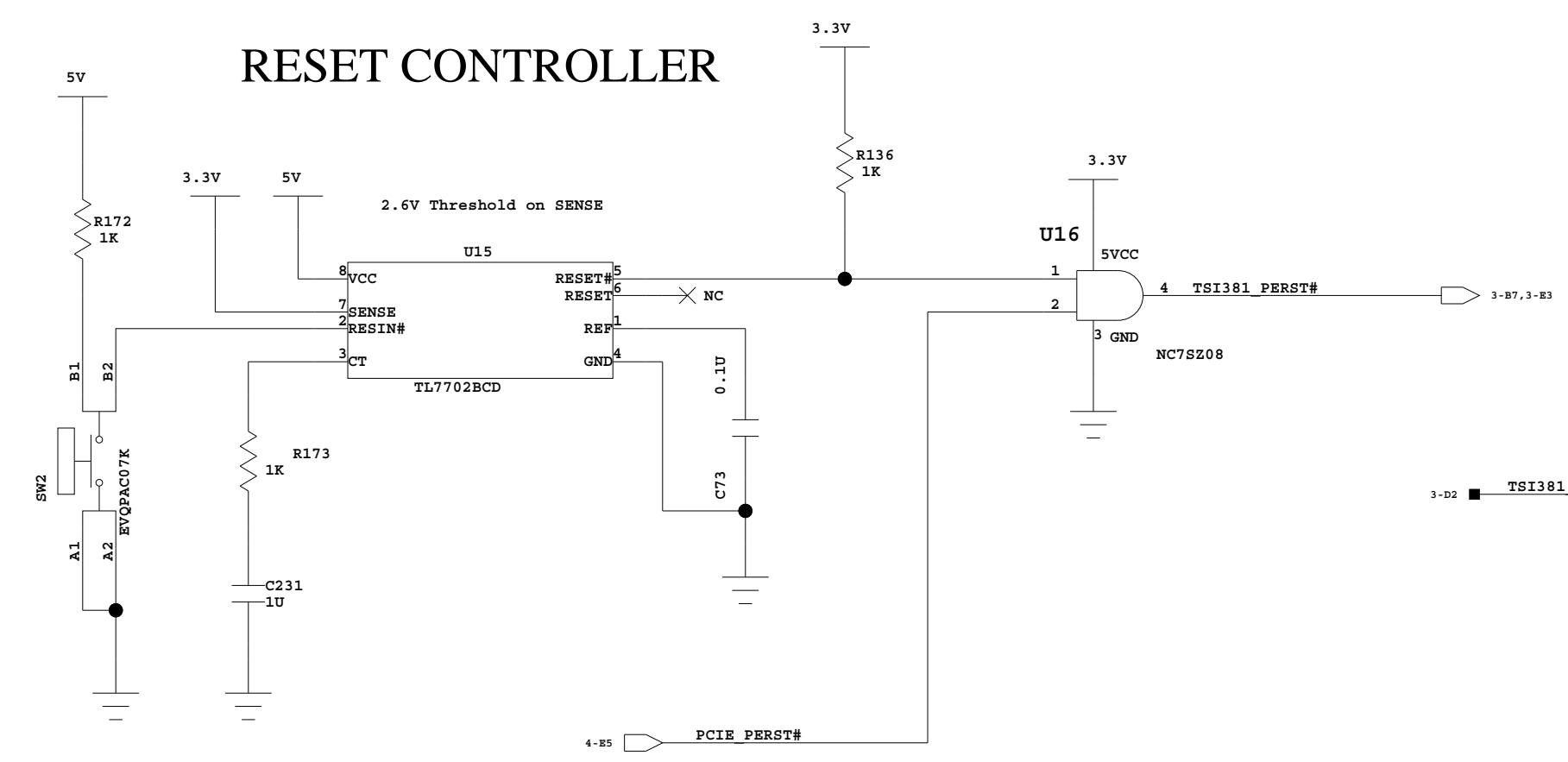
## Test for IDT Only



## TSI381 JTAG

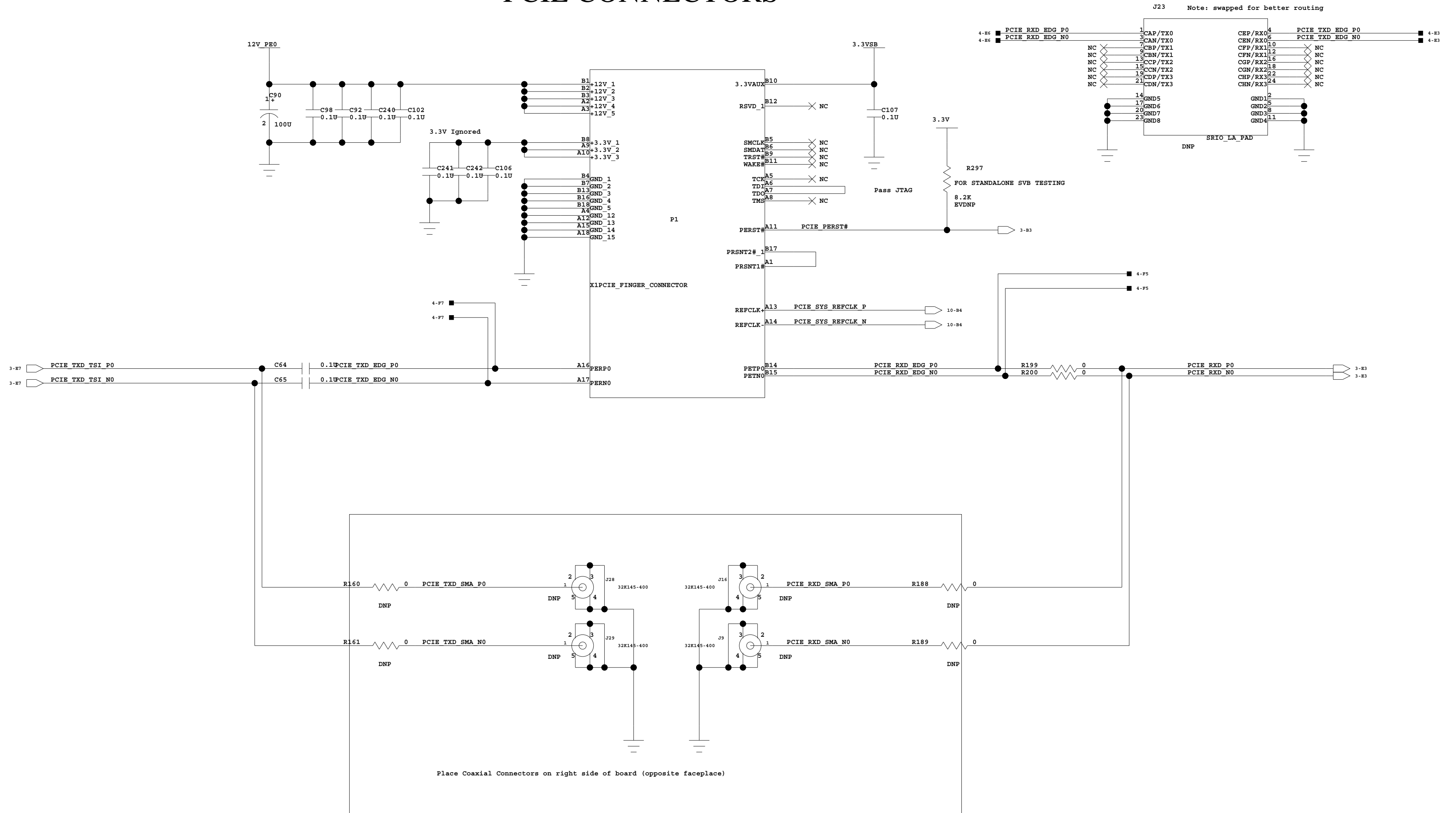


## RESET CONTROLLER



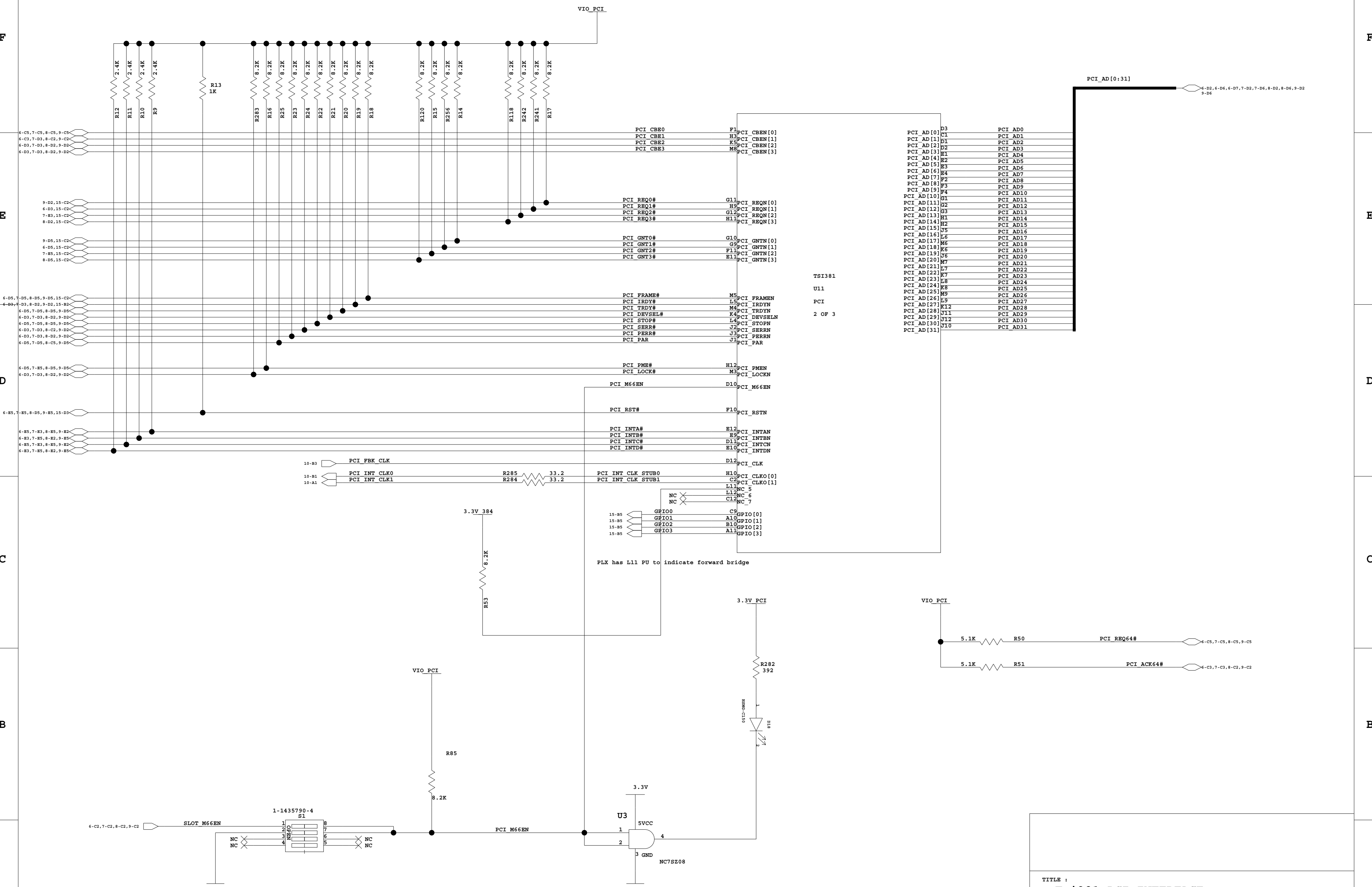
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SIZE <b>C</b>	DRAWING NUMBER : 60E2000_SCO01_03	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 7-24-2007_17:09			SHEET <b>3</b> OF <b>15</b>

# PCIE CONNECTORS



TITLE :			
PCIE CONNECTORS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2000_SCO01_03	1.0	
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# TSI381 PCI INTERFACE



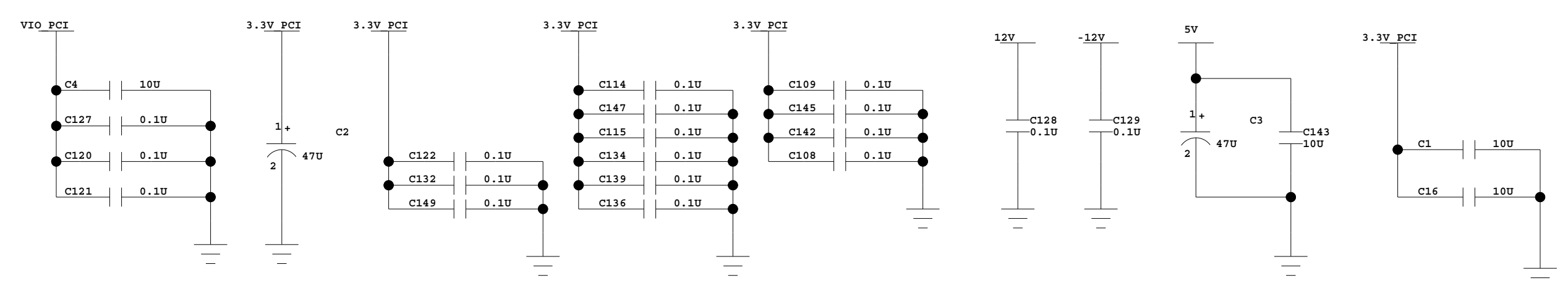
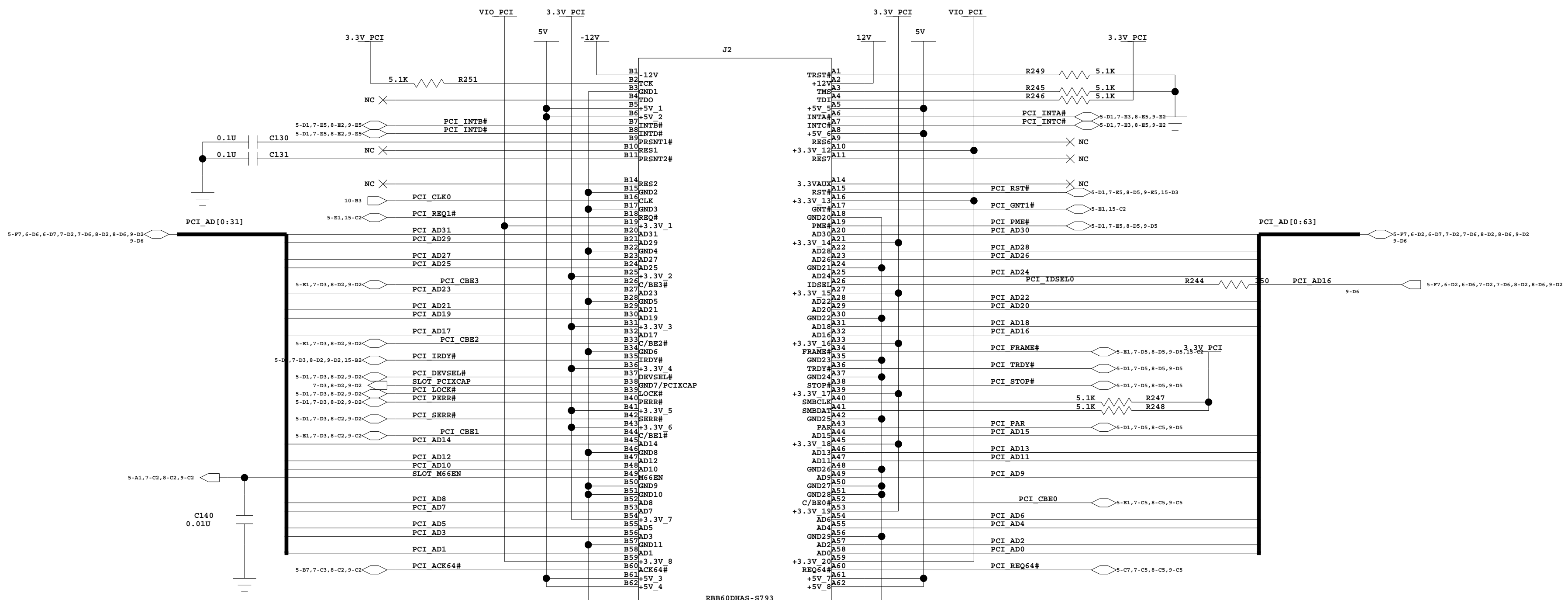
PCI\_AD[0:31]

6-D2, 6-D6, 6-D7, 7-D2, 7-D6, 8-D2, 8-D6, 9-D2	9-D6
PCI AD[0]	D3
PCI AD[1]	D1
PCI AD[2]	D2
PCI AD[3]	E1
PCI AD[4]	E2
PCI AD[5]	E3
PCI AD[6]	E4
PCI AD[7]	F2
PCI AD[8]	F3
PCI AD[9]	F4
PCI AD[10]	G1
PCI AD[11]	G2
PCI AD[12]	G3
PCI AD[13]	H1
PCI AD[14]	H2
PCI AD[15]	H3
PCI AD[16]	J5
PCI AD[17]	J6
PCI AD[18]	K5
PCI AD[19]	K6
PCI AD[20]	J6
PCI AD[21]	N7
PCI AD[22]	N7
PCI AD[23]	L8
PCI AD[24]	M8
PCI AD[25]	M8
PCI AD[26]	L9
PCI AD[27]	K12
PCI AD[28]	J11
PCI AD[29]	J12
PCI AD[30]	J12
PCI AD[31]	J10

TITLE :			
<b>Tsi381 PCI INTERFACE</b>			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
<b>C</b>	60E2000_SC001_03	1.0	
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# PCI SLOT 0 (R/A)

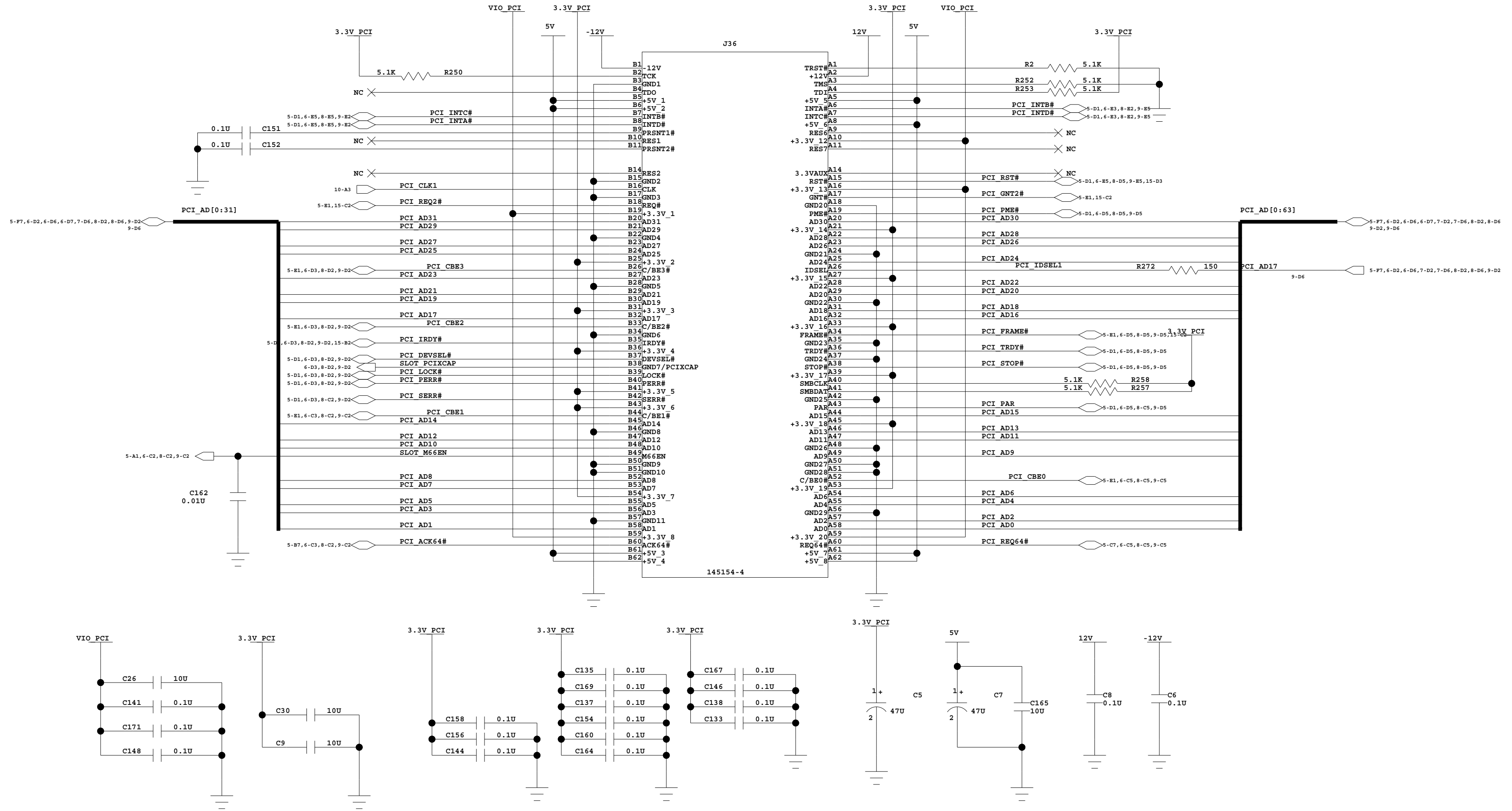
IDSEL AD16  
 - Required Interrupt Routing  
 SLOT : BRIDGE  
 INTA -> INTA  
 INTB -> INTB  
 INTC -> INTC  
 INTD -> INTD  
 - PCI Clock PCI\_CLK0  
 - PCI Arbitration PCI\_GNT#1/PCI\_REQ#1



TITLE :			
PCI SLOT 0			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2000_SC001_03	1.0	
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# PCI SLOT 1 (Vertical)

**IDSEL AD17**  
 - Required Interrupt Routing  
 SLOT : BRIDGE  
 INTA -> INTB  
 INTB -> INTC  
 INTC -> INTD  
 INTD -> INTA  
  
 - PCI Clock PCI\_CLK1  
  
 - PCI Arbitration PCI\_GNT#2/PCI\_REQ#2

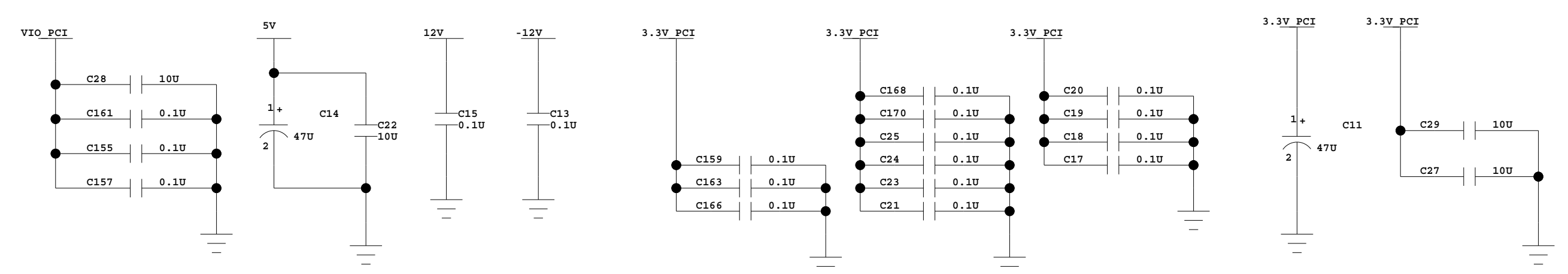
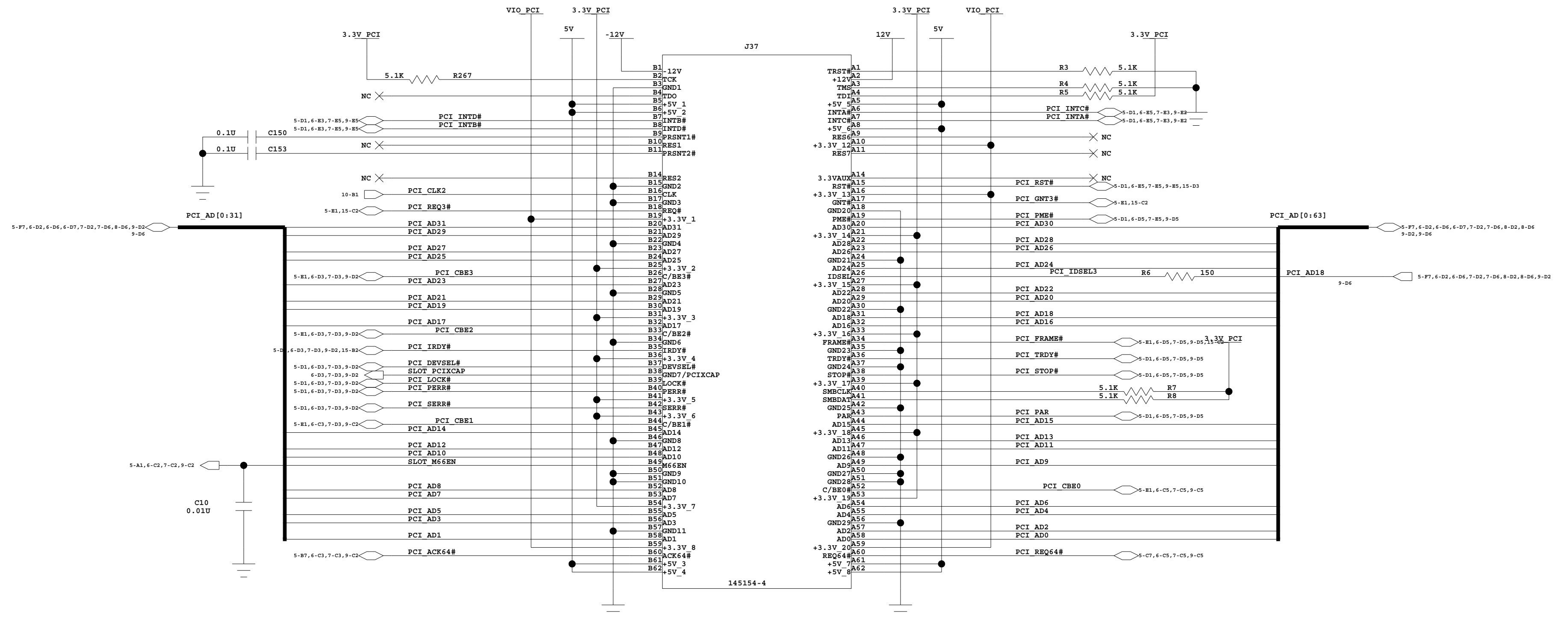


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<b>PCI SLOT 1</b>			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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# PCI SLOT 3 (Vertical)

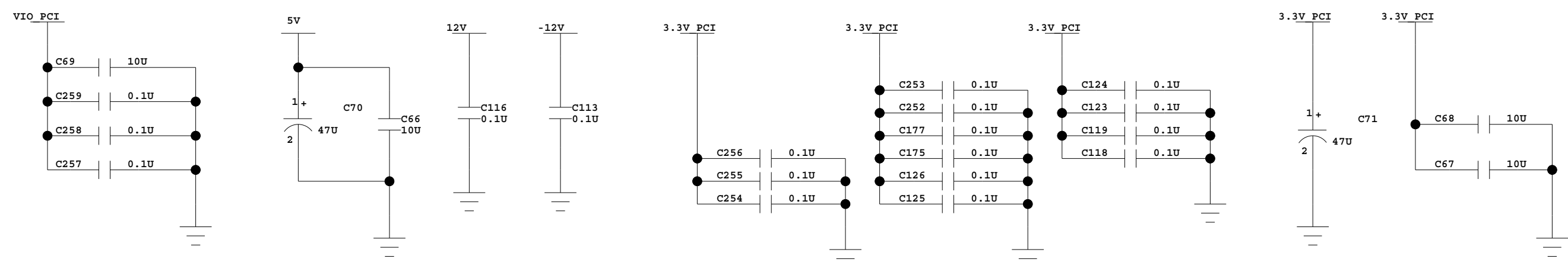
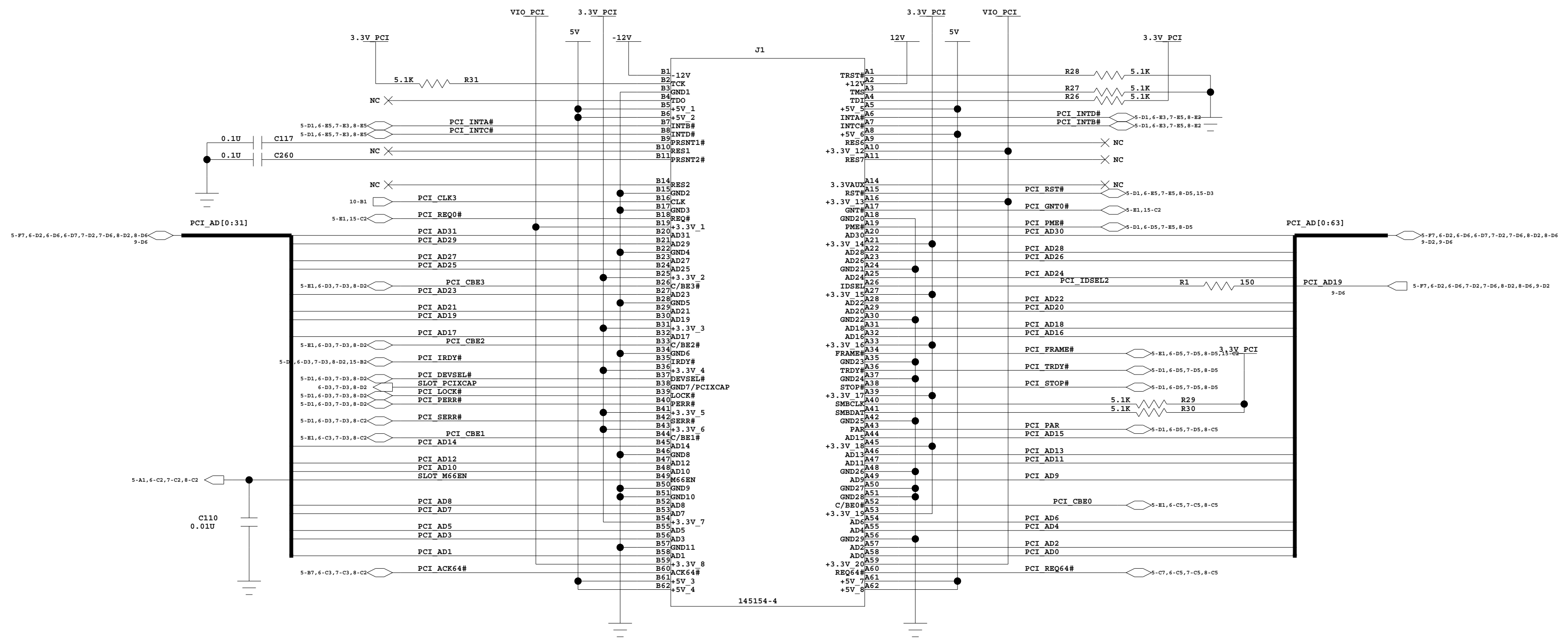
**IDSEL AD18**  
 - Required Interrupt Routing  
 SLOT : BRIDGE  
 INTA -> INTC  
 INTB -> INTD  
 INTC -> INTA  
 INTD -> INTB  
  
 - PCI Clock PCI\_CLK2  
  
 - PCI Arbitration PCI\_GNT#3/PCI\_REQ#3



TITLE :			
<b>PCI SLOT 3</b>			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
<b>C</b>	60E2000_SCO01_03	1.0	
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# PCI SLOT 2 (Vertical)

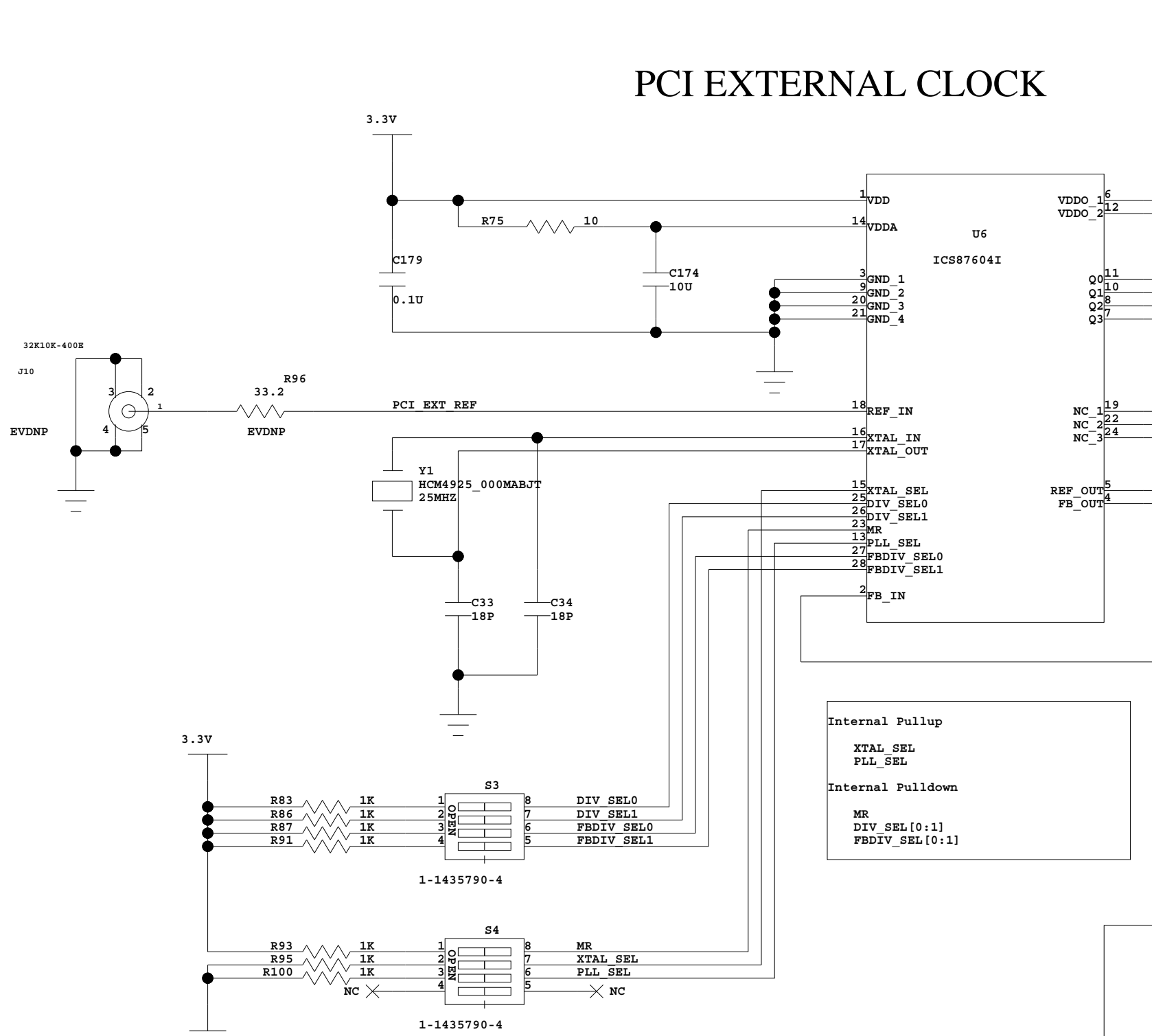
**IDSEL AD19**  
 - Required Interrupt Routing  
 SLOT : BRIDGE  
 INTA -> INTD  
 INTB -> INTA  
 INTC -> INTB  
 INTD -> INTC  
  
 - PCI Clock PCI\_CLK3  
  
 - PCI Arbitration PCI\_GNT#0/PCI\_REQ#0



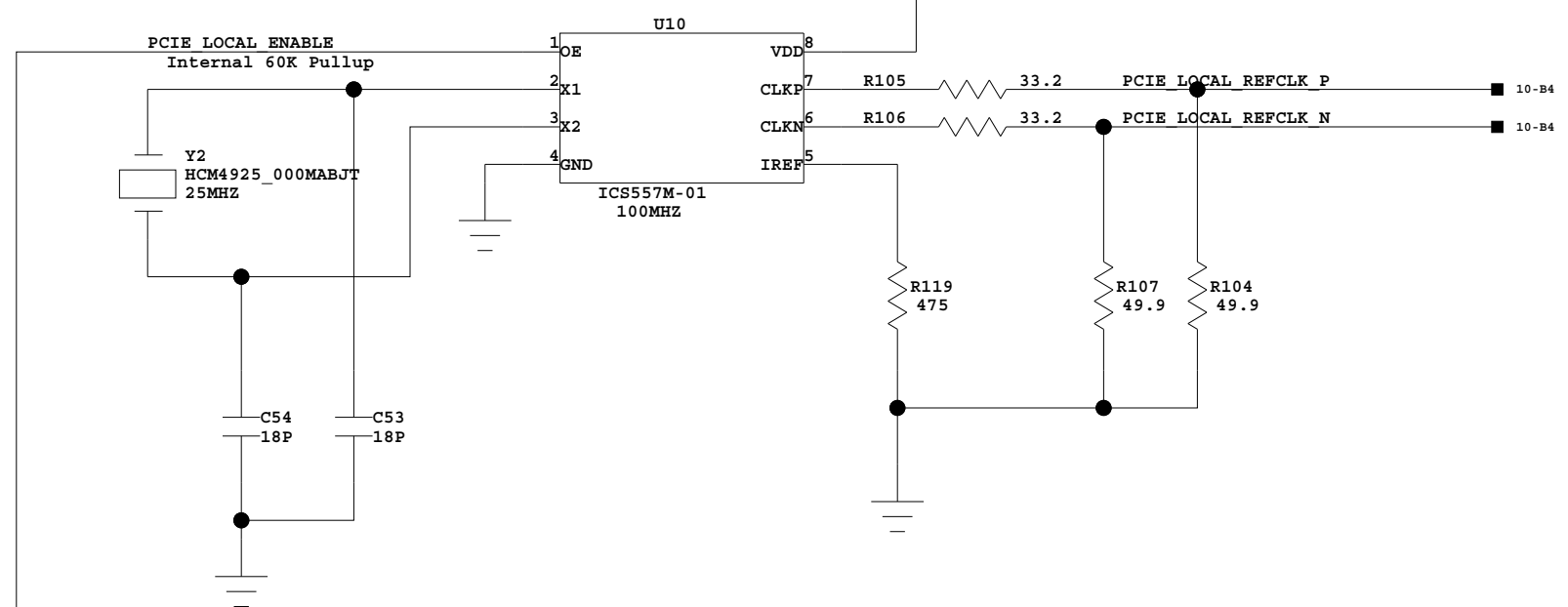
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# CLOCK DISTRIBUTION

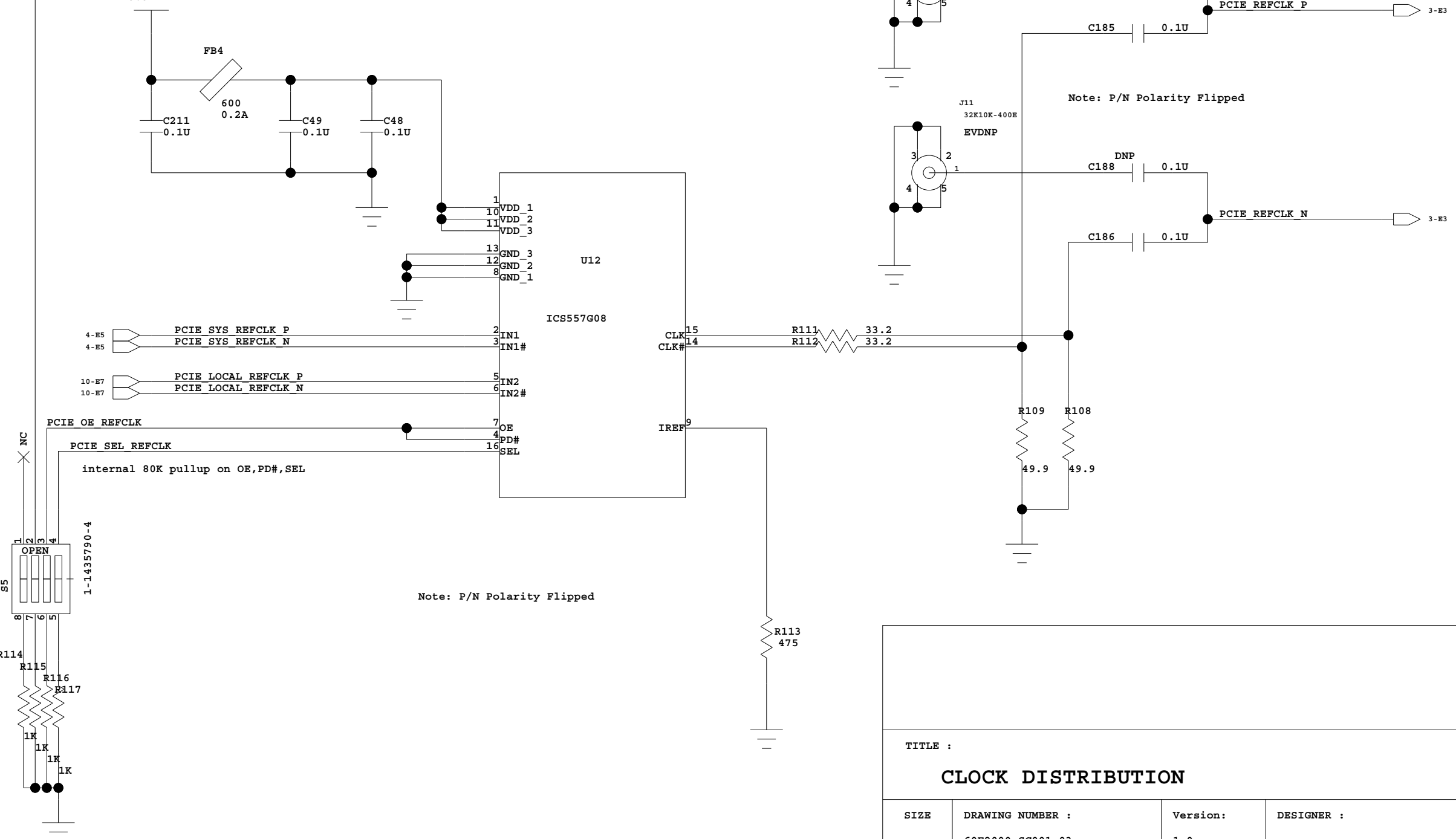
## PCI EXTERNAL CLOCK



## PCIe LOCAL CLOCKGEN

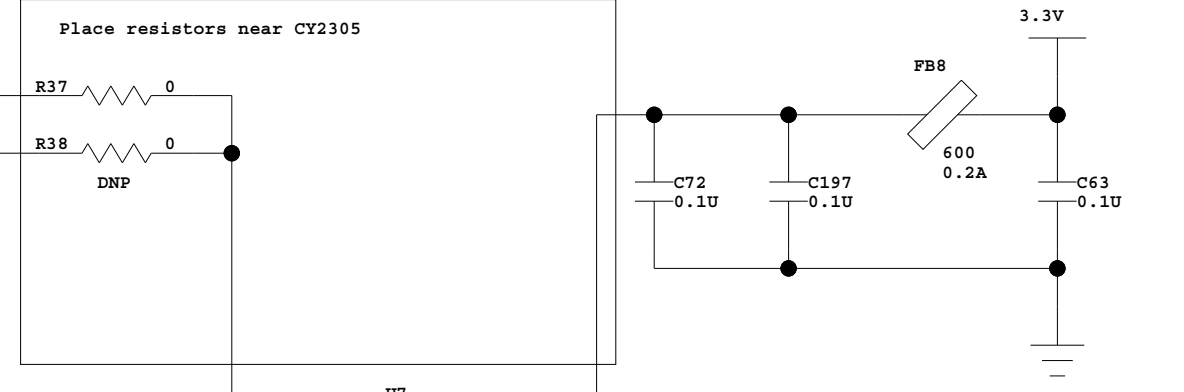


## SYS/LOCAL PCIe CLOCK MULTIPLEXER



Frequency Select (ICS87604I)

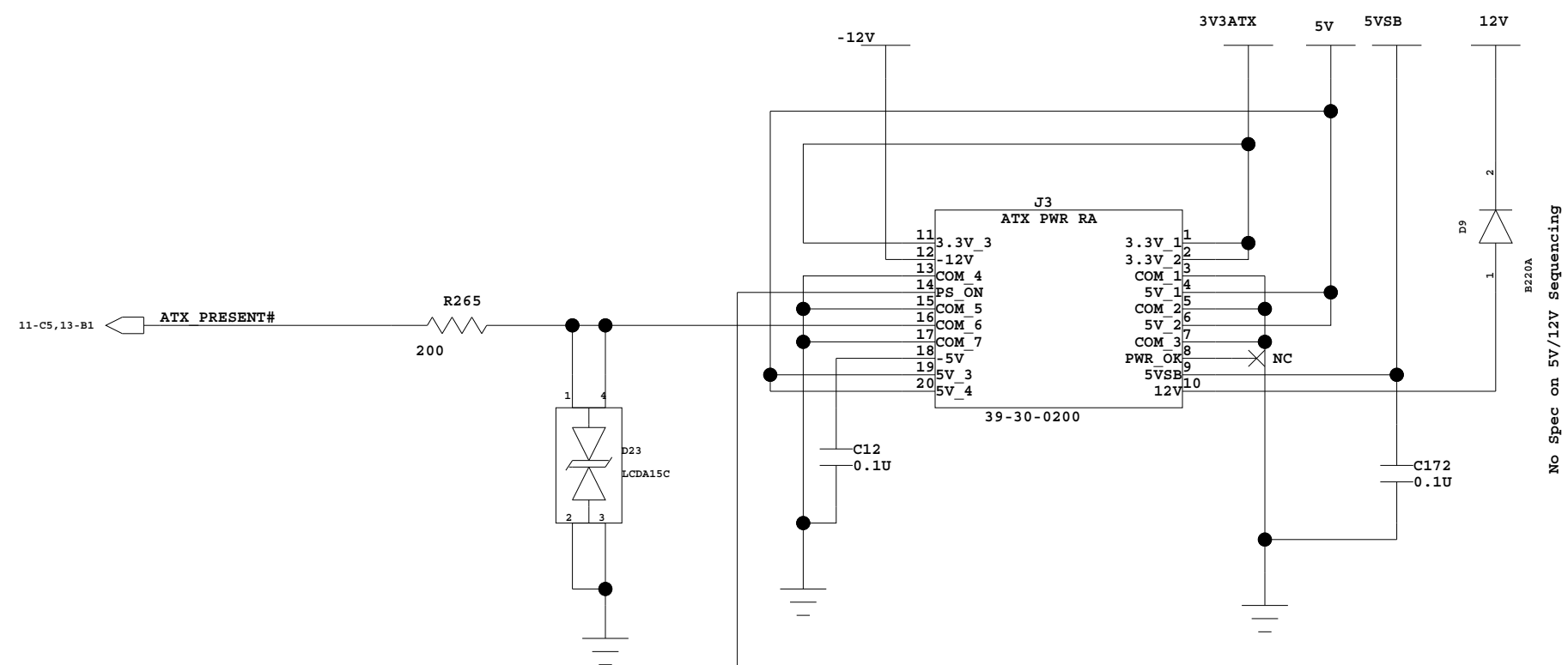
FBDIV_SEL[0:1]	DIV_SEL[0:1]	OUTPUT
0:0	0:0	100Mhz
0:0	1:0	50Mhz
0:0	1:1	25Mhz
0:1	0:0	133Mhz
0:1	1:0	66Mhz
0:1	1:1	33Mhz



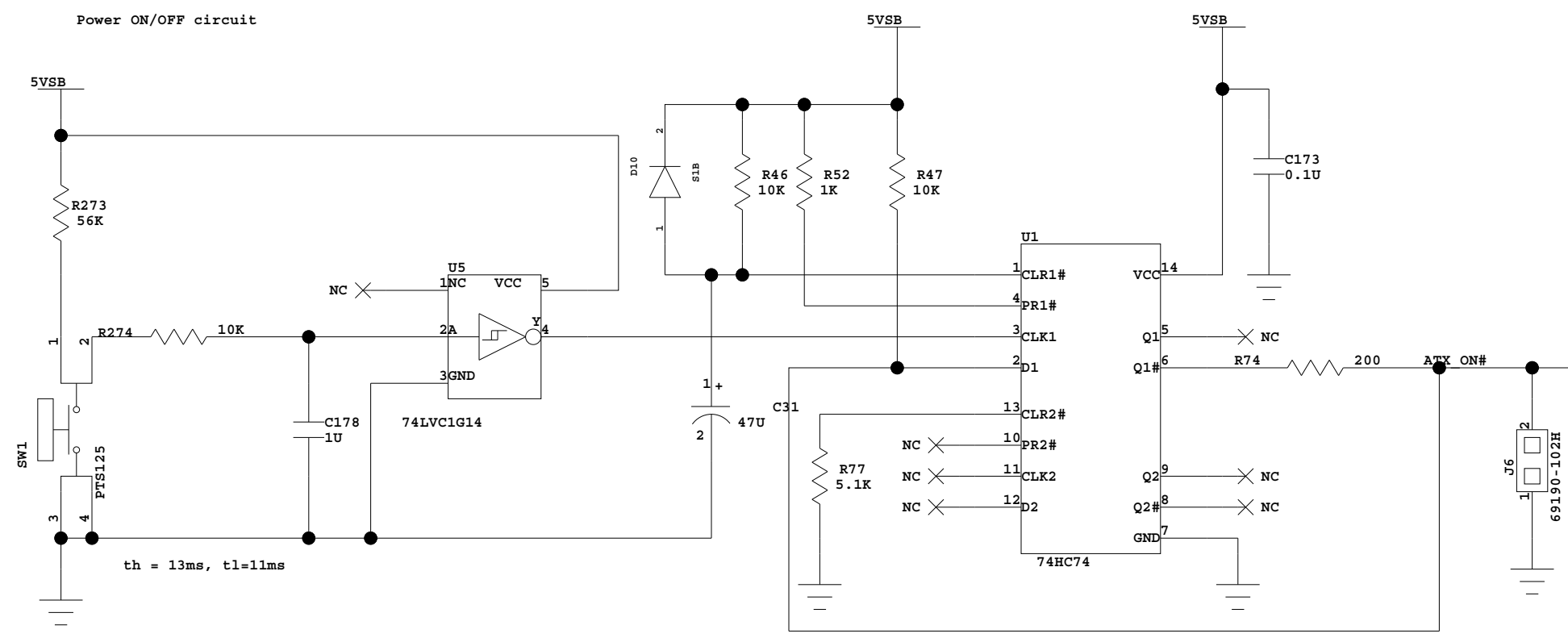
TITLE :			
<b>CLOCK DISTRIBUTION</b>			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
<b>C</b>	60E2000_SC001_03	1.0	
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# POWER SOURCES

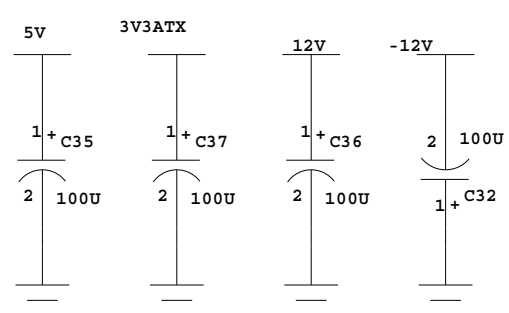
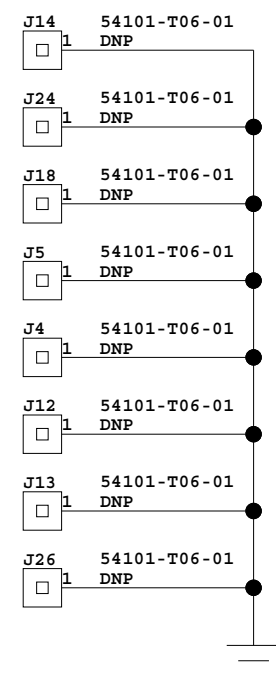
## ATX



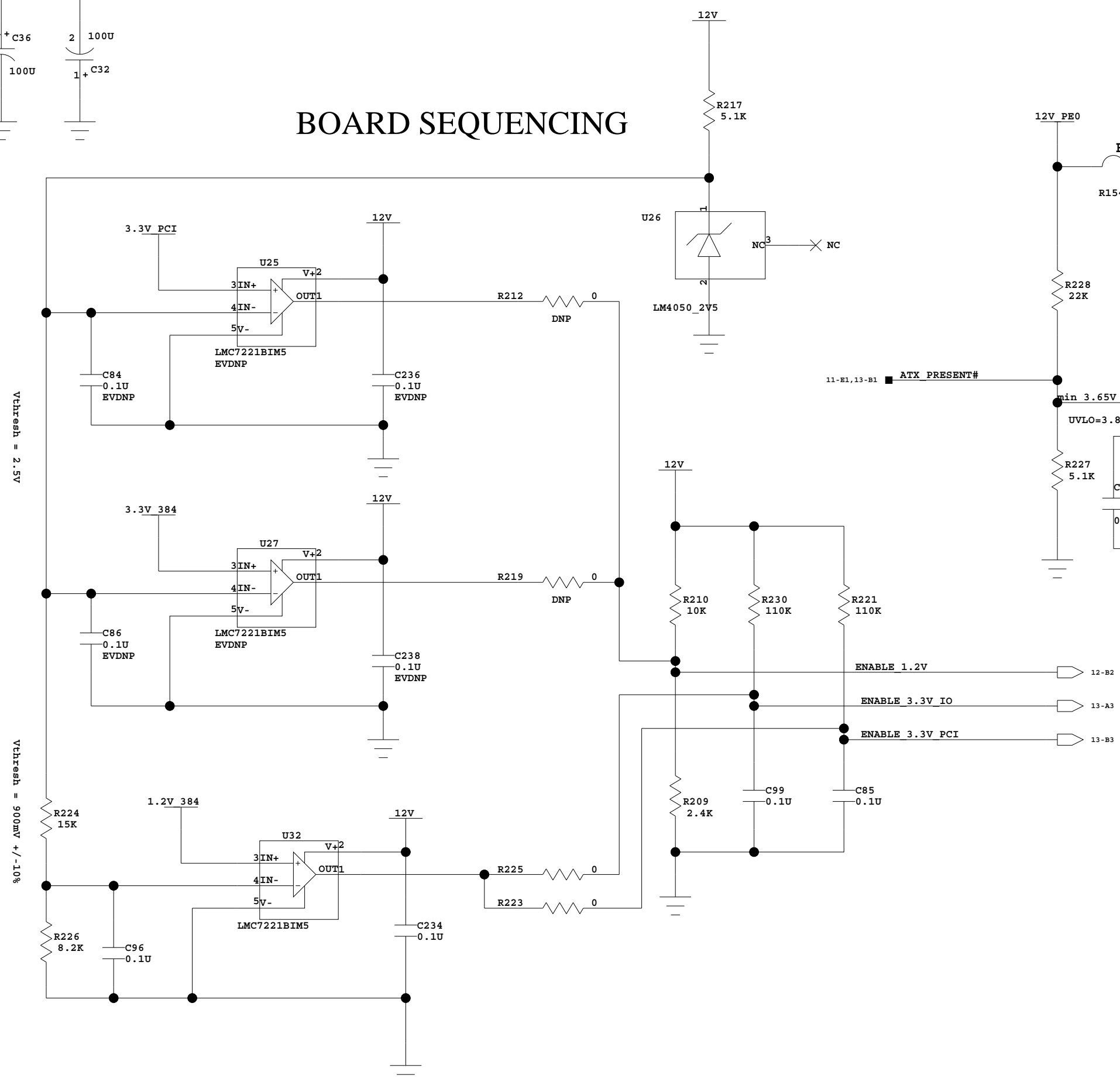
## ATX SUPPLY TOGGLE



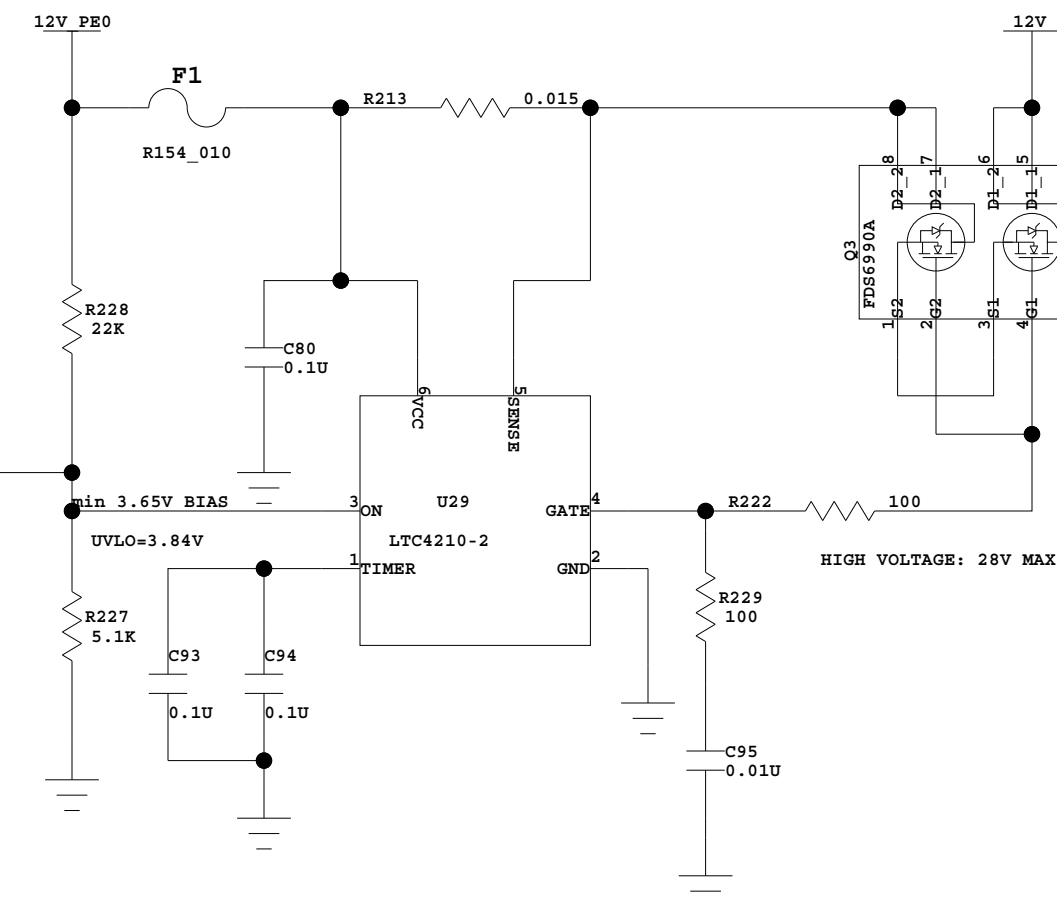
## GND TESTPOINTS



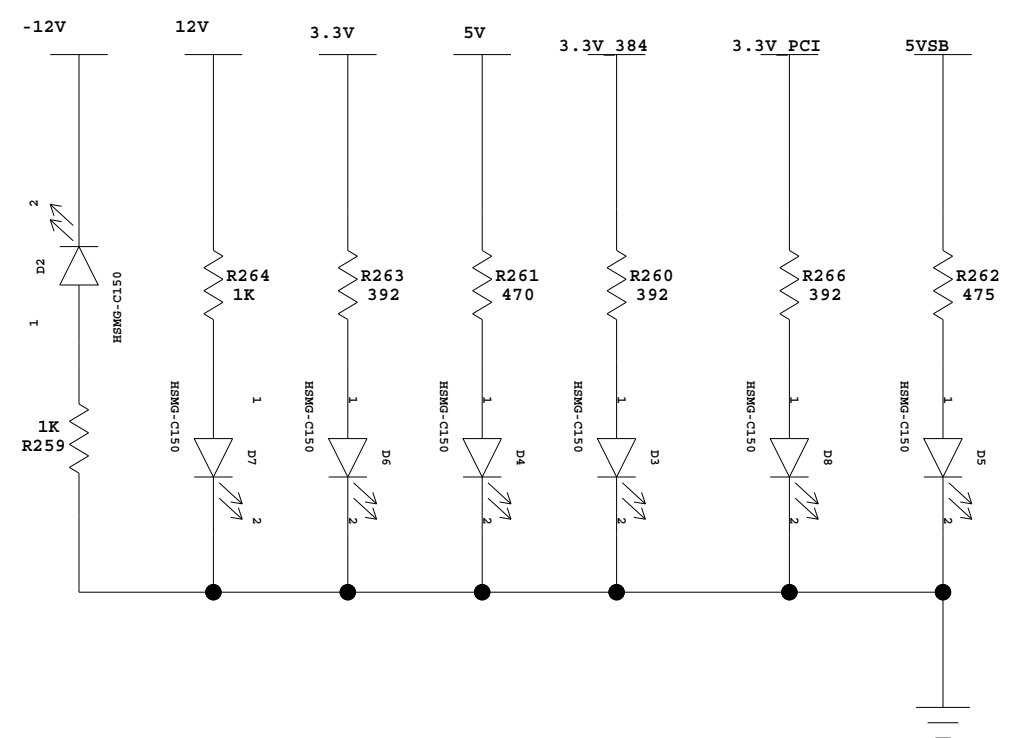
## BOARD SEQUENCING



## SYS SUPPLY SWITCH

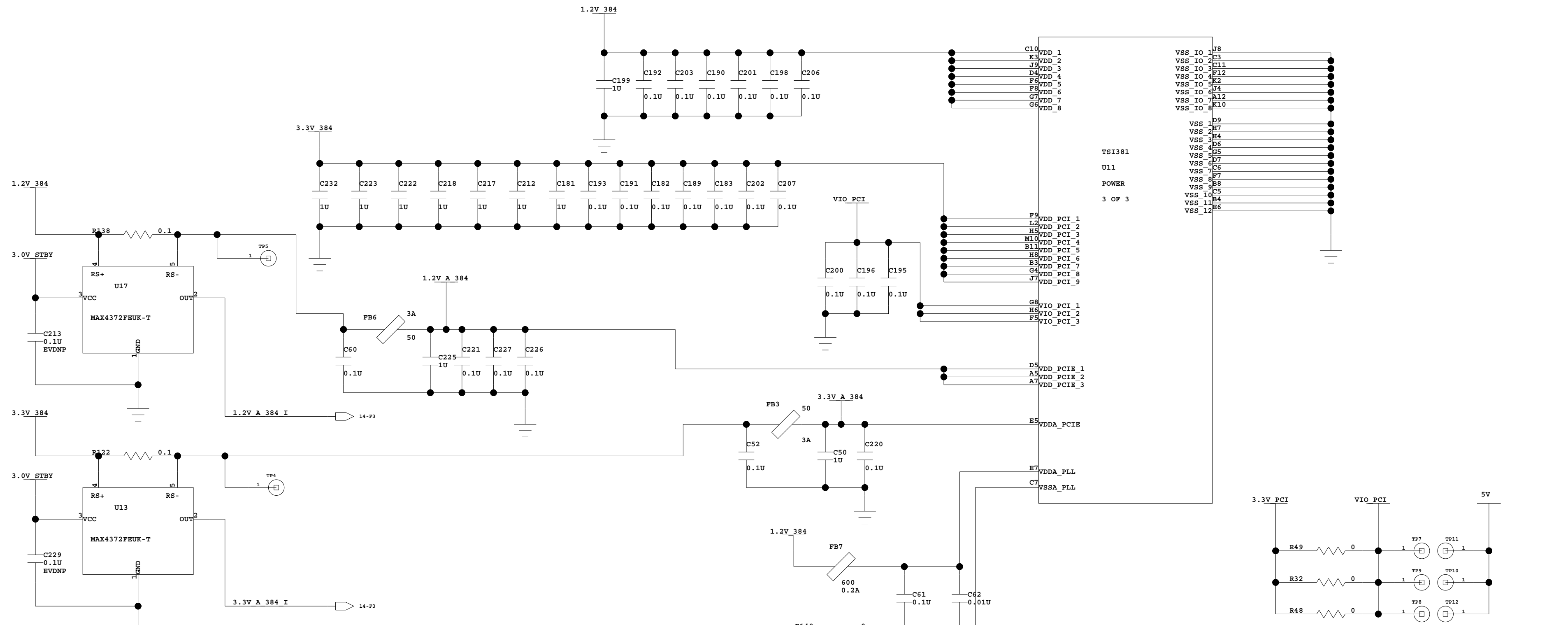


## POWER STATUS



TITLE : <b>POWER SOURCES</b>			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
<b>C</b>	60E2000_SC001_03	1.0	
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# TSI381 POWER/REGULATORS

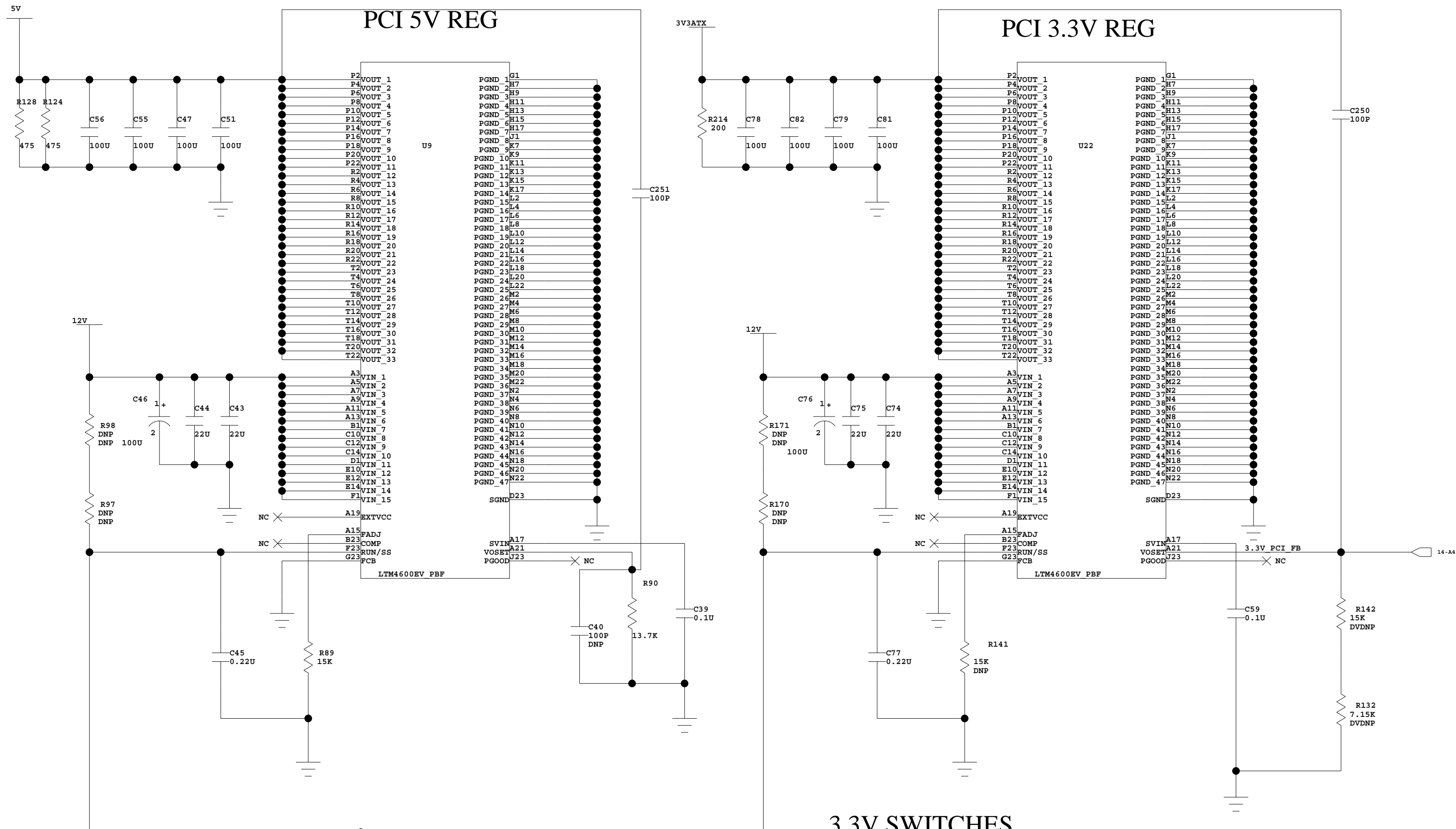


## TSI381 VDD REG

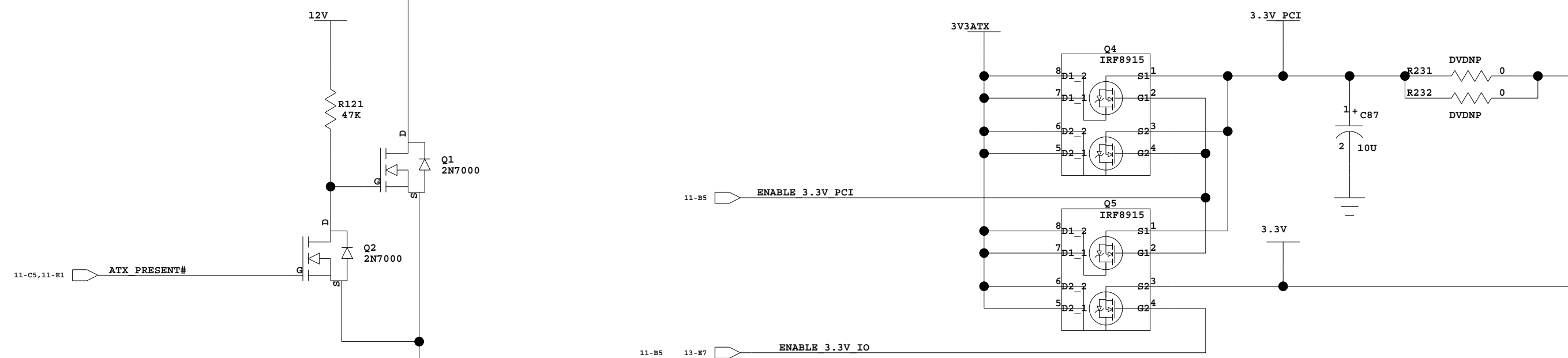
## TSI381 VIO CURRENT SENSE

TITLE :			
Tsi381 POWER/REGULATORS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2000_SCO01_03	1.0	
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# PCI POWER REGULATORS



## 3.3V SWITCHES

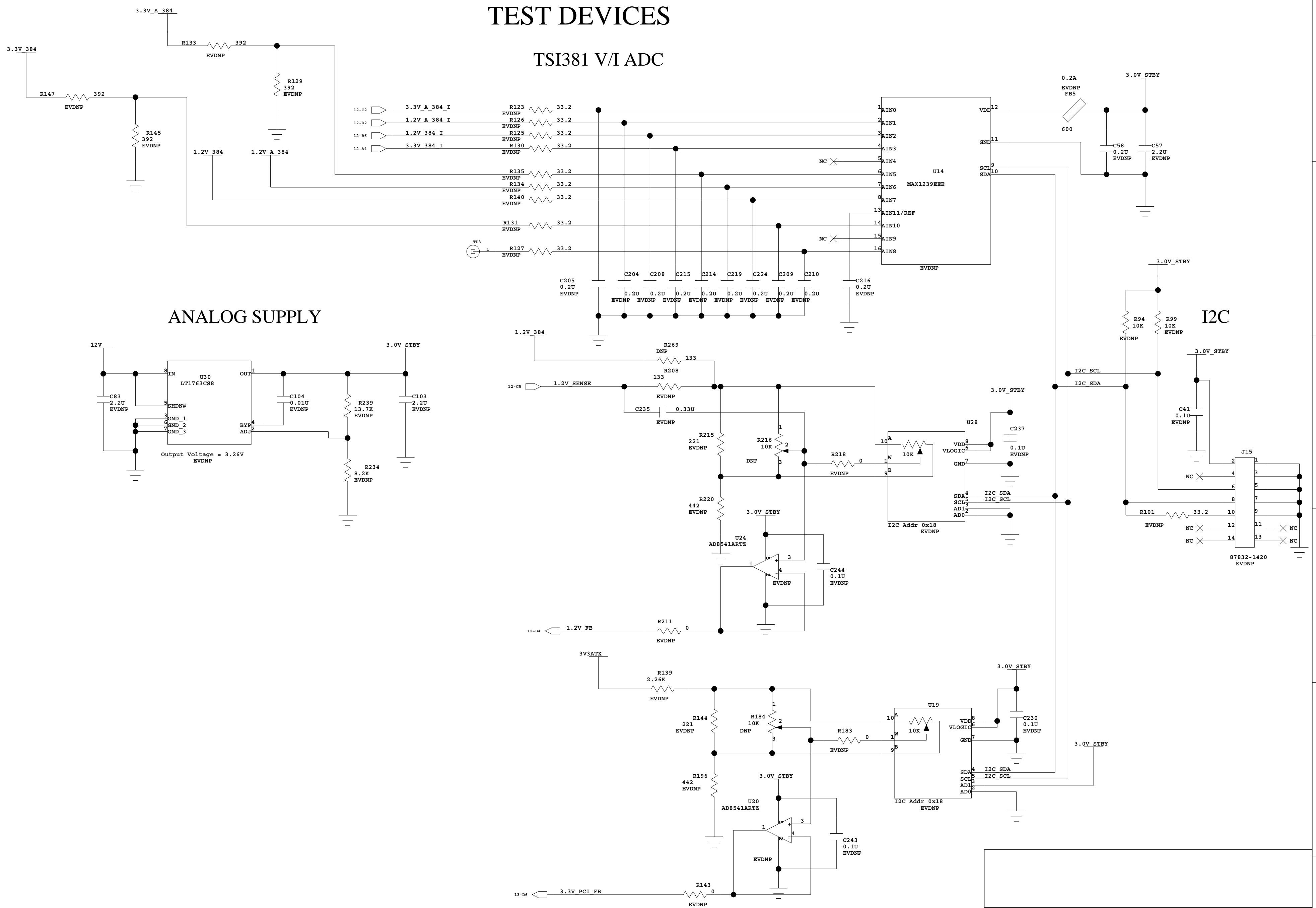


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<b>PCI POWER REGULATORS</b>			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
<b>C</b>	60E2000_SC001_03	1.0	
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# TEST DEVICES

## TSI381 V/I ADC

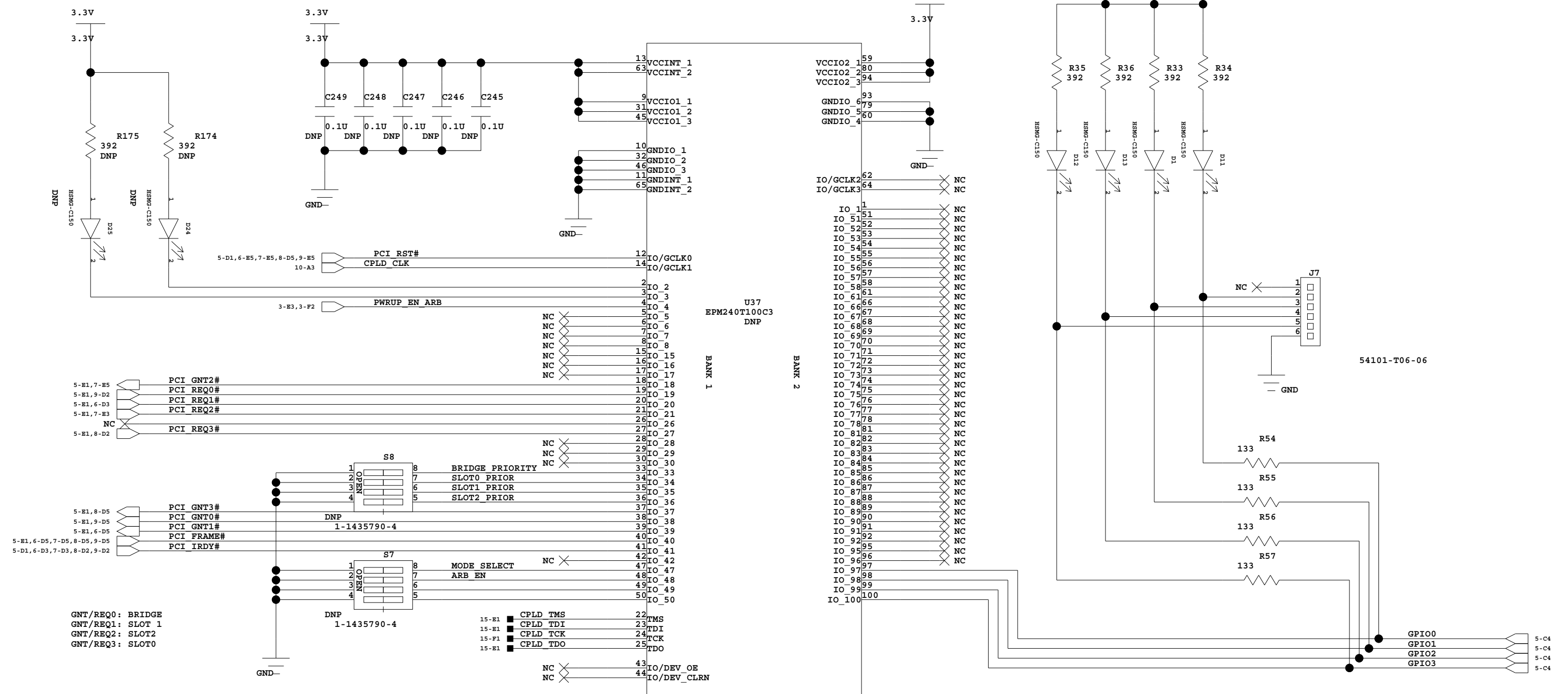
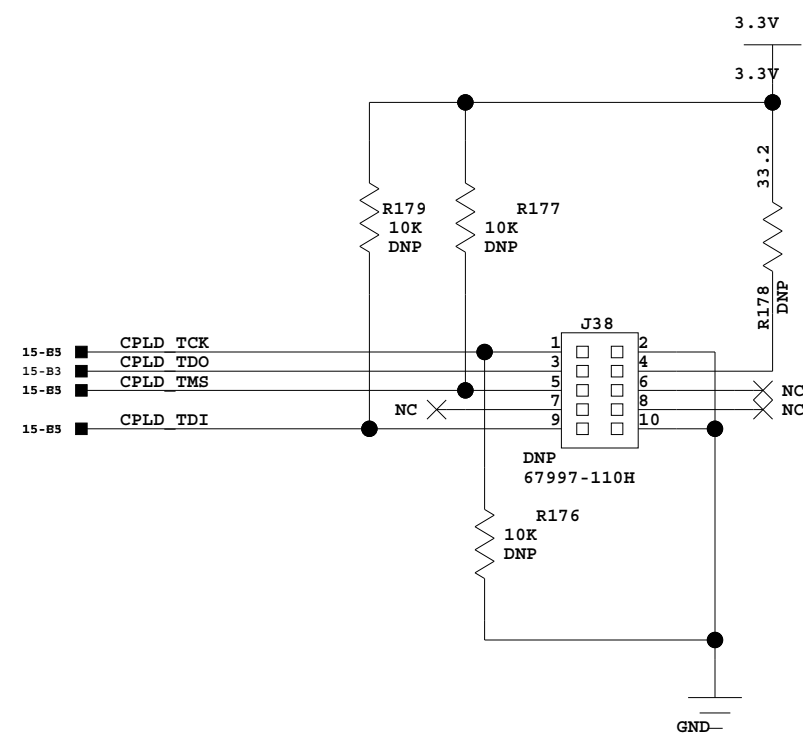
### ANALOG SUPPLY



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<b>TEST DEVICES</b>			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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LAST MODIFIED DATE :			SHEET
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# TEST DEVICES CONT'D

## PCIARBITER/GPIO CONTROL



TITLE :			
TEST DEVICES CONT'D			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2000_SCO01_03	1.0	
LAST MODIFIED DATE :			SHEET
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