

DA1458x Reference Design

Design Name	DA1458xDEVKT-B-VA (QFN40)
Ref. Number	321-4-B
Version	B00
Date	May, 02, 2017
Designer	PR KR

Version	Date	Comments
A00	19 /Oct / 2016	Initial Schematic
A01	02 /Jan / 2017	1. R17, R18, R19: changed from 4.7k to 6.8k 2. U6 inverter NC7SZ04P5X changed to populated
A02	02 /May / 2017	3.Xtall Y2 changed to TXC 9HT11-32.768KDZB-T (6pF)
B00	08 /May / 2018	4. Critical change on the footprint of U4

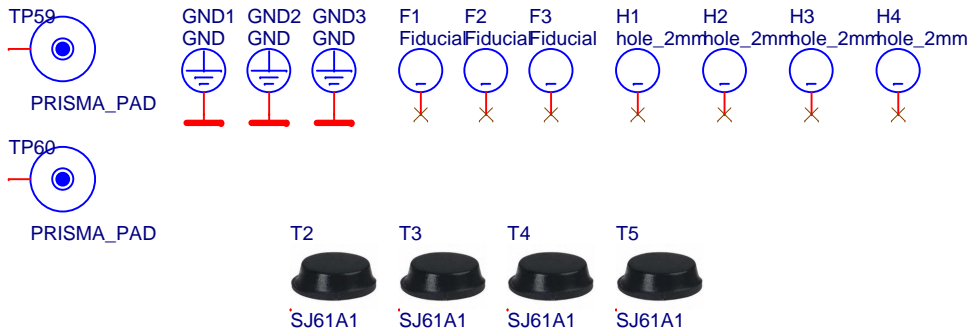
Configuration note

NOTE box

Changes in this Version.

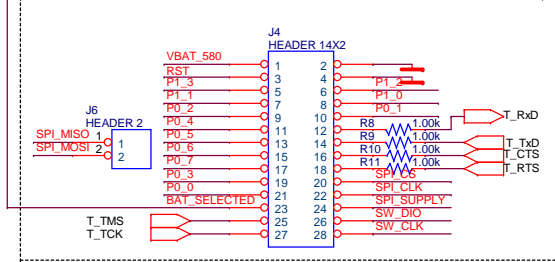
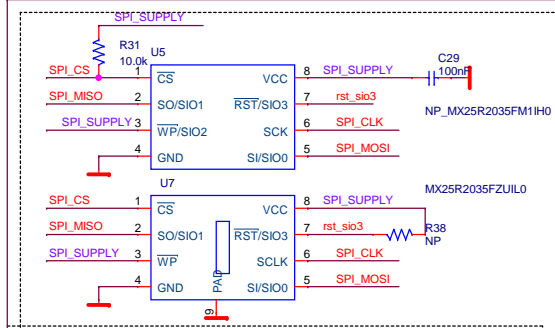


Label_Dialog_L6008

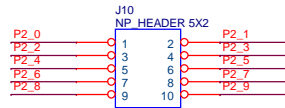


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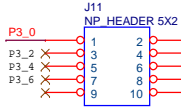
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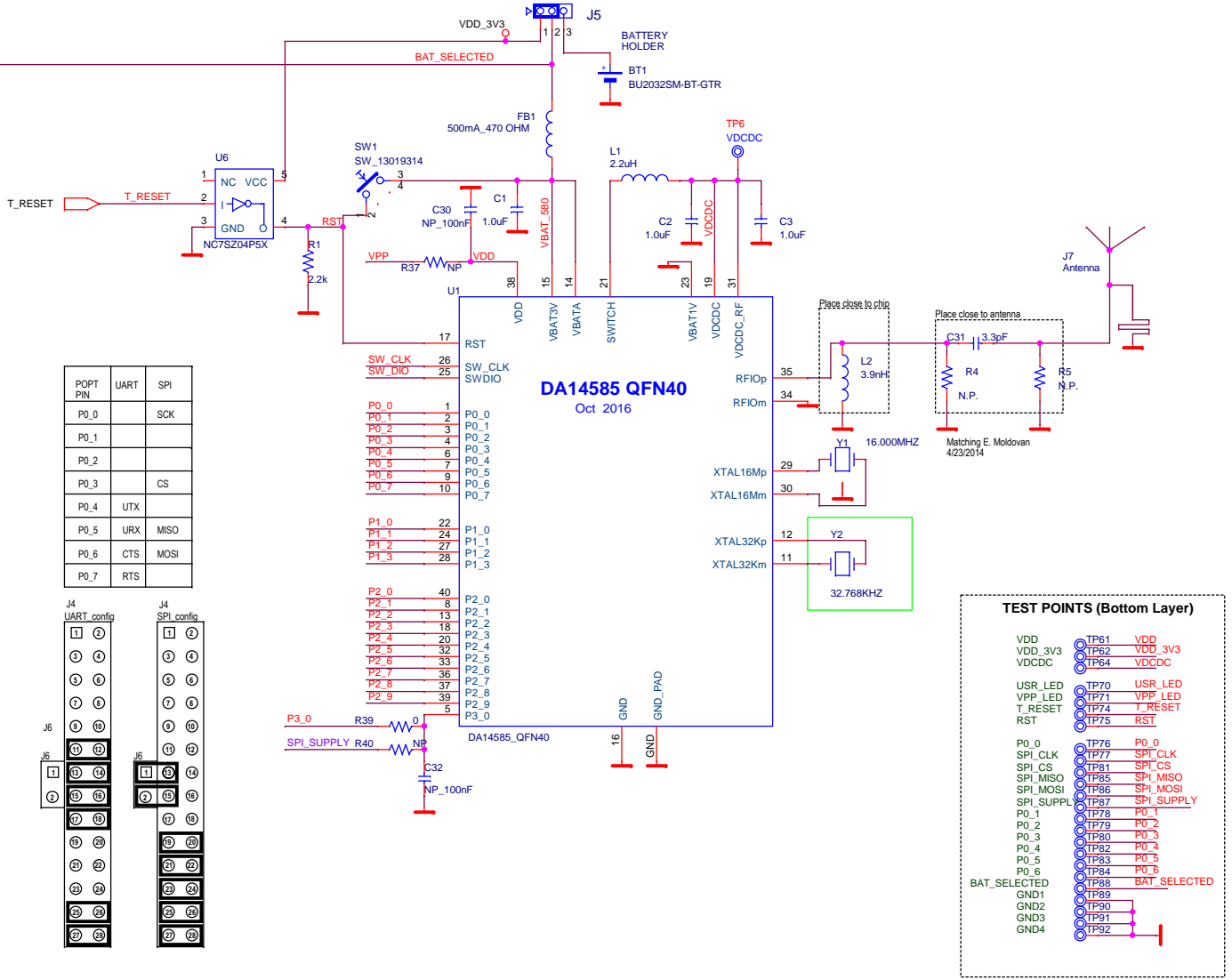
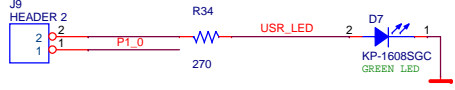
Available on QFN40 - QFN48



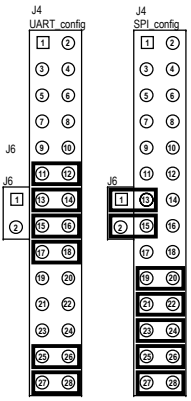
Available on QFN48



User LED



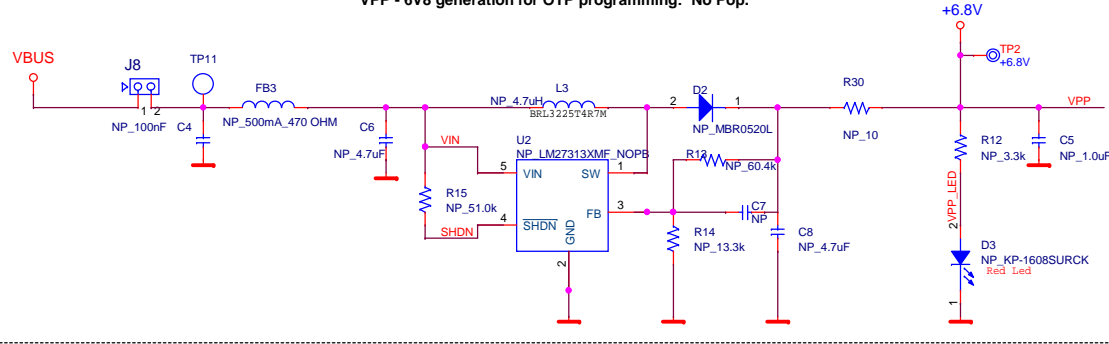
POPT PIN	UART	SPI
P0_0		SCK
P0_1		
P0_2		
P0_3		CS
P0_4	UTX	
P0_5	URX	MISO
P0_6	CTS	MOSI
P0_7	RTS	



TEST POINTS (Bottom Layer)

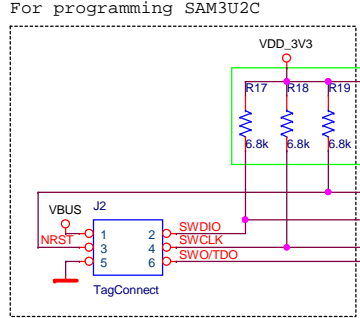
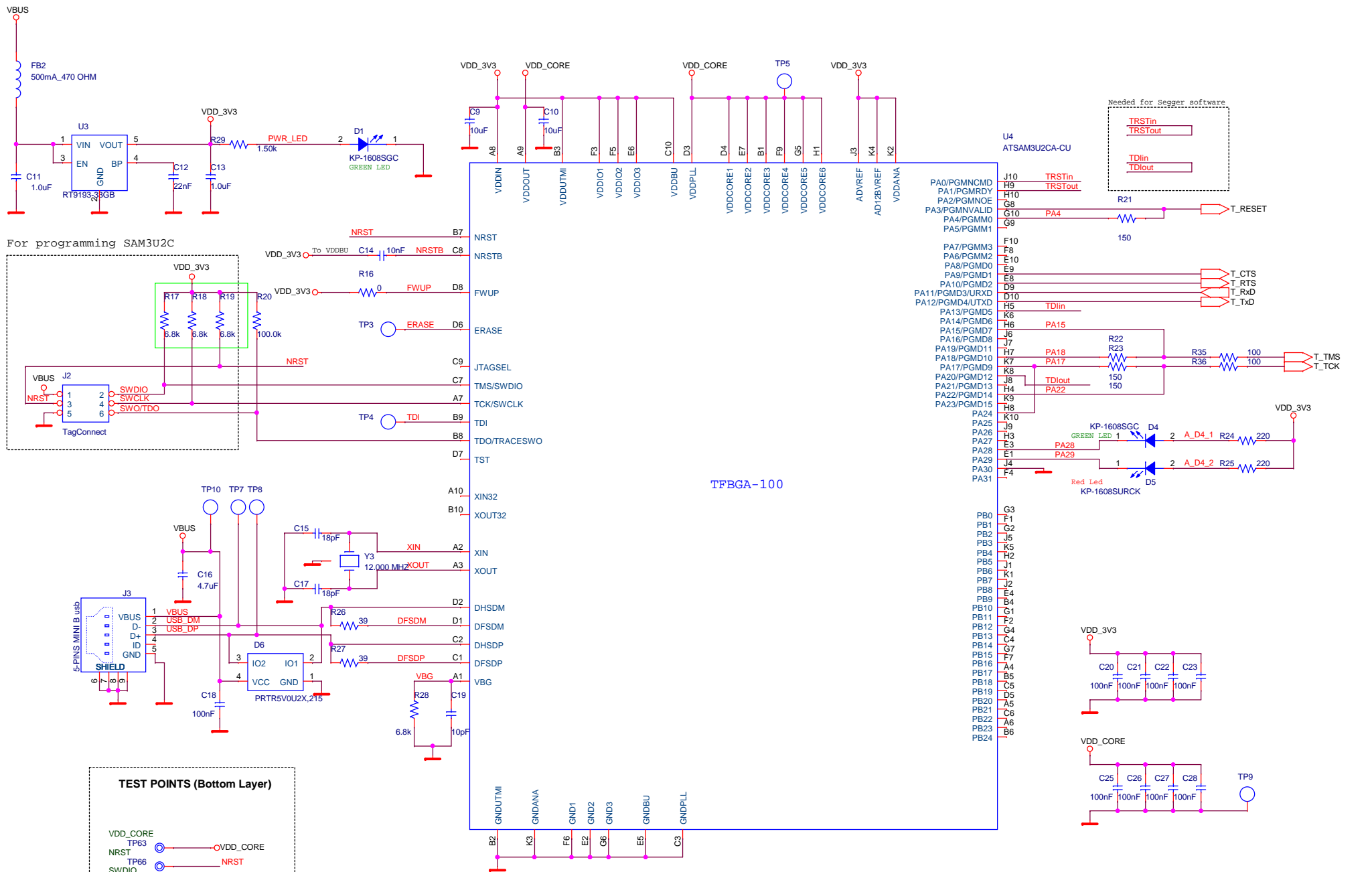
- VDD: TP61
- VDD_3V3: TP62
- VDDCDC: TP64
- USR_LED: TP70
- VPP_LED: TP71
- T_RESET: TP74
- RST: TP75
- P0_0: TP76
- SPI_CLK: TP77
- SPI_CS: TP81
- SPI_MISO: TP85
- SPI_MOSI: TP86
- SPI_SUPPLY: TP87
- P0_1: TP78
- P0_2: TP79
- P0_3: TP80
- P0_4: TP82
- P0_5: TP83
- P0_6: TP84
- BAT_SELECTED: TP88
- GND1: TP89
- GND2: TP90
- GND3: TP91
- GND4: TP92

VPP - 6V8 generation for OTP programming: No Pop.



Description	Configuration				
	to VPP	Decoupl. to VDD	to P3_0	VBAT3V	Decoupl.
580	R37	C30	R39	R40	C32
581	0ohm	NP	NP	NP	NP
583	0ohm	NP	NP	0ohm	100nF
584	0ohm	NP	NP	0ohm	100nF
585 (default)	NP	NP	0ohm	NP	NP
586	NP	NP	NP	0ohm	100nF





TEST POINTS (Bottom Layer)

VDD_CORE	TP63	VDD_CORE
NRST	TP66	NRST
SWDIO	TP67	SWDIO
SWCLK	TP68	SWCLK
ERASE	TP69	ERASE
A_D4_2	TP72	A_D4_2
PWR_LED	TP73	PWR_LED

Needed for Segger software

TRSTin
TRSTout

TDlin
TDlout

dialog SEMICONDUCTOR

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