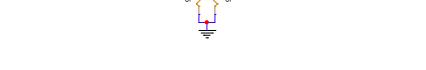
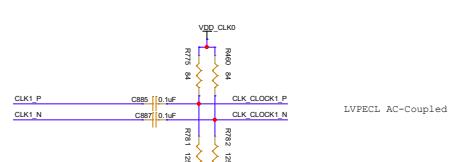
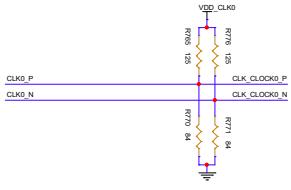


Input Termination Example: Put it close to 8A34001

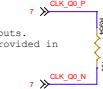


The above input termination of CLK0~CLK3 can be used for CLK4~CLK7.

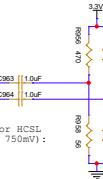
LVPECL DC-Coupled  
Note: if the driver is the 8A34x chip, do not use this termination scheme.  
Use the LVDS terminations scheme.

Output Termination Example: Put it close to the receiver side

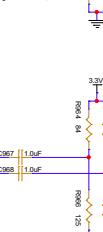
Termination scheme for dc-coupled differential outputs.  
This should be used for the standard selections provided in  
the GUR, such as LVPECL (2.3V/3.3V) or LVDS



Example Termination for HCSL  
(set the Amplitude to 750mV):



Example Termination for CML:  
(Set output to 750mV amplitude)



Example Termination for ac-coupling to a 3.3V LVPECL receiver.  
Note that no pull-downs are used at the driver.

The above output termination of Q0-Q3 can be used for Q4-Q11.

USA	
CLK_CLOCK0_P	B1
CLK_CLOCK0_N	C1
CLK_CLOCK1_P	D1
CLK_CLOCK1_N	E1
CLK_CLOCK2_P	F1
CLK_CLOCK2_N	G1
CLK_CLOCK3_P	H1
CLK_CLOCK3_N	I1
CLK_CLOCK4_P	J1
CLK_CLOCK4_N	K1
CLK_CLOCK5_P	L1
CLK_CLOCK5_N	M1
CLK_CLOCK6_P	N1
CLK_CLOCK6_N	O1
CLK_CLOCK7_P	P1
CLK_CLOCK7_N	Q1
Q0_P	A6
Q0_N	B6
Q1_P	C6
Q1_N	D6
Q2_P	E6
Q2_N	F6
Q3_P	G6
Q3_N	H6
Q4_P	I6
Q4_N	J6
Q5_P	K6
Q5_N	L6
Q6_P	M6
Q6_N	N6
Q7_P	O6
Q7_N	P6
Q8_P	R6
Q8_N	S6
Q9_P	T6
Q9_N	U6
Q10_P	V6
Q10_N	W6
Q11_P	X6
Q11_N	Y6

The Simple Ref Design of the Clock Matrix		
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