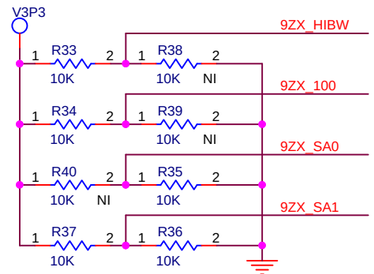
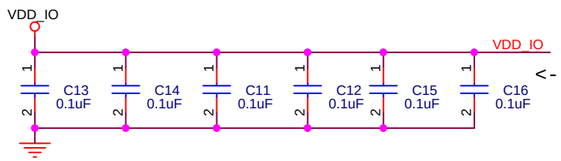
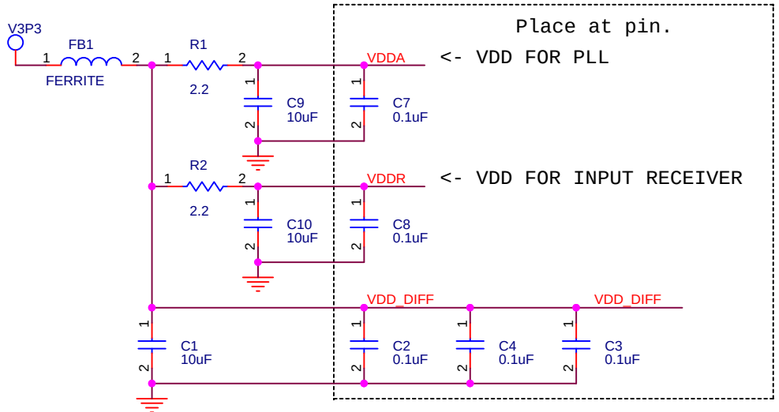


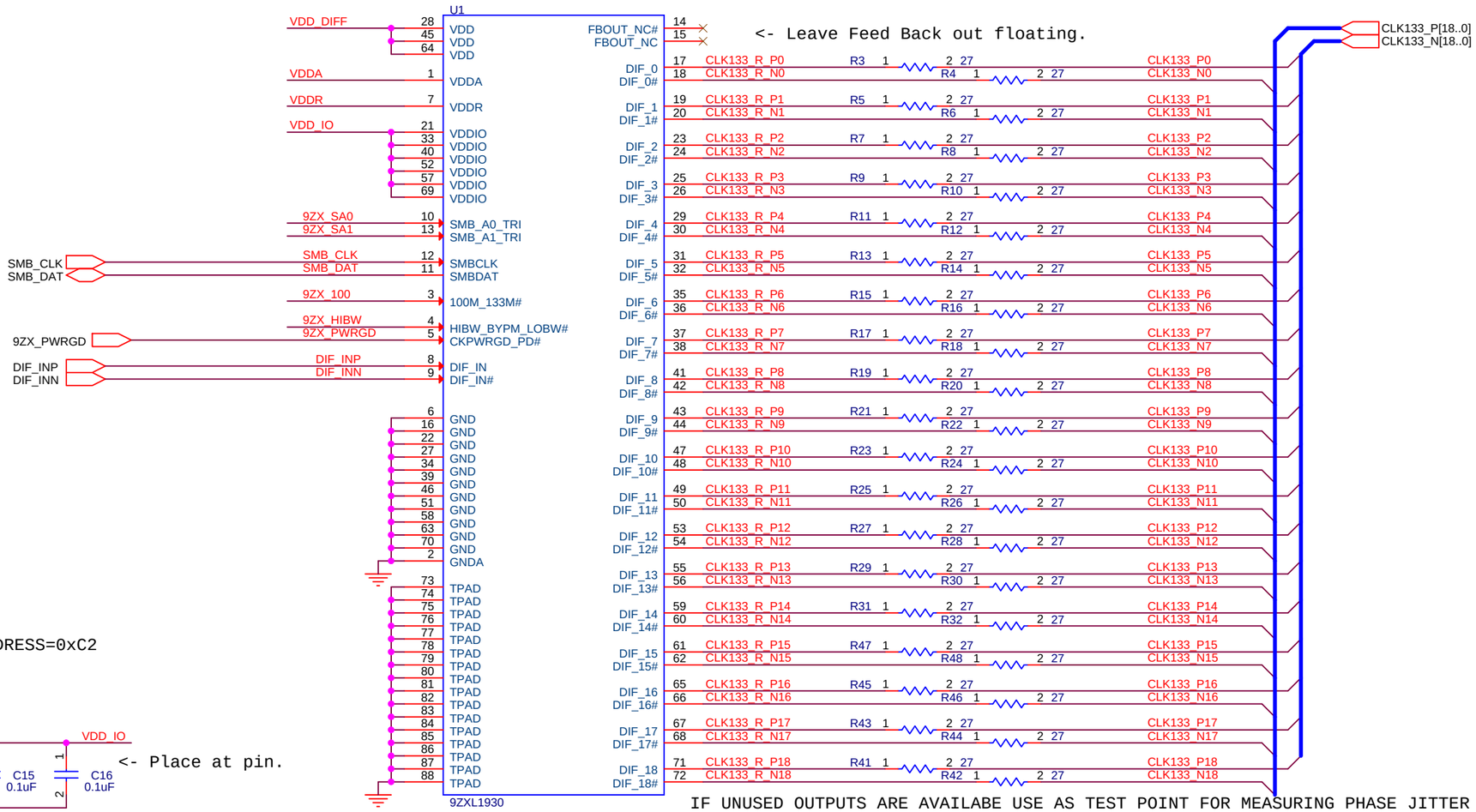
CONFIGURATION SHOWN =
HIGH_BANDWIDTH, 100 MHz, SMBus ADDRESS=0xC2

VDD_IO May be 1.05 to 3.3 volts



<- Place at pin.





<- Leave Feed Back out floating.

IF UNUSED OUTPUTS ARE AVAILABE USE AS TEST POINT FOR MEASURING PHASE JITTER

HiBW BypM LoBW#	MODE
Low	PLL Lo BW
Mid	Bypass
High	PLL Hi BW

NOTE: PLL is OFF in Bypass Mode

Impedance dependent resistor values

Resistor	Zdiff = 100 ohm	Zdiff = 85 ohm
Series	33 5%	27 5%

NOTE:FERRITE BEADS =

Manufacture	Part Number	Z@100MHz	PkgSz	DC res.	Current(Ma)
muRata	BLM21AG601SN1	600	0805	0.30	600
TDK	MMZ2012S601A	600	0805	0.30	600
STEWARD	HZ0805E601R	600	0805	0.30	600
AssocCmpTch	CBG0805-600-50	600	0805	0.30	600

Tri-Level

SMB_A1	SMB_A0	Add
0	0	D8
0	M	DA
0	1	DE
M	0	C2
M	M	C4
M	1	C6
1	0	CA
1	M	CC
1	1	CE

Revision history

Rev	Change
0.1	First publication

Integrated Device Technology
6024 Silver Creek Valley Road
San Jose, CA

Title: 9ZXL1930		
Size: B	Document Number	Rev: 0.2
Date: Thursday, June 15, 2017	Sheet 1 of 1	