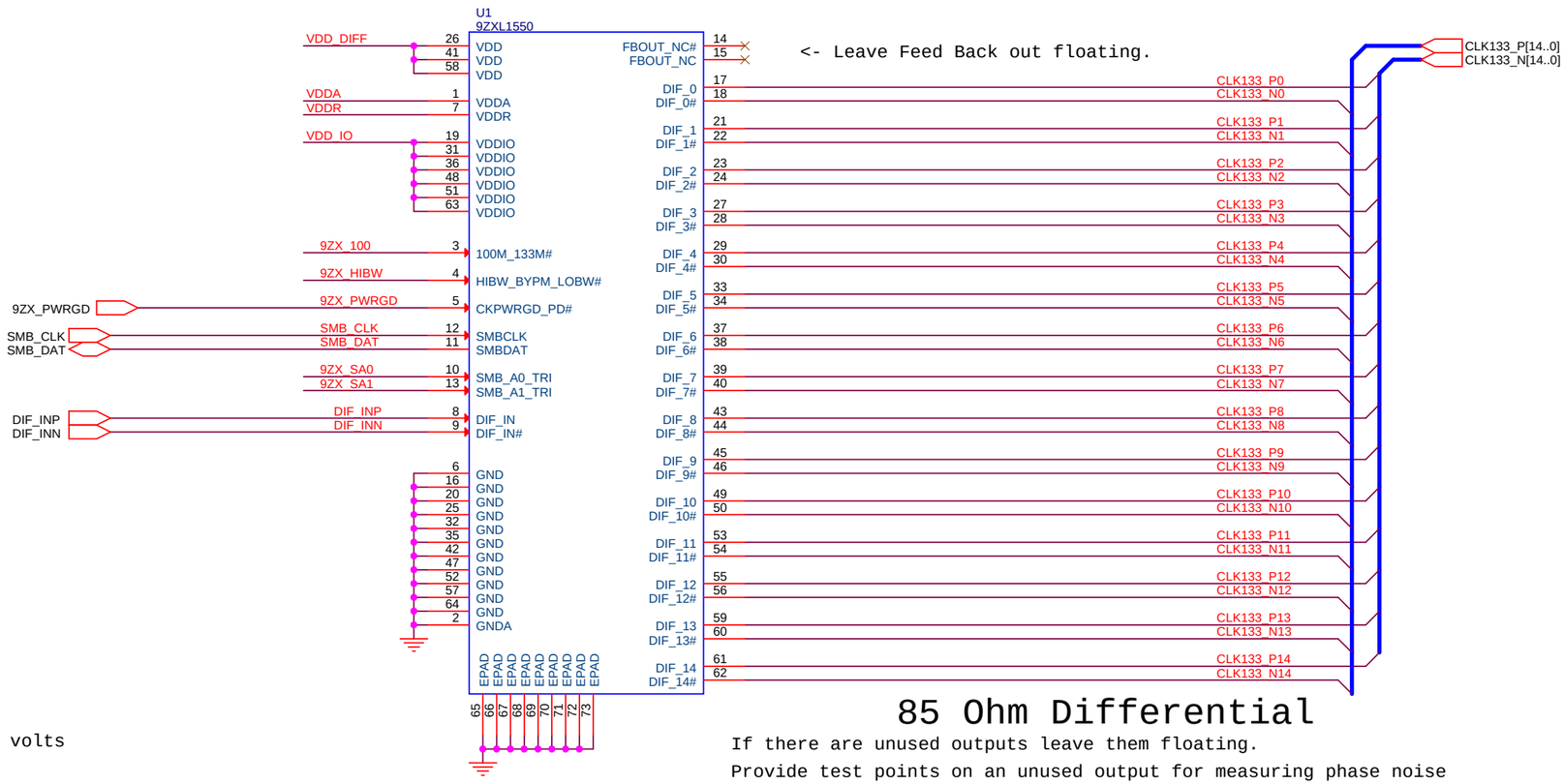
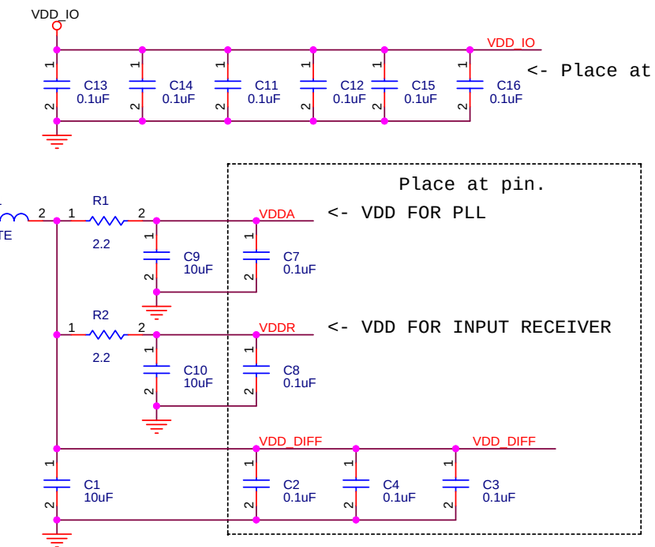


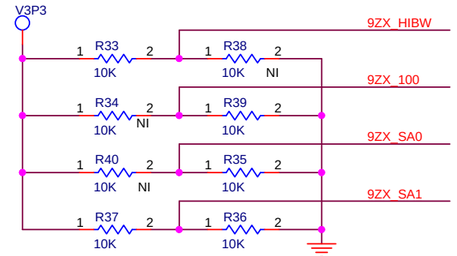
85 Ohm Differential

If there are unused outputs leave them floating.

Provide test points on an unused output for measuring phase noise

VDD_IO May be 1.05 to 3.3 volts





HiBW_BypM_LoBW#	MODE
Low	PLL Lo BW
Mid	Bypass
High	PLL Hi BW

NOTE: PLL is OFF in Bypass Mode

SMB_A1	SMB_A0	Add
Tri-Level		
0	0	D8
0	M	DA
0	1	DE
M	0	C2
M	M	C4
M	1	C6
1	0	CA
1	M	CC
1	1	CE

NOTE:FERRITE BEADS =

Manufacture	Part Number	Z@100MHz	PkgSz	DC res	Current(Ma)
muRata	BLM21A601R	600	0805	0.30	600
TDK	MMZ2012S601A	600	0805	0.30	600
STEWARD	HZ0805E601R	600	0805	0.30	600
AssocCmpTch	CBG0805-600-50	600	0805	0.30	600

CONFIGURATION SHOWN =
HIGH_BANDWIDTH, 133 MHz, SMBus ADDRESS=0xC2

Revision history

Rev	Change
0.1	First publication
0.2	Changed 1 uF caps to 10 uF

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Title		
9ZXL1550		
Size B	Document Number	Rev 0.2
Date: Thursday, August 24, 2017	Sheet 1 of 1	