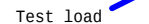


## Layout notes

1. Separate Xout and Xin traces by at least 3 x the trace width.
2. Do not share crystal load capacitor ground via with other components.
3. Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
4. Do not share ground vias. One ground pin one ground via.
5. Exposed pad should be grounded but is not required.



Vdd3P3 SW1

1 VCC

8 VEE

s1  
s2  
s3  
s4  
s5  
s6  
s7

16 FGROE 0 R3 1 2 10K FG OE 0

15 FGROE 1 R4 1 2 10K FG OE 1

14 FGROE 3:2 R6 1 2 10K FG OE 3:2

13 FGROE 5:4 R7 1 2 10K FG OE 5:4

12 FGROE 7:6 R8 1 2 10K FG OE 7:6

11 SMB ADD

10 CKRPD# R10 1 2 10K FG PD#

9 FG RSS EN R11 1 2 10K FG SS EN

For VddIO pins.

