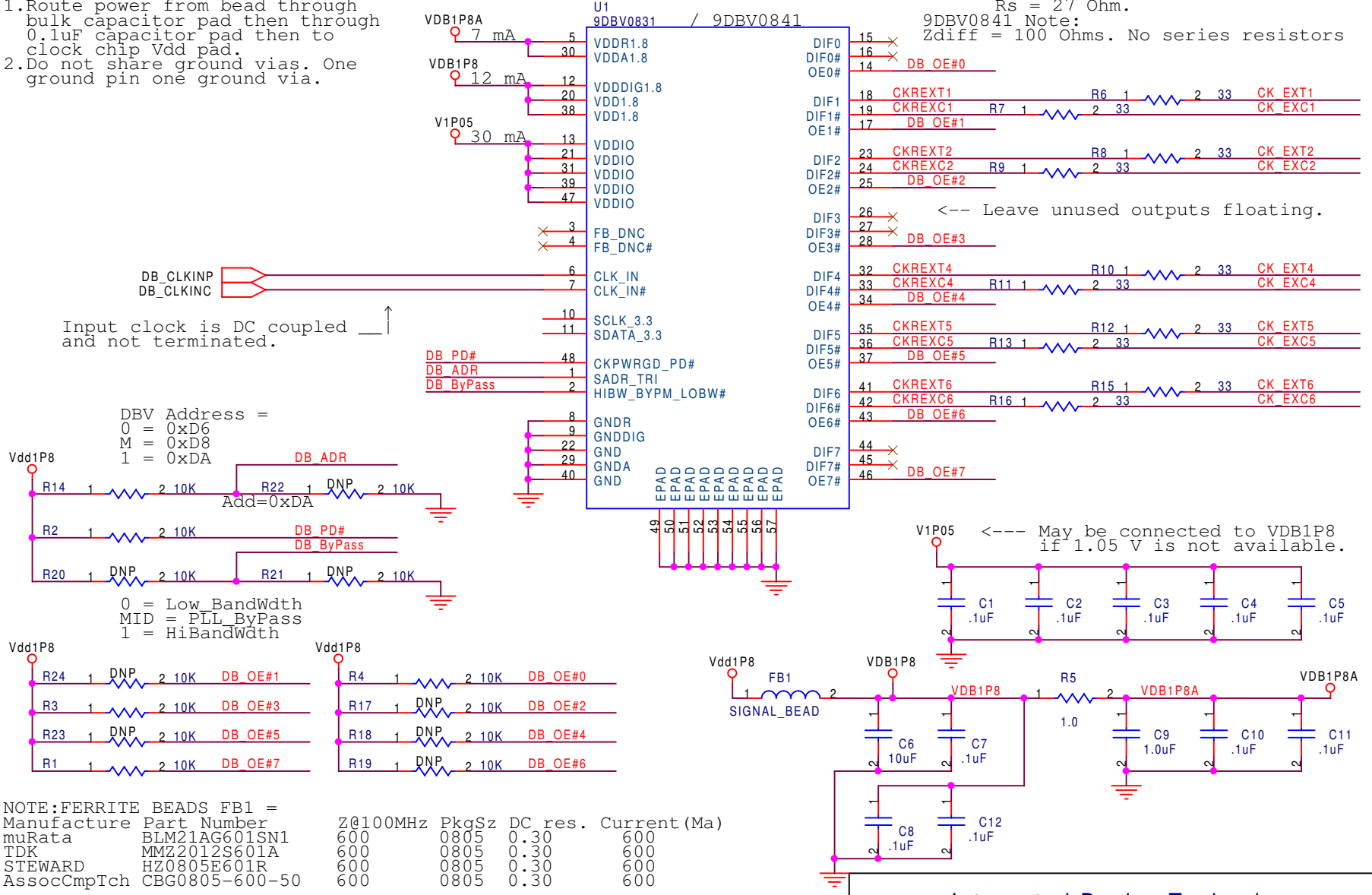
Layout notes.
1.Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
2.Do not share ground vias. One ground pin one ground via.

9DBV0831 Note: TO CONFIGURE FOR Zdiff = 85 Ohms Rs = 27 Ohm.
9DBV0841 Note: Zdiff = 100 Ohms. No series resistors



<-- Leave unused outputs floating.

Input clock is DC coupled and not terminated.

DBV Address =
0 = 0xD6
M = 0xD8
1 = 0xDA

0 = Low_BandWdth
MID = PLL_ByPass
1 = HiBandWdth

V1P05 <--- May be connected to VDB1P8 if 1.05 V is not available.

NOTE:FERRITE BEADS FB1 =

Manufacture	Part Number	Z@100MHz	PkgSz	DC res.	Current(Ma)
muRata	BLM21AG601SN1	600	0805	0.30	600
TDK	MMZ2012S601A	600	0805	0.30	600
STEWARD	HZ0805E601R	600	0805	0.30	600
AssocCmpTch	CBG0805-600-50	600	0805	0.30	600

Manufacture	Part Number	Z@100MHz	PkgSz	DC res.	Current(Ma)
muRata	BLM18AG601SN1	600	0603	0.50	200
muRata	BLM18BD601SN1_PB	600	0603	0.65	200
Ceratech	HB-1T1608-601	600	0603	0.50	200
TDK	MMZ1608R301A	300	0603	0.20	500

Integrated Device Technology
San Jose, CA

Size	Document Number	Rev
A	9DBV0831 / 9DBV0841	0.2

Date: Friday, July 18, 2014 Sheet 1 of 1