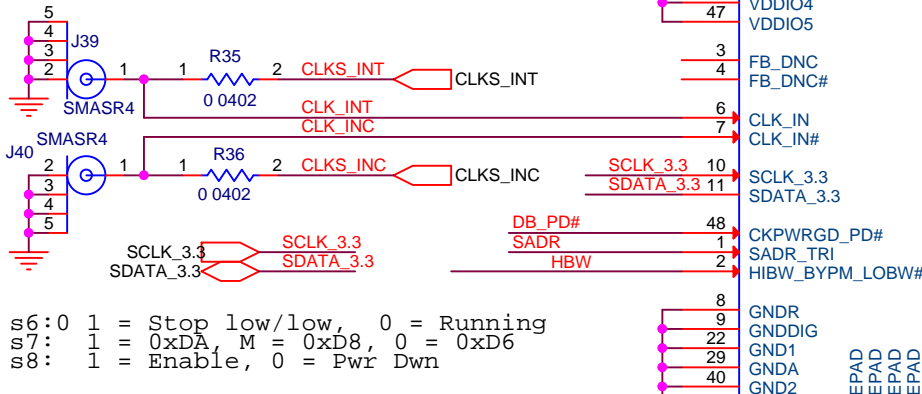
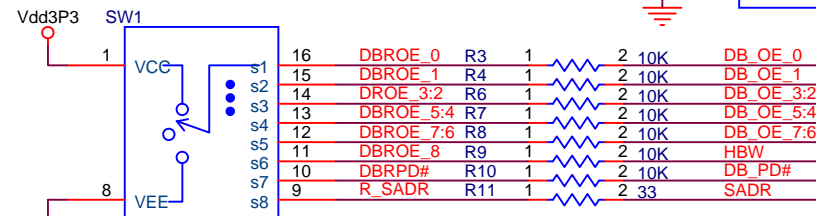


Layout notes.

- Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
- Do not share ground vias. One ground pin one ground via.
- Exposed pad should be grounded but is not required.

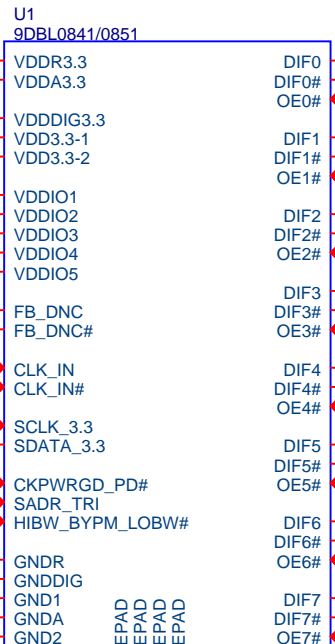
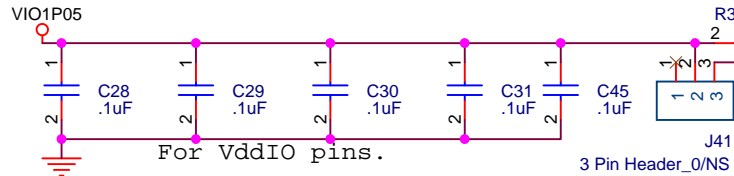


s6:0 1 = Stop low/low, 0 = Running  
 s7: 1 = 0xDA, M = 0xD8, 0 = 0xD6  
 s8: 1 = Enable, 0 = Pwr Dwn



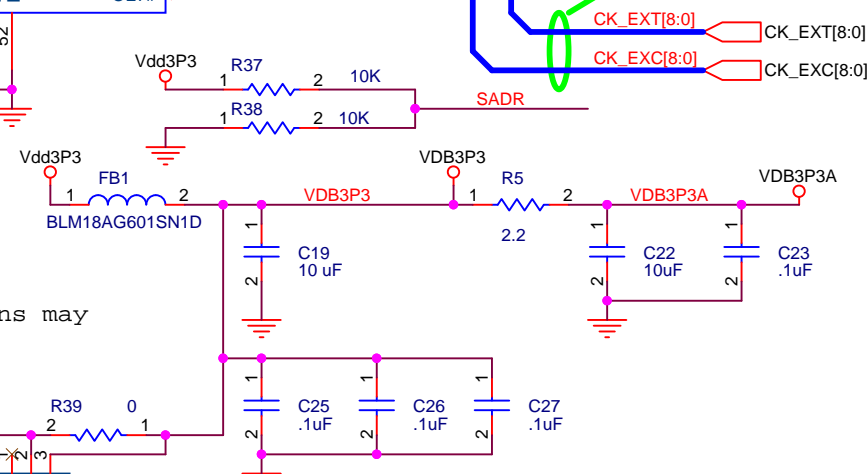
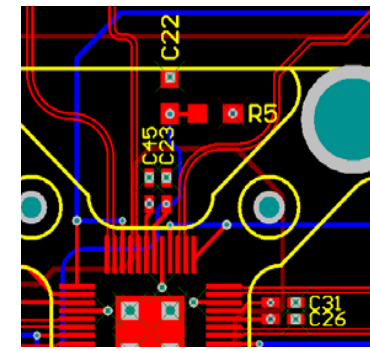
May be connected to VDB3P3 if 1.05 V is not available.

If 3.3 V is used for VddIO these Vdd pins may share the same bypass capacitor.  
 12 & 13. 20 & 21. 38 & 39.



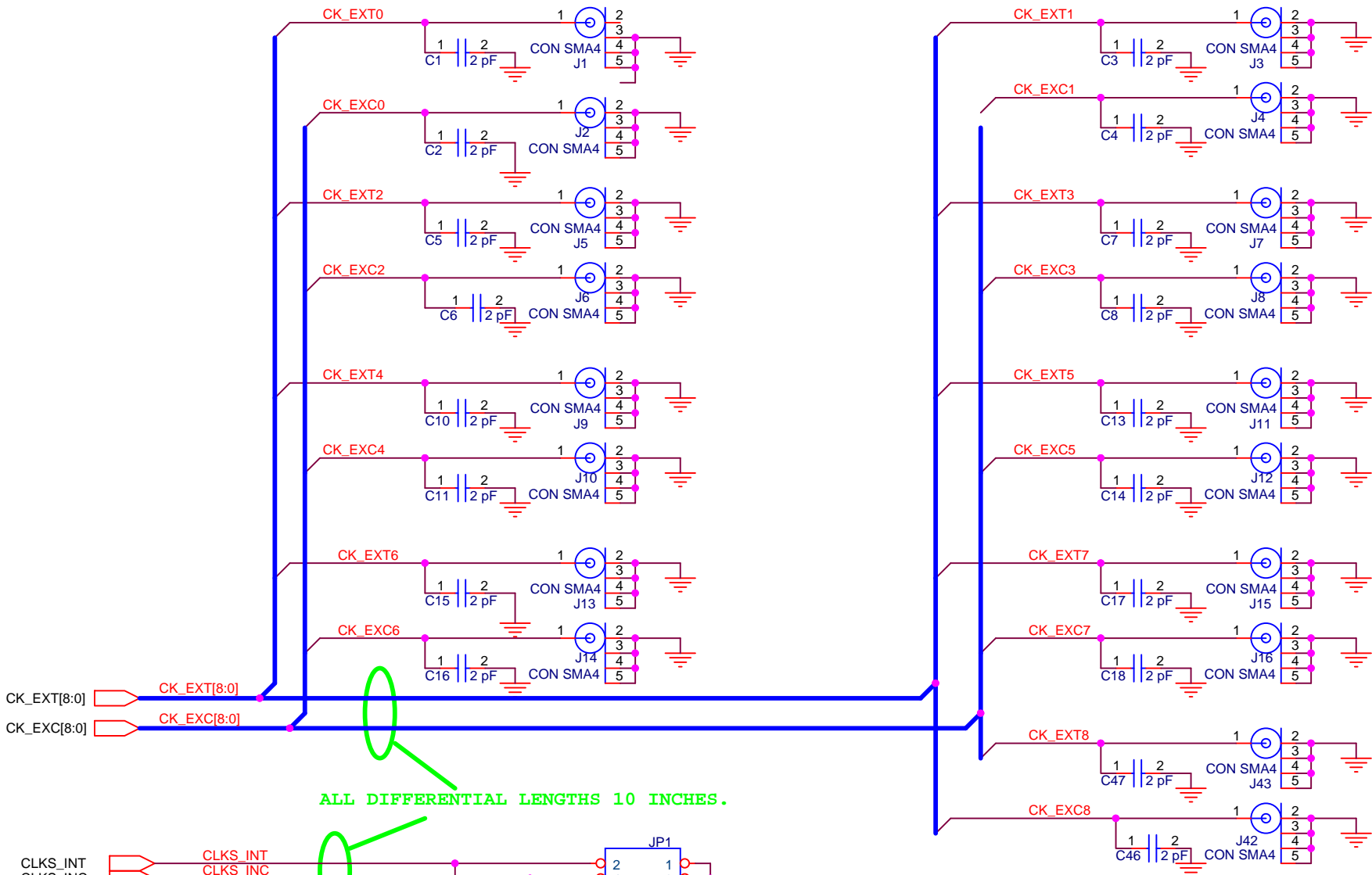
9DBL0841:  
 100 Ohms Differential

9DBL0851:  
 85 Ohms Differential



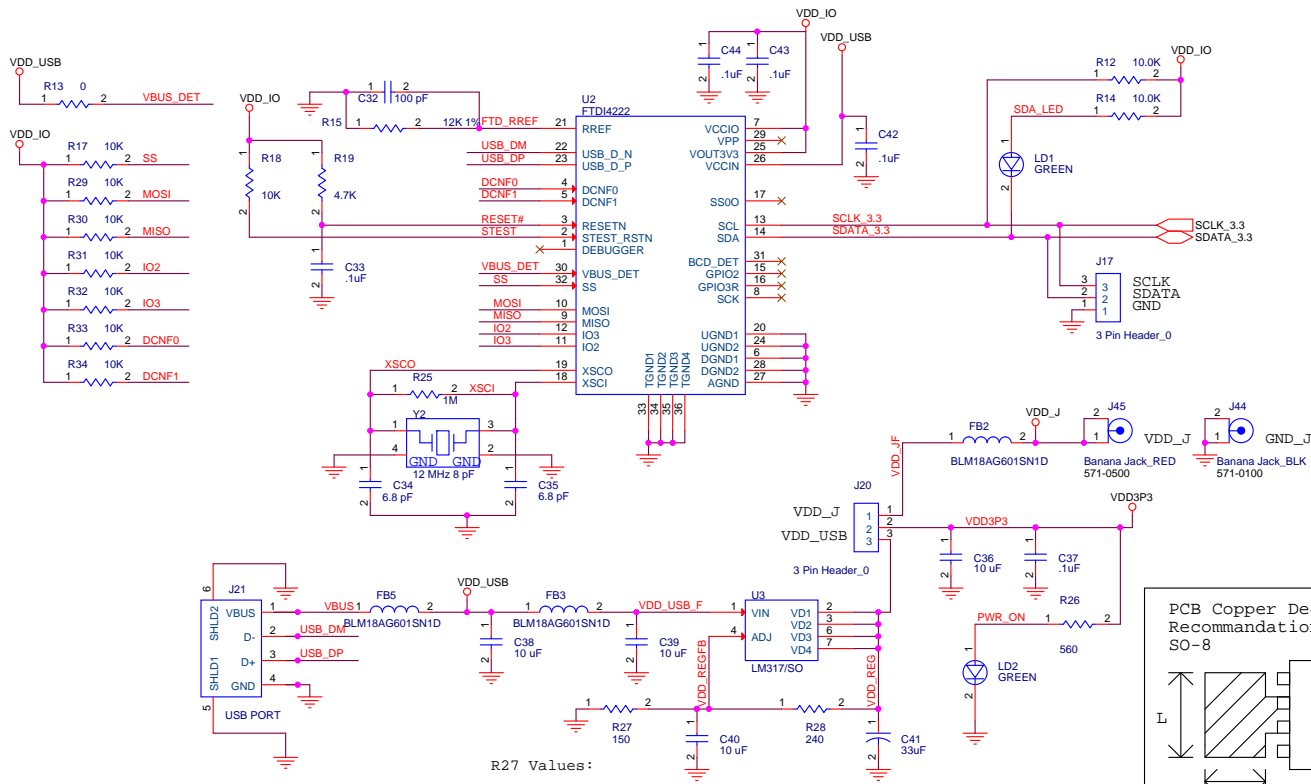
**Integrated Device Technology**  
 San Jose, CA

Size A	Document Number 9DBL08	Rev 0.4
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Integrated Device Technology		
Title 9DBL0851 Test Loads		
Size A	Document Number <Doc>	Rev 0.2
Date: Friday, June 15, 2018	Sheet 2	of 3

- FID1 Fiducial
- FIDUCIAL
- FID2 Fiducial
- FIDUCIAL
- FID3 Fiducial
- FIDUCIAL
- MTH#6\_1 NS/MOUNTING HOLE
- MTH#6\_2 NS/MOUNTING HOLE
- MTH#6\_3 NS/MOUNTING HOLE
- MTH#6\_4 NS/MOUNTING HOLE
- LOGO\_IDT1 IDT



R27 Values:  
 VDD=1.5V: R22=1.2K  
 VDD=1.8V: R22=560  
 VDD=2.5V: R22=240  
 VDD=3.3V: R22=150

