

REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
	1.0	INITIAL RELEASE	2009-12-05	T. TRAN

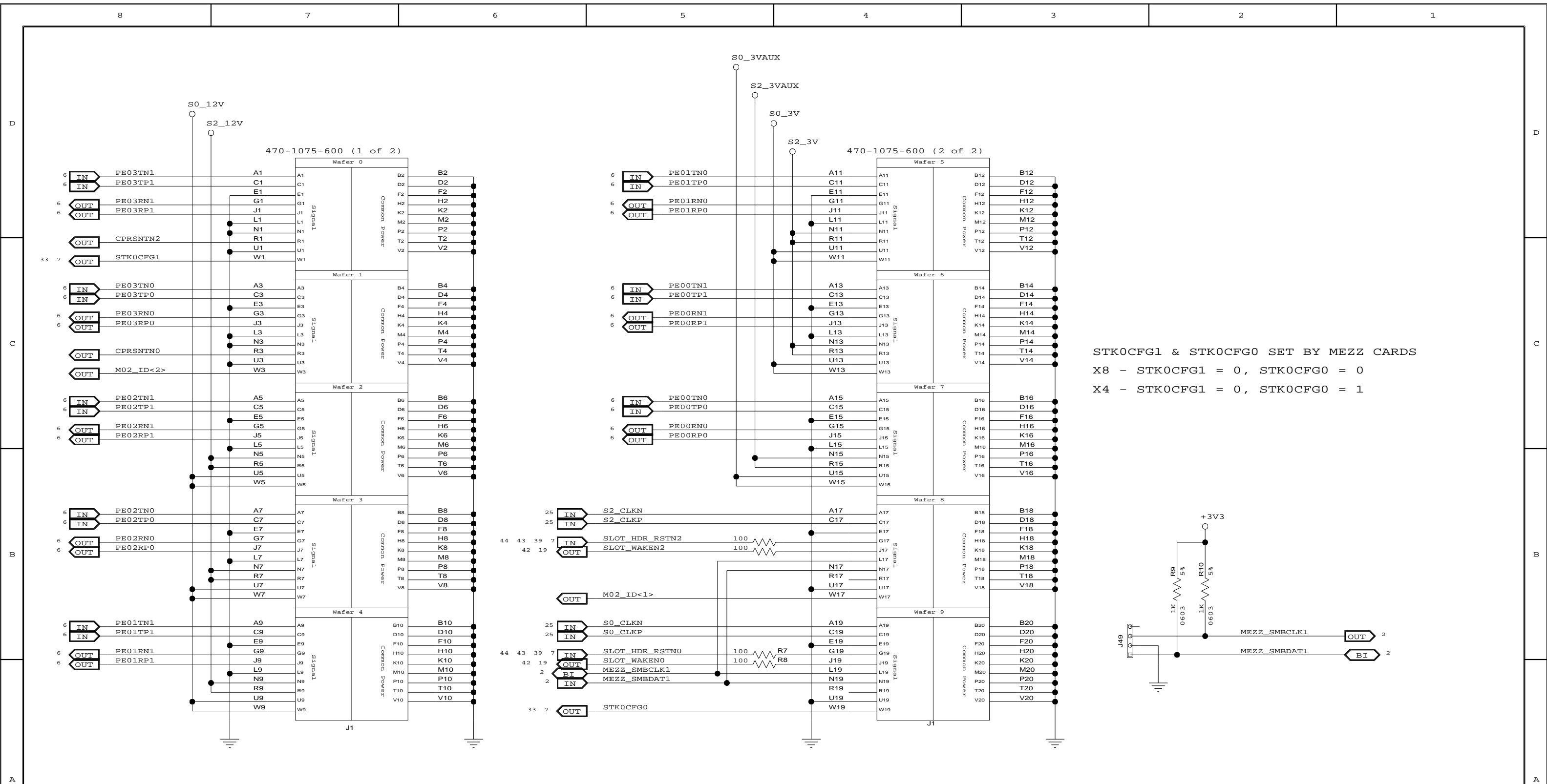
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TITLE EB-LOGAN-23			
SIZE B	DRAWING NO. SCH-PESEB-001	FAB P/N 18-691-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jul 01 15:00:52 2010			SHEET 1 OF 52



STK0CFG1 & STK0CFG0 SET BY MEZZ CARDS
 X8 - STK0CFG1 = 0, STK0CFG0 = 0
 X4 - STK0CFG1 = 0, STK0CFG0 = 1



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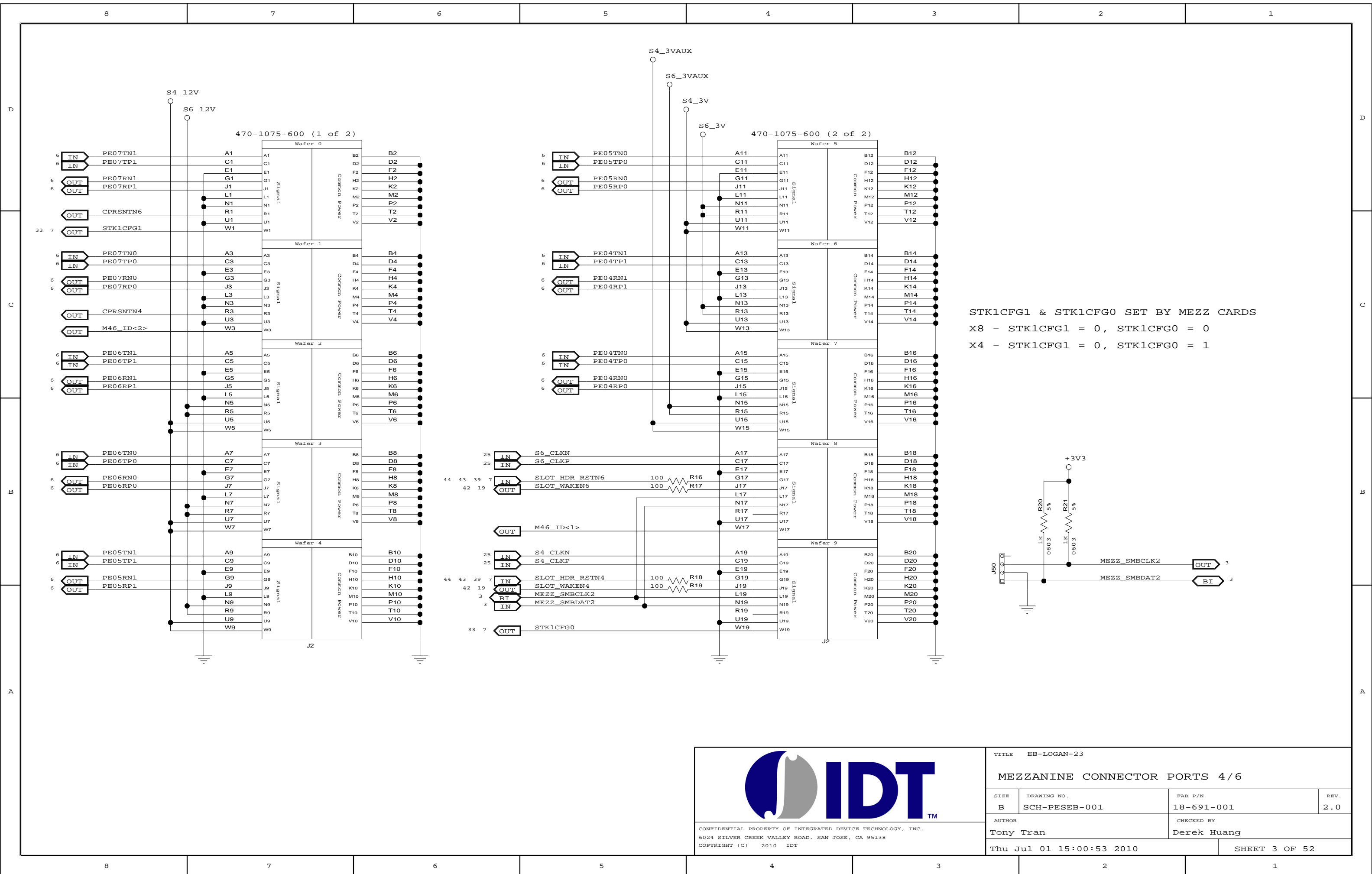
TITLE EB-LOGAN-23

MEZZANINE CONNECTOR PORTS 0/2


SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0

AUTHOR: Tony Tran
 CHECKED BY: Derek Huang

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STK1CFG1 & STK1CFG0 SET BY MEZZ CARDS
 X8 - STK1CFG1 = 0, STK1CFG0 = 0
 X4 - STK1CFG1 = 0, STK1CFG0 = 1



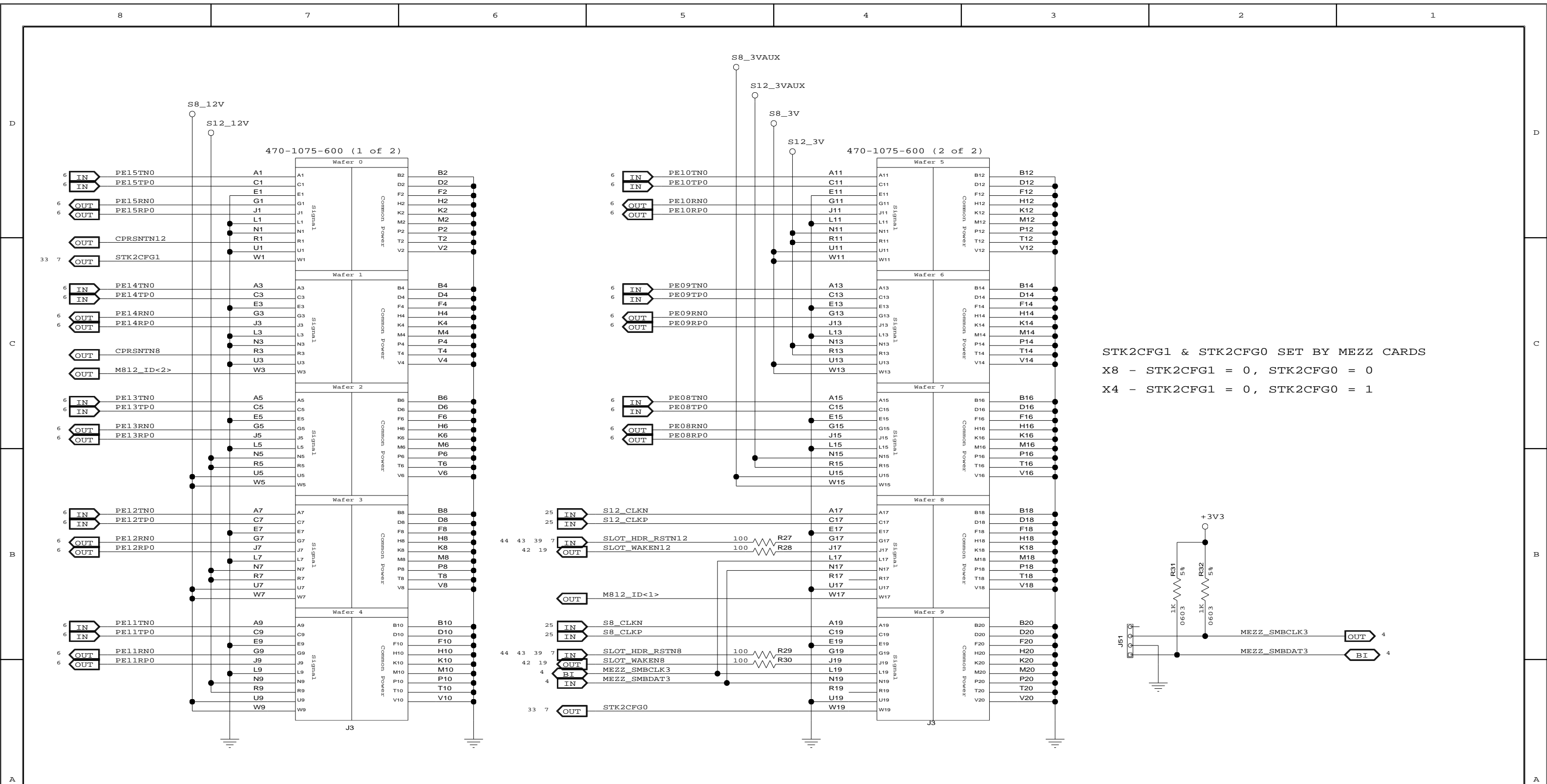
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MEZZANINE CONNECTOR PORTS 4/6

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Tony Tran		Derek Huang	

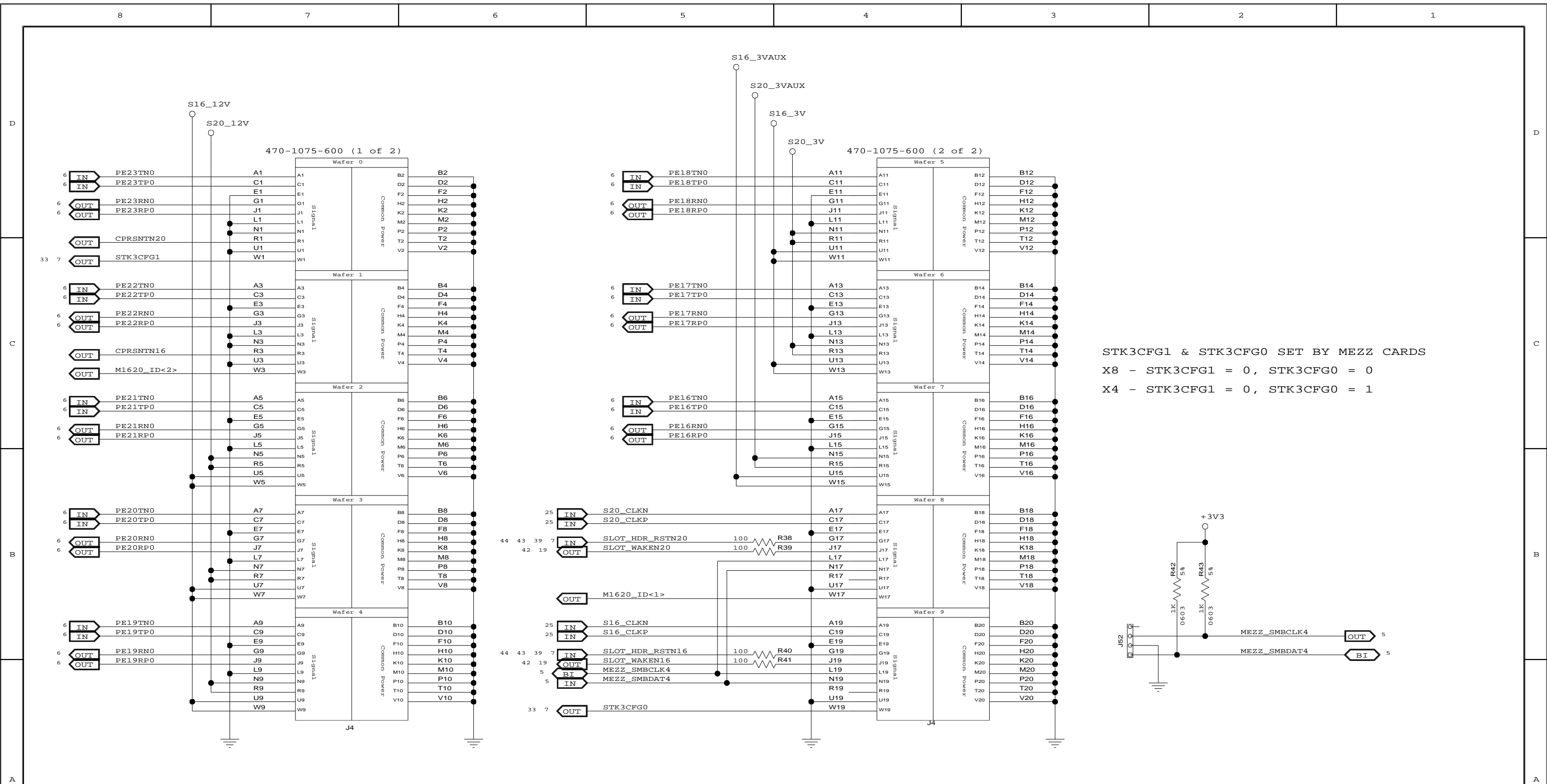
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 X4 - STK2CFG1 = 0, STK2CFG0 = 1

				TITLE EB-LOGAN-23			
MEZZANINE CONNECTOR PORTS 8/12							
SIZE	DRAWING NO.	FAB P/N	REV.				
B	SCH-PESEB-001	18-691-001	2.0				
AUTHOR			CHECKED BY				
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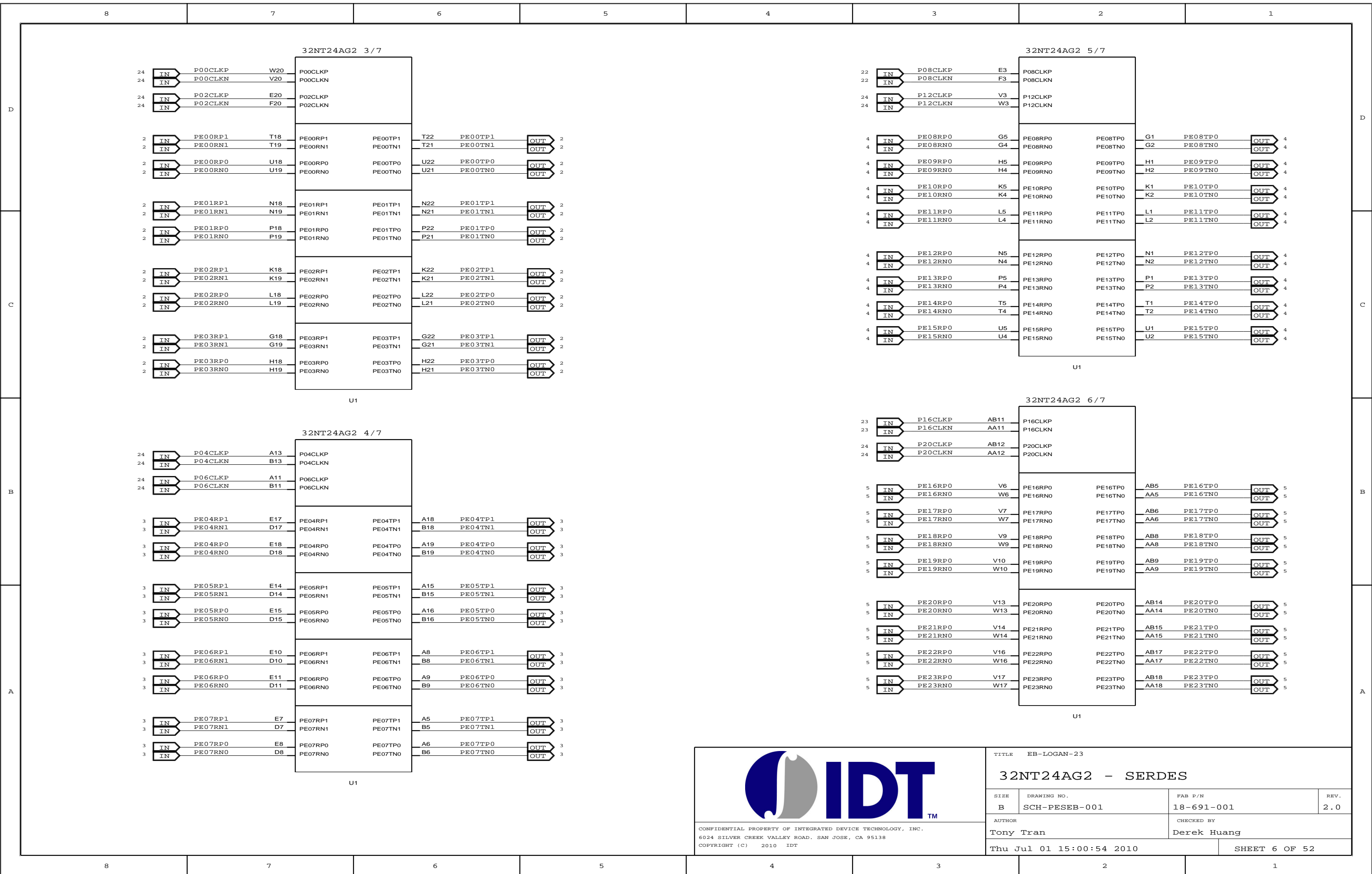
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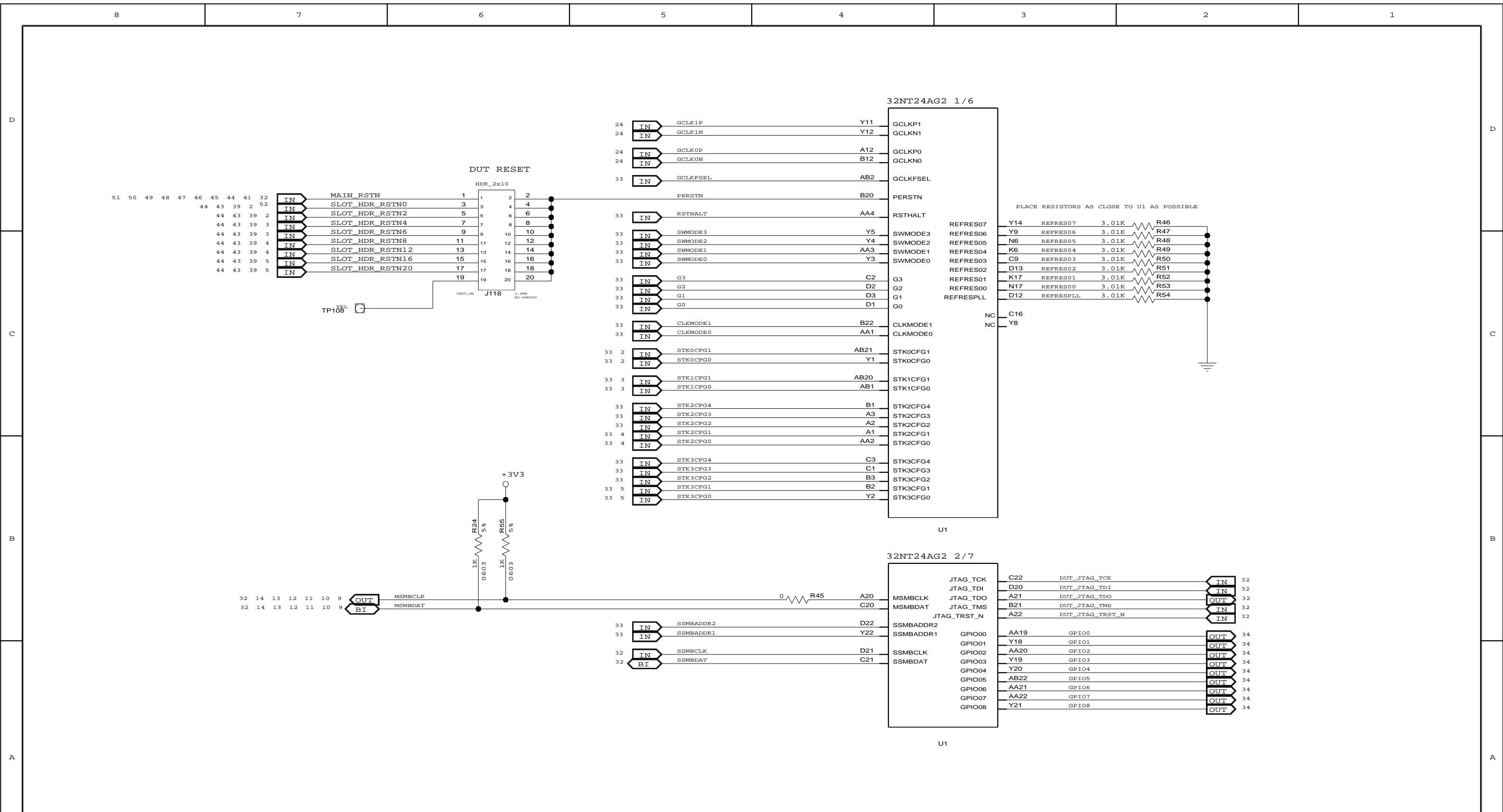
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MEZZANINE CONNECTOR PORTS 16/20							
SIZE	DRAWING NO.	FAB P/N	REV.				
B	SCH-PESEB-001	18-691-001	2.0				
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		TITLE EB-LOGAN-23	
		32NT24AG2 - SERDES	
SIZE B	DRAWING NO. SCH-PESEB-001	FAB P/N 18-691-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
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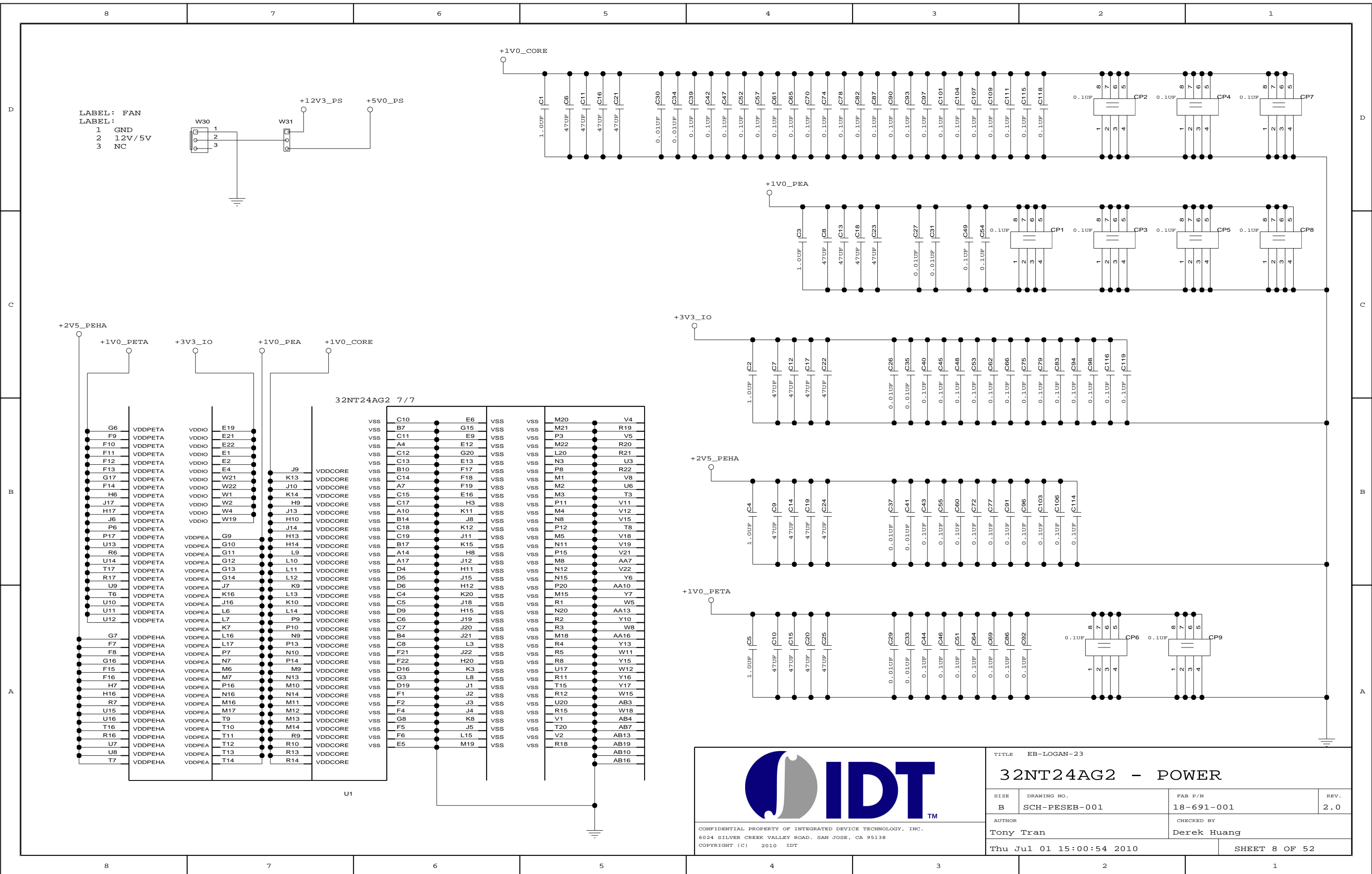


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TITLE EB-LOGAN-23

32NT24AG2 CLK, CONFIG, GPIO

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LABEL: FAN
 LABEL:
 1 GND
 2 12V/5V
 3 NC

32NT24AG2 7/7

VSS	C10	E6	VSS	VSS	M20	V4
VSS	B7	G15	VSS	VSS	M21	R19
VSS	C11	E9	VSS	VSS	P3	V5
VSS	A4	E12	VSS	VSS	M22	R20
VSS	C12	G20	VSS	VSS	L20	R21
VSS	C13	E13	VSS	VSS	N3	U3
VSS	B10	F17	VSS	VSS	P8	R22
VSS	C14	F18	VSS	VSS	M1	V8
VSS	A7	F19	VSS	VSS	M2	U6
VSS	C15	E16	VSS	VSS	M3	T3
VSS	C17	H3	VSS	VSS	P11	V11
VSS	A10	K11	VSS	VSS	M4	V12
VSS	B14	J8	VSS	VSS	N8	V15
VSS	C18	K12	VSS	VSS	P12	T8
VSS	C19	J11	VSS	VSS	M5	V18
VSS	B17	K15	VSS	VSS	N11	V19
VSS	A14	H8	VSS	VSS	P15	V21
VSS	A17	J12	VSS	VSS	M8	AA7
VSS	D4	H11	VSS	VSS	N12	V22
VSS	D5	J15	VSS	VSS	N15	Y6
VSS	D6	H12	VSS	VSS	P20	AA10
VSS	C4	K20	VSS	VSS	M15	Y7
VSS	C5	J18	VSS	VSS	R1	W5
VSS	D9	H15	VSS	VSS	N20	AA13
VSS	C6	J19	VSS	VSS	R2	Y10
VSS	C7	J20	VSS	VSS	R3	W8
VSS	B4	J21	VSS	VSS	M18	AA16
VSS	C8	L3	VSS	VSS	R4	Y13
VSS	F21	J22	VSS	VSS	R5	W11
VSS	F22	H20	VSS	VSS	R8	Y15
VSS	D16	K3	VSS	VSS	U17	W12
VSS	G3	L8	VSS	VSS	R11	Y16
VSS	D19	J1	VSS	VSS	T15	Y17
VSS	F1	J2	VSS	VSS	R12	W15
VSS	F2	J3	VSS	VSS	U20	AB3
VSS	F4	J4	VSS	VSS	R15	W18
VSS	G8	K8	VSS	VSS	V1	AB4
VSS	F5	J5	VSS	VSS	T20	AB7
VSS	F6	L15	VSS	VSS	V2	AB13
VSS	E5	M19	VSS	VSS	R18	AB19
						AB10
						AB16

U1



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32NT24AG2 - POWER			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
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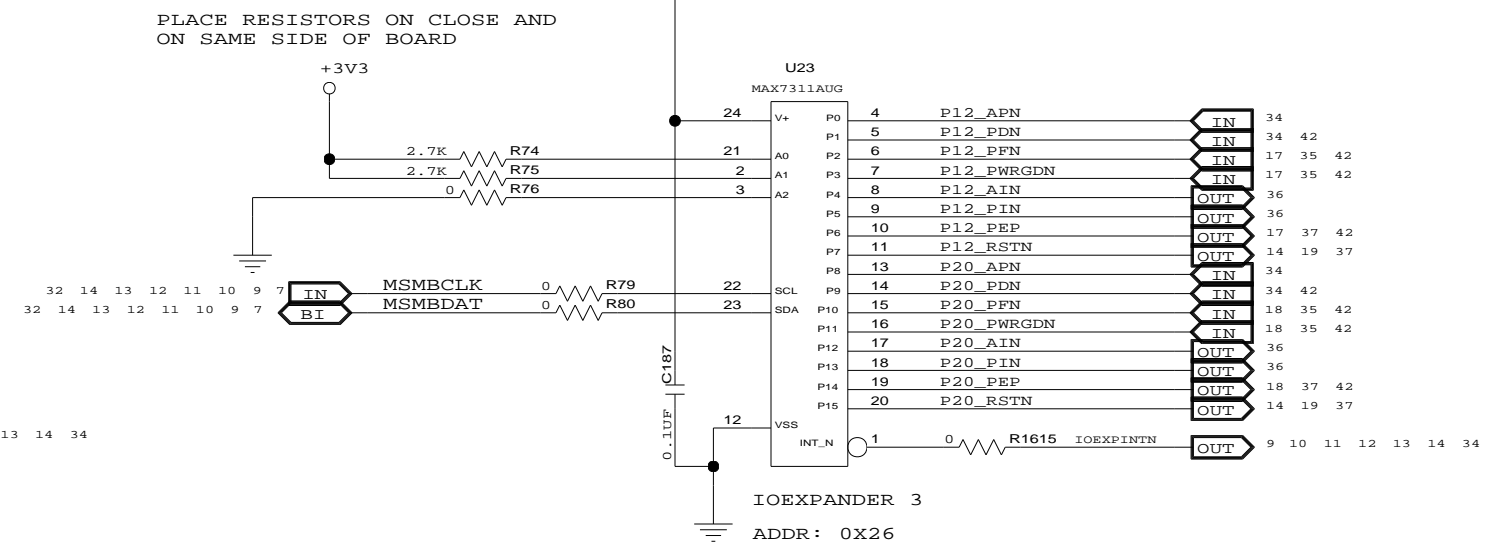
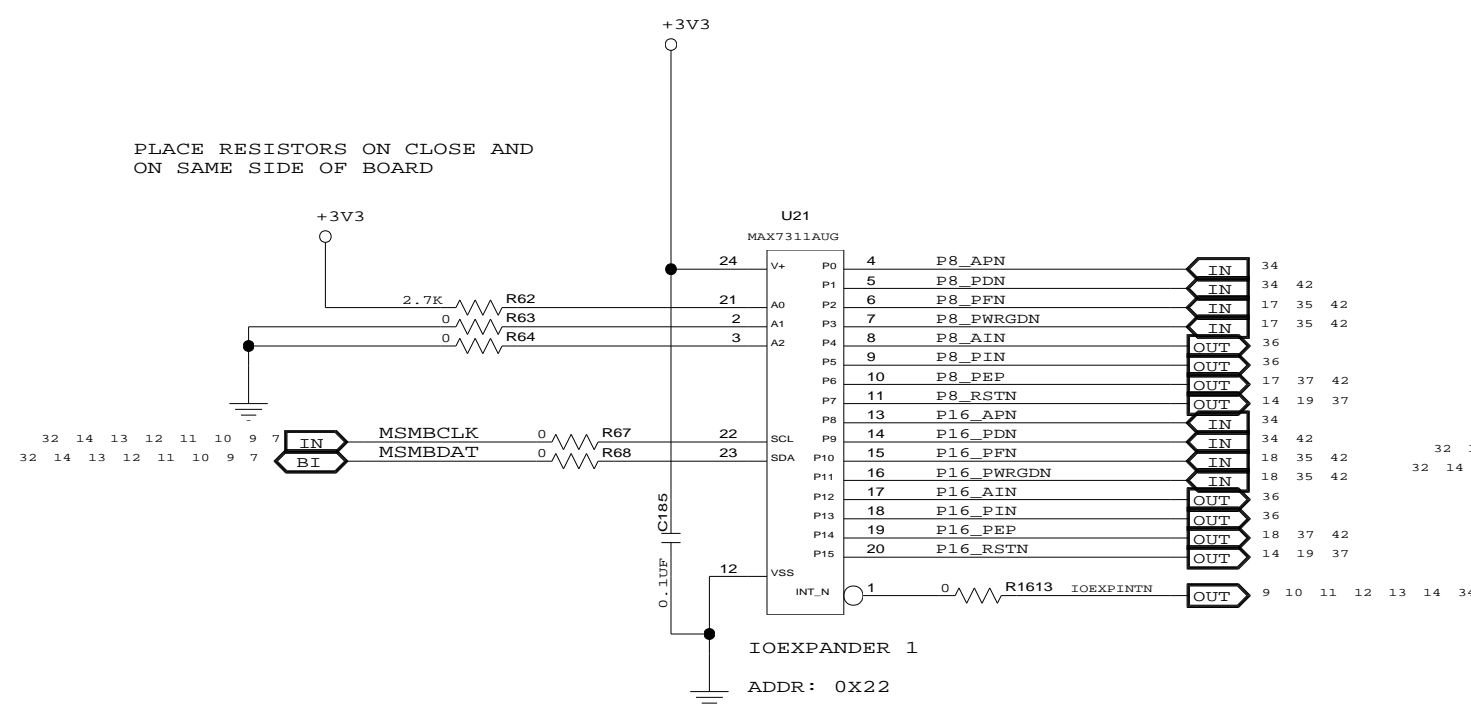
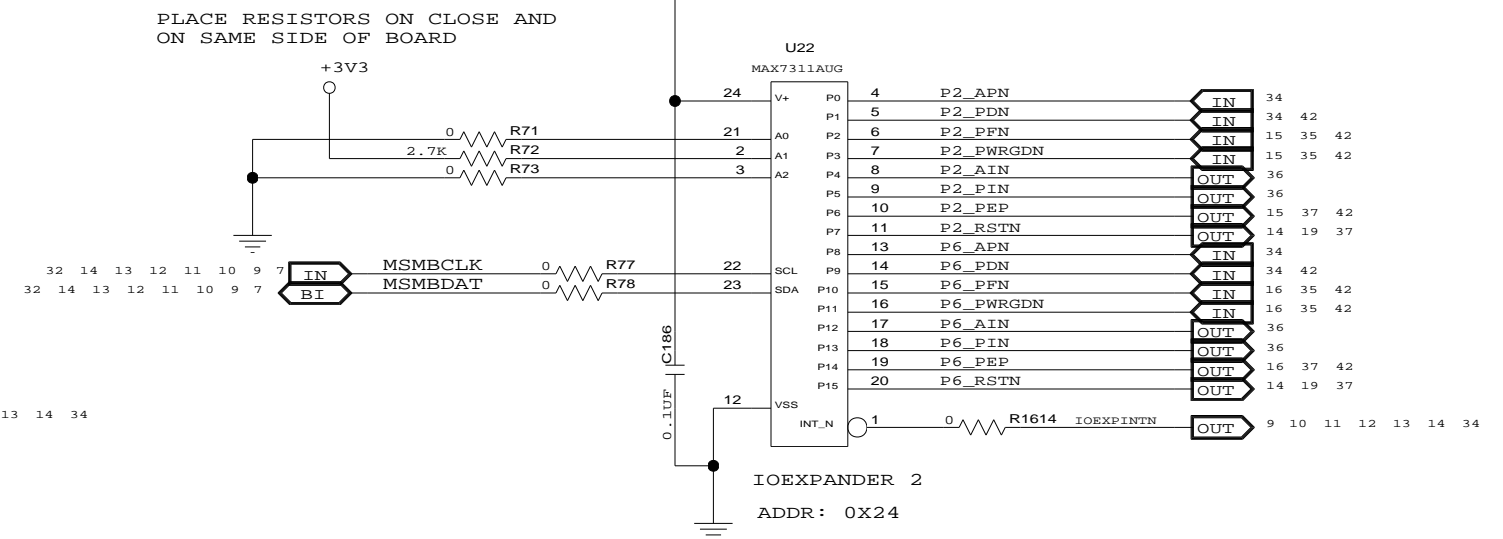
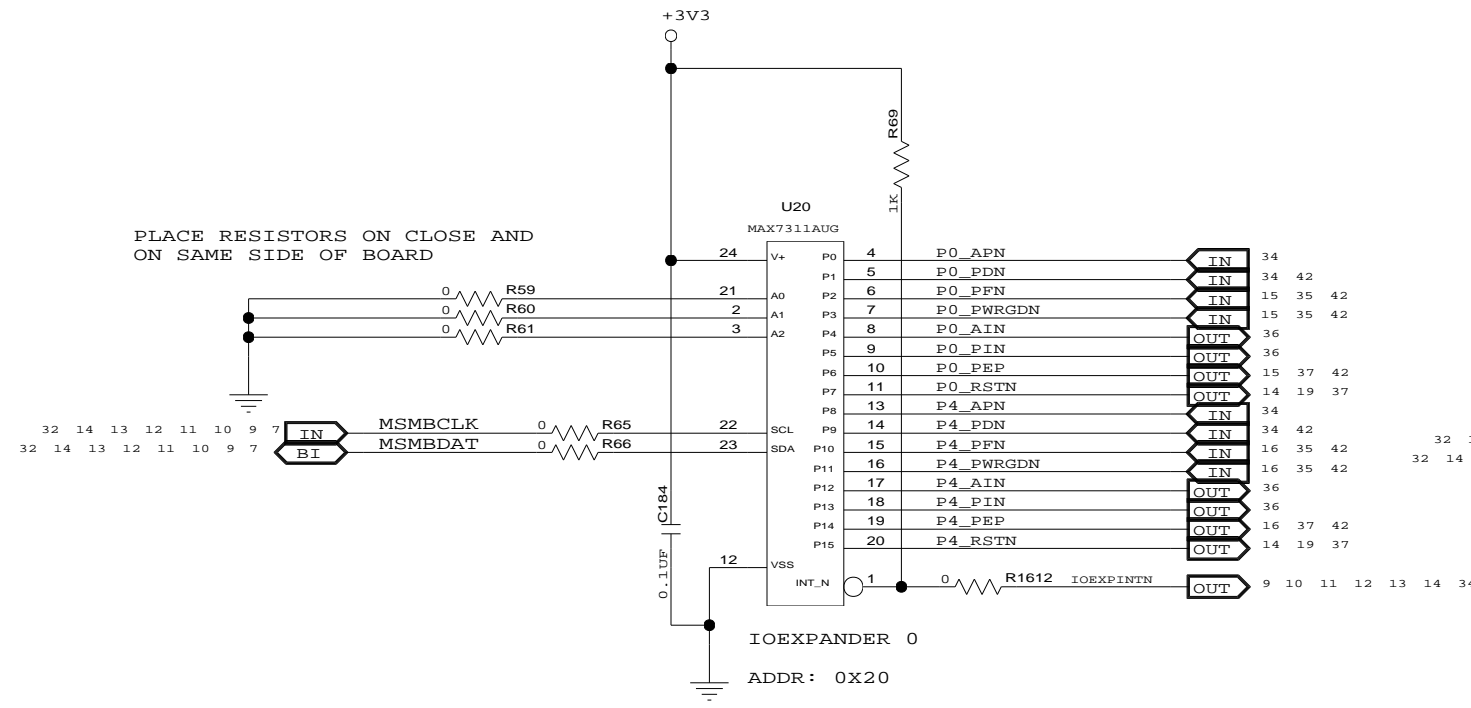
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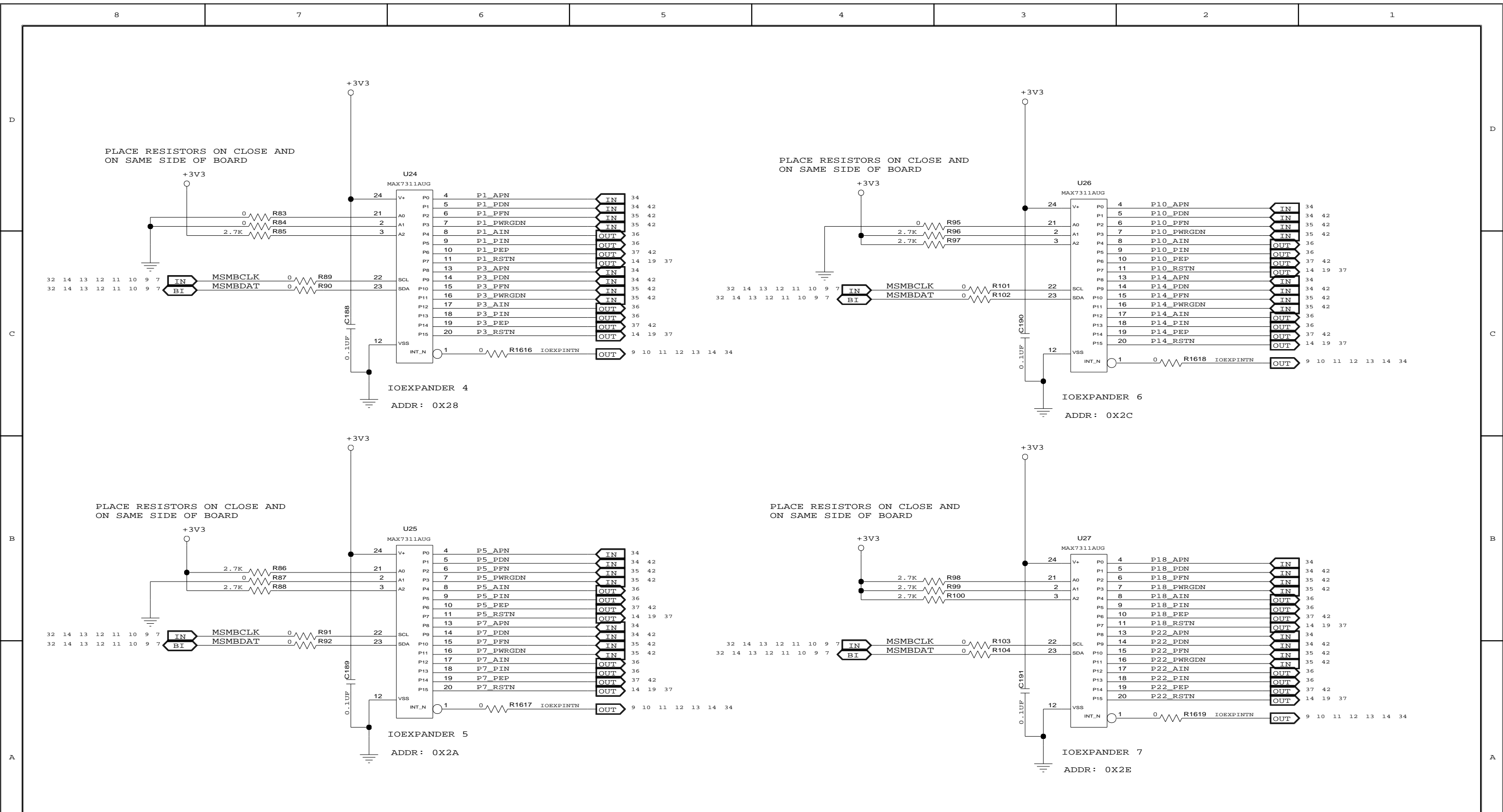


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IOEXPANDER 0-3

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TITLE EB-LOGAN-23

IOEXPANDER 4-7

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
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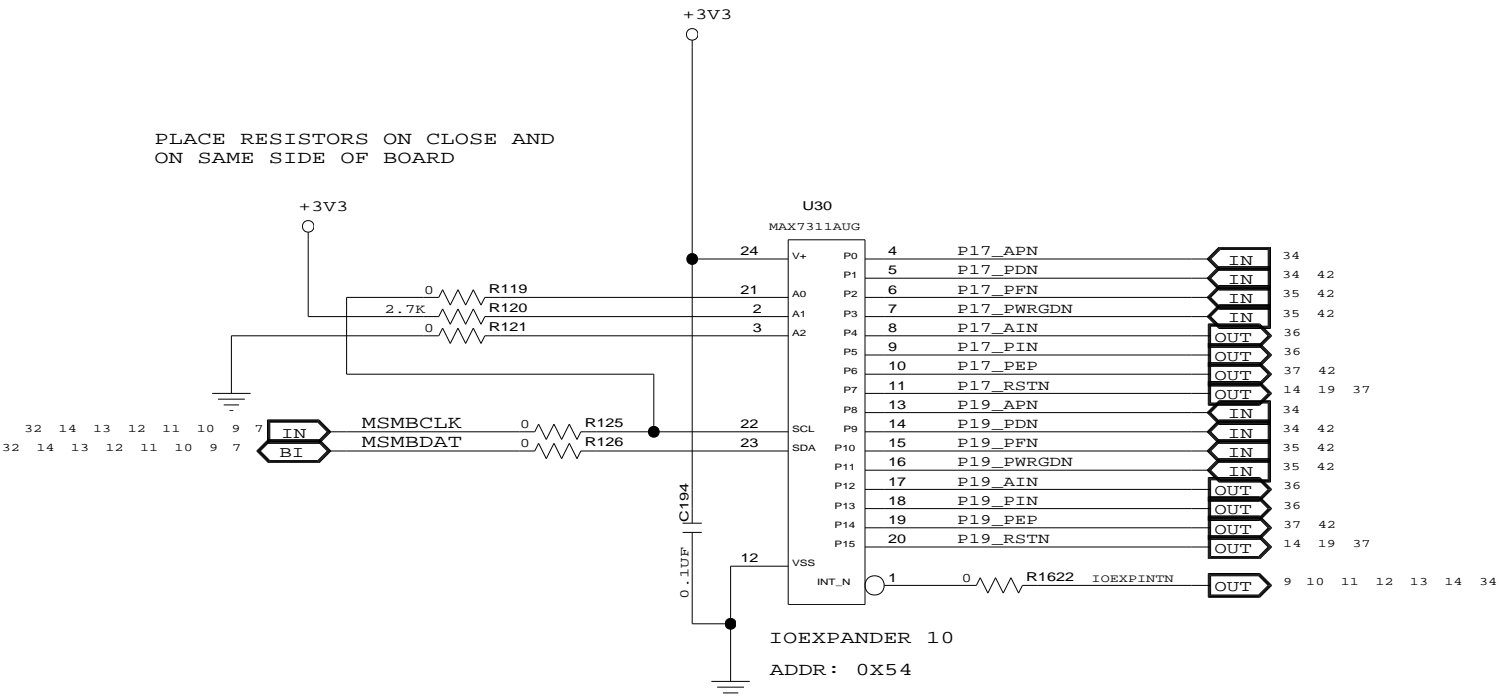
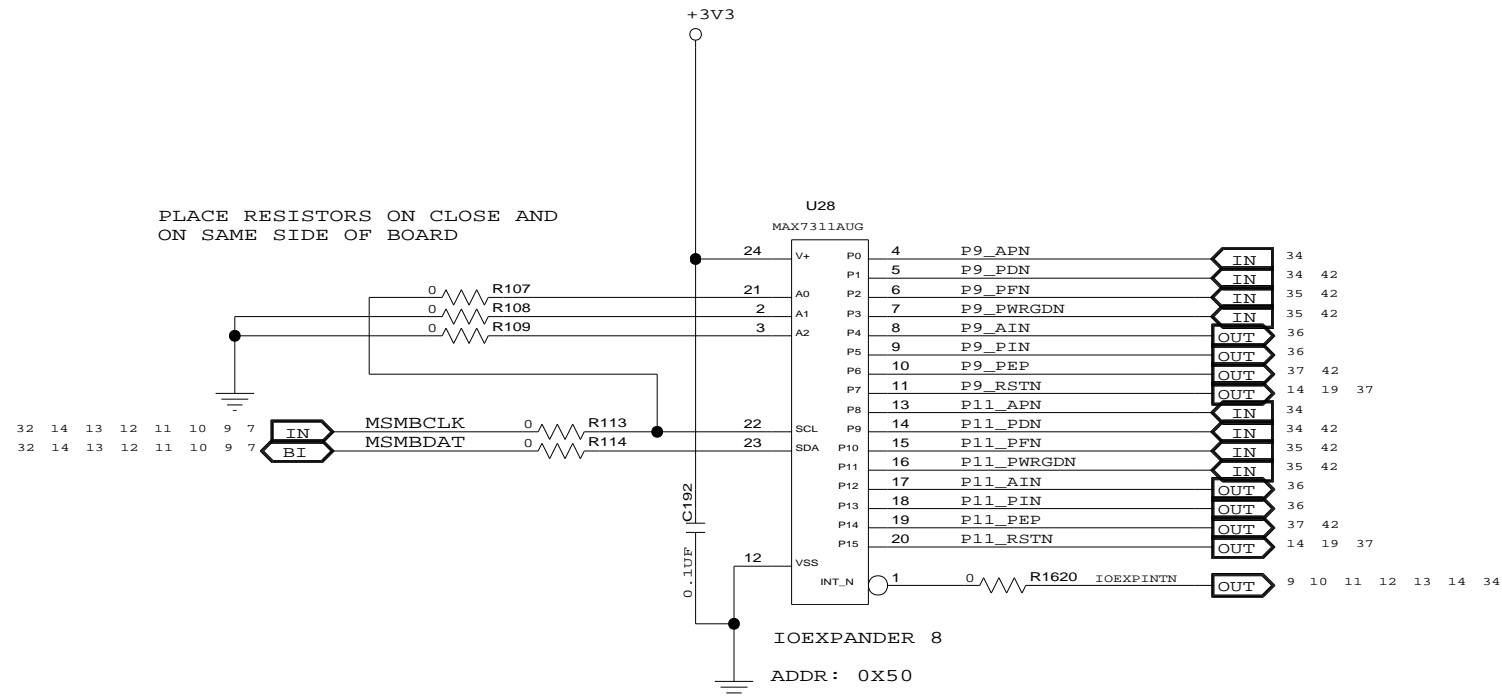
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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

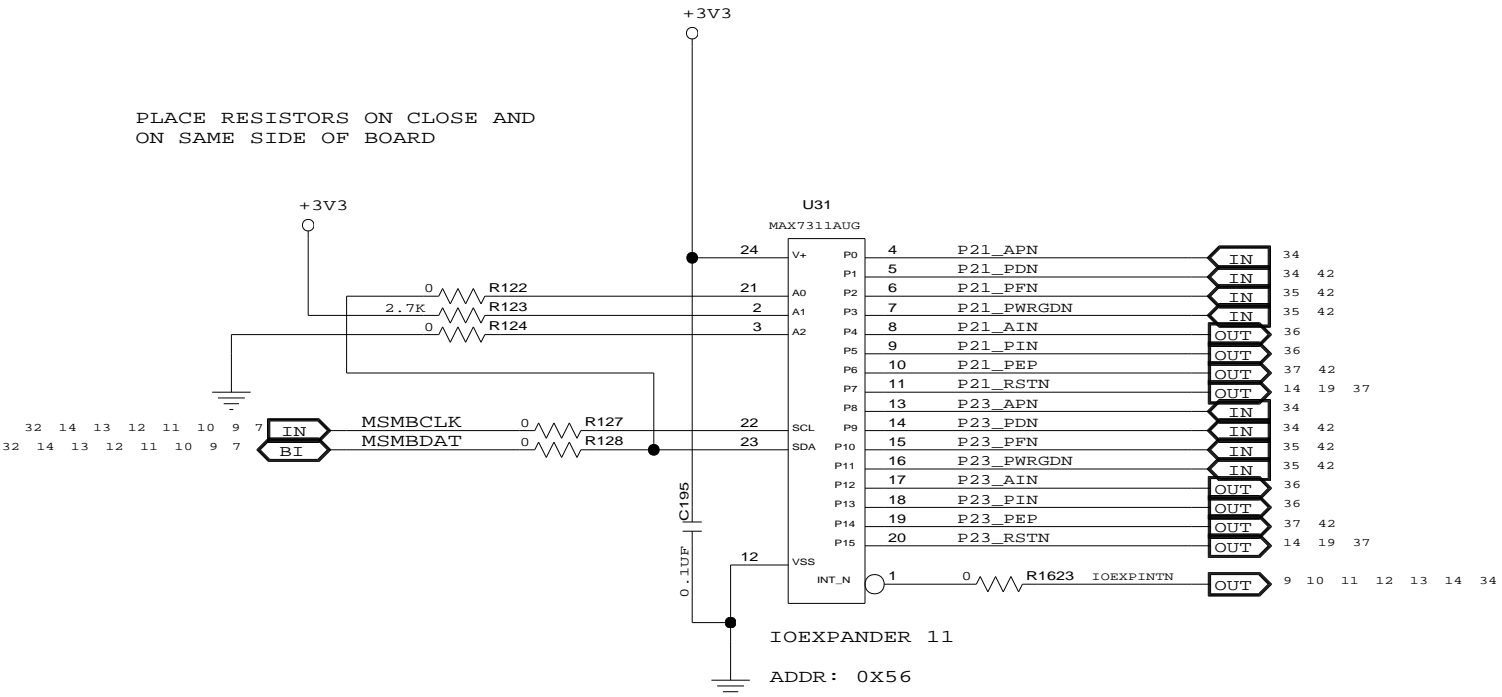
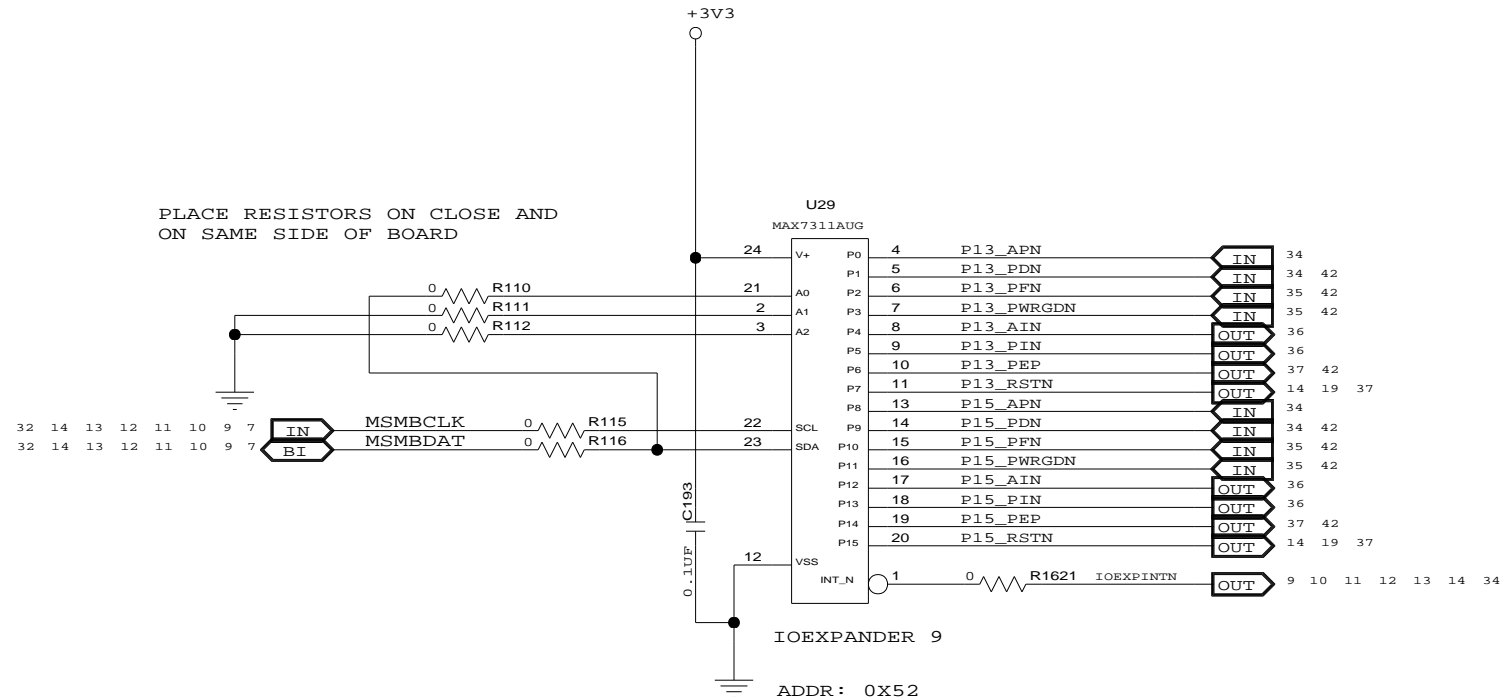


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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD




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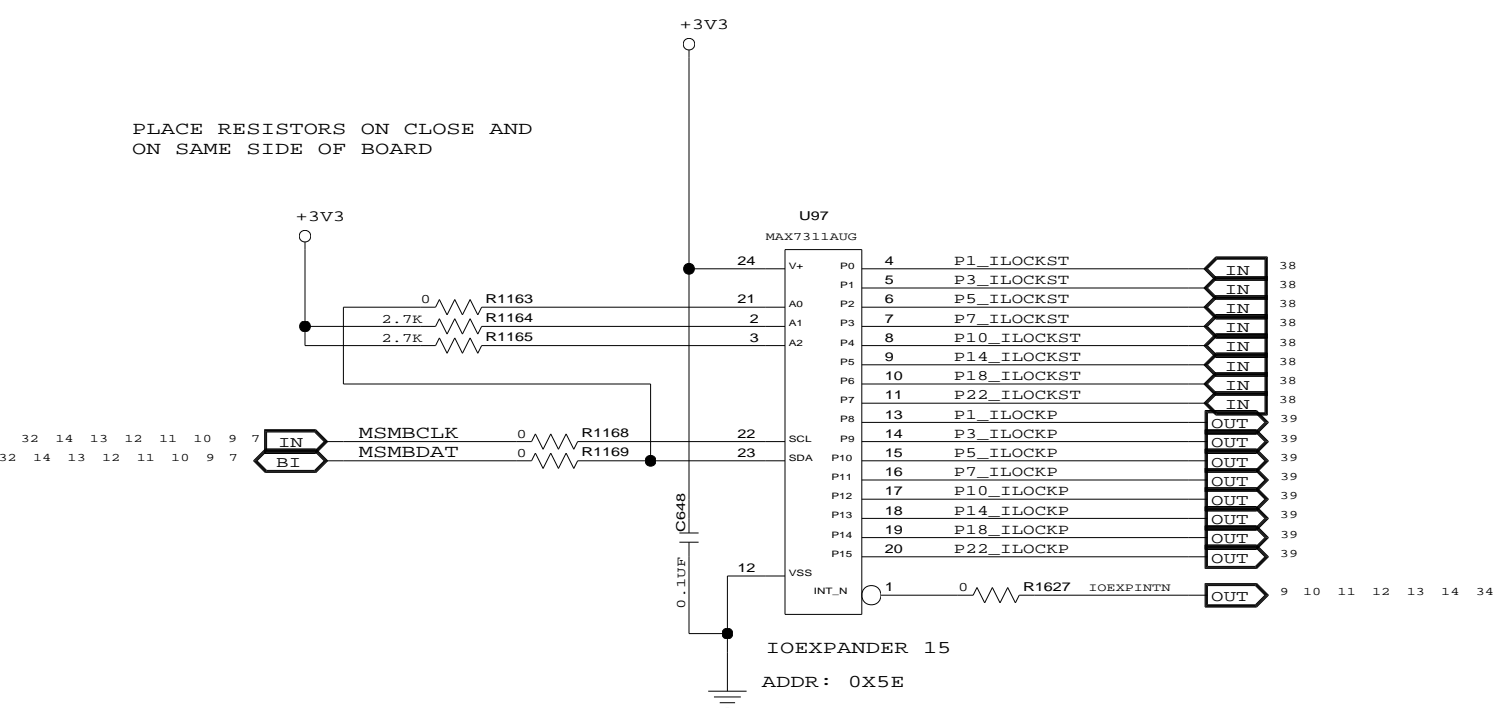
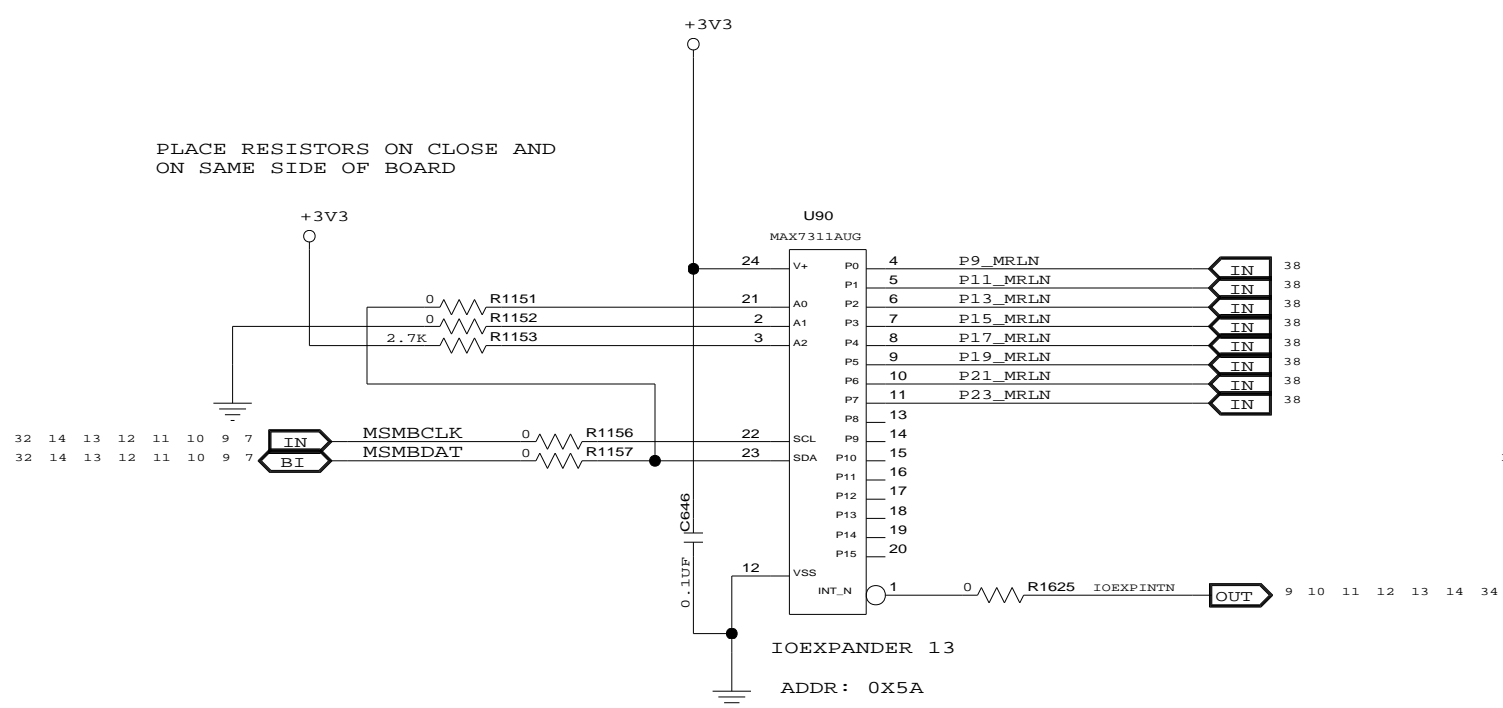
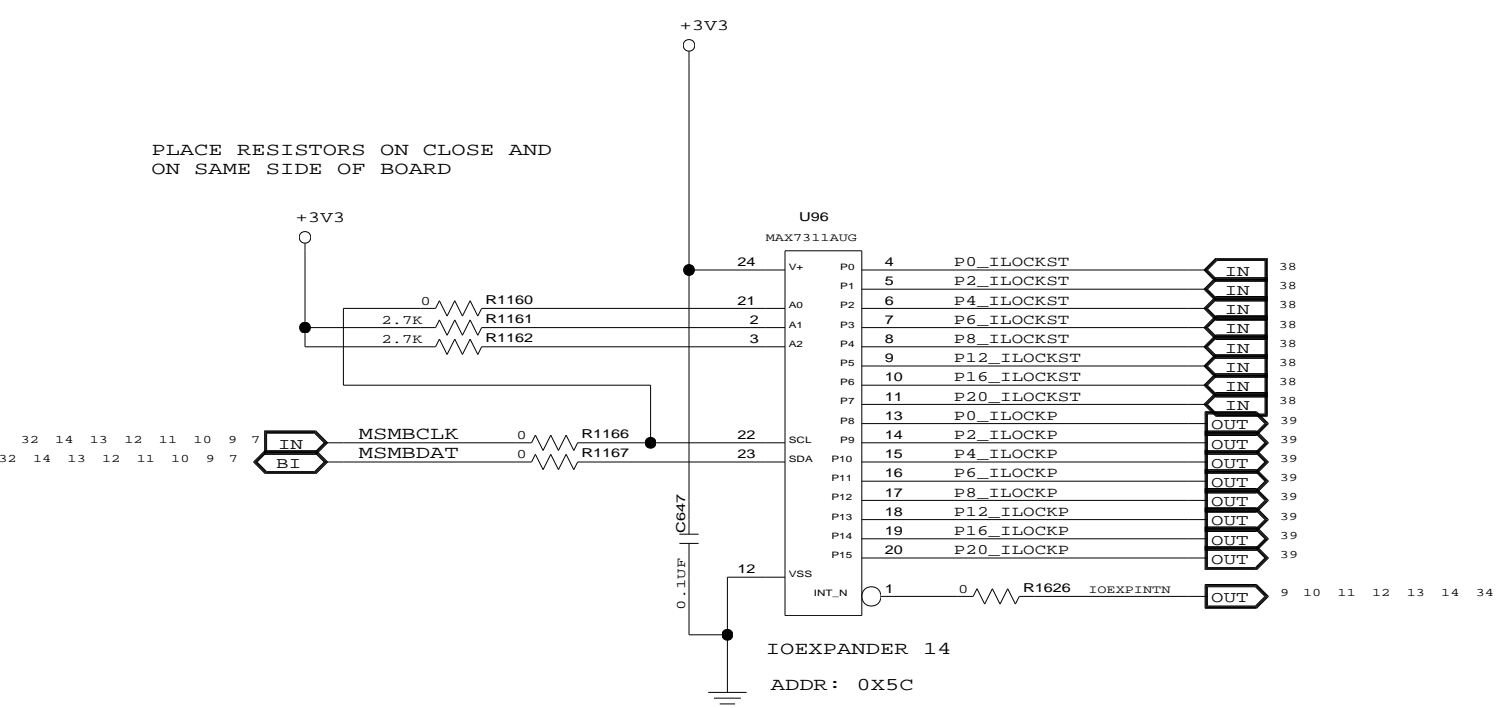
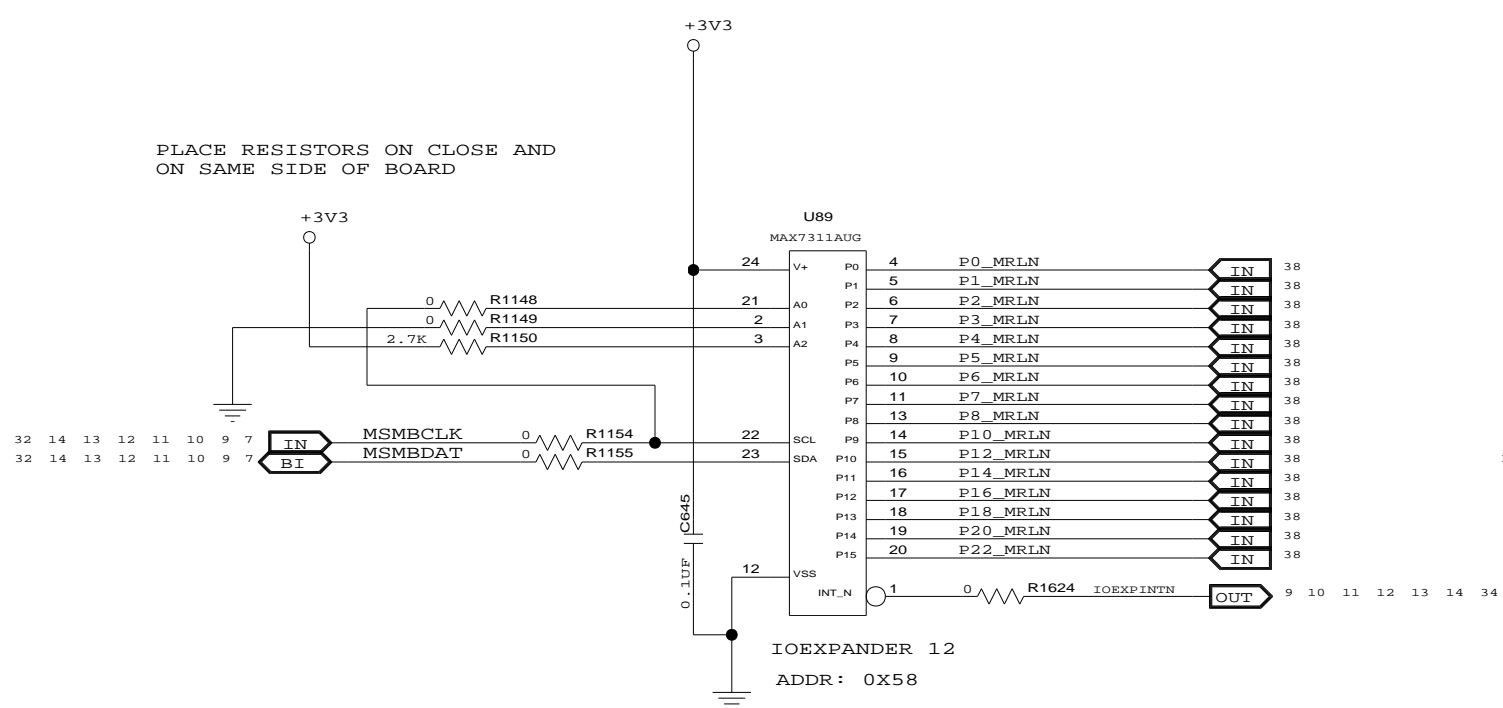
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IOEXPANDER 12-15

SIZE	DRAWING NO.	FAB P/N	REV.
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Tony Tran		Derek Huang	
Thu Jul 01 15:00:55 2010			SHEET 12 OF 52

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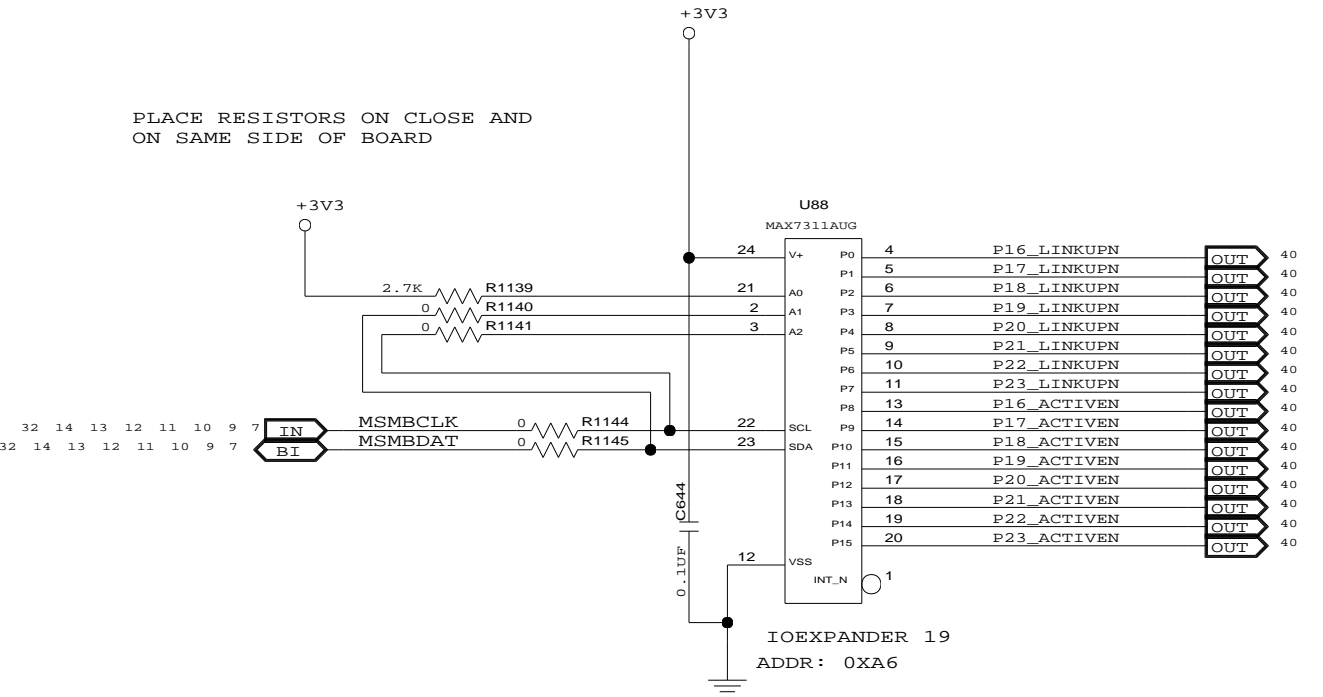
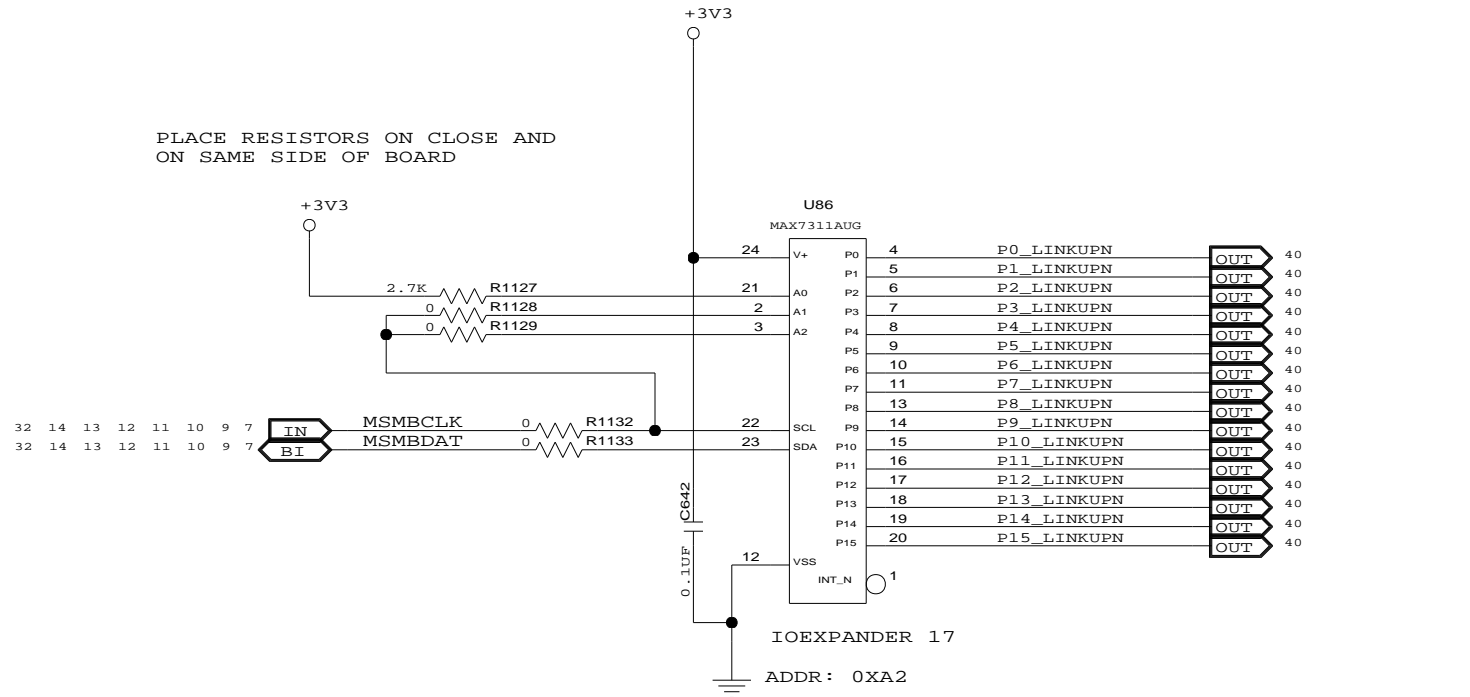
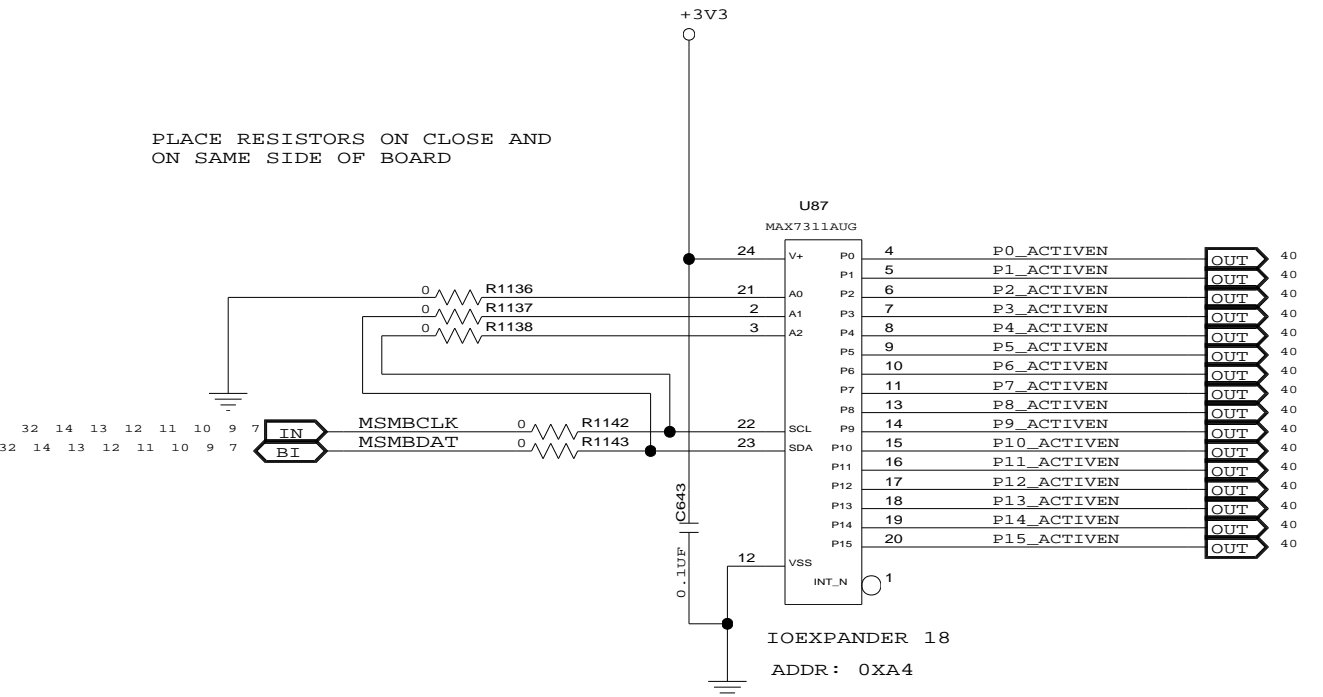
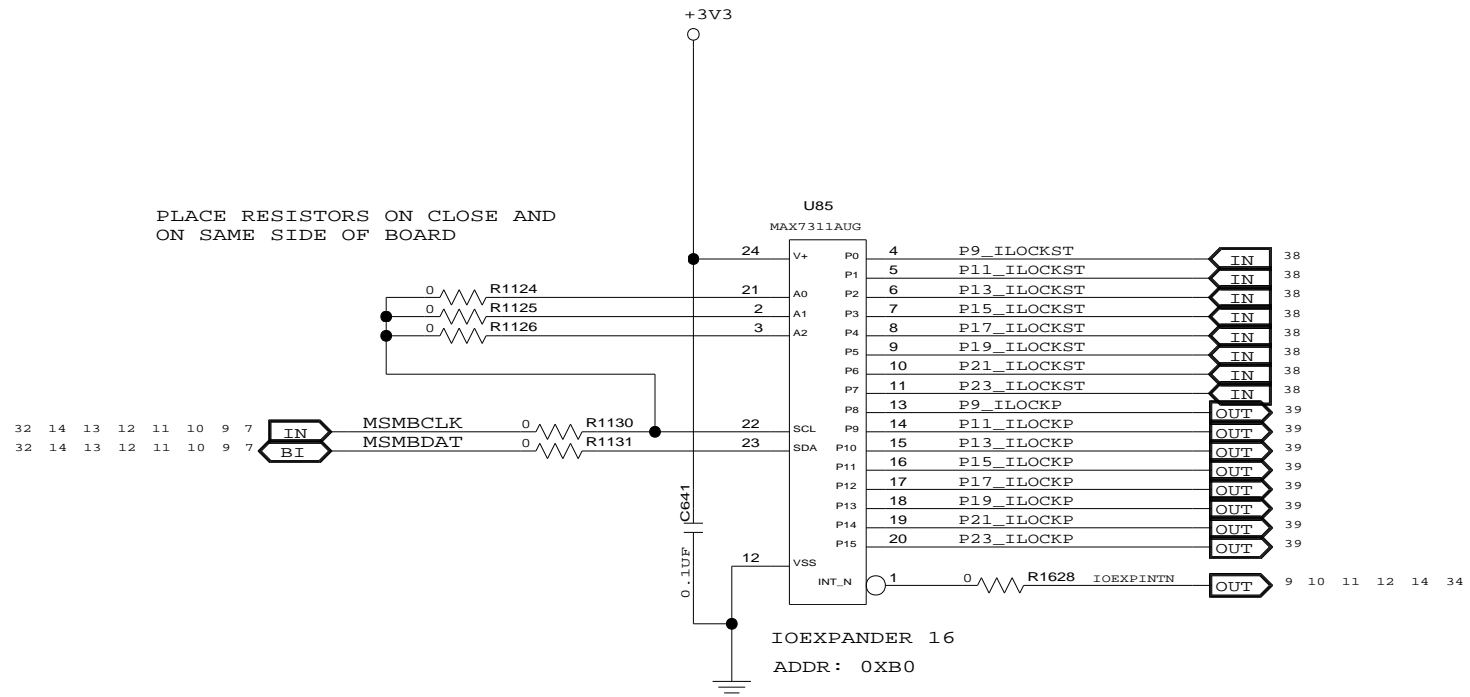
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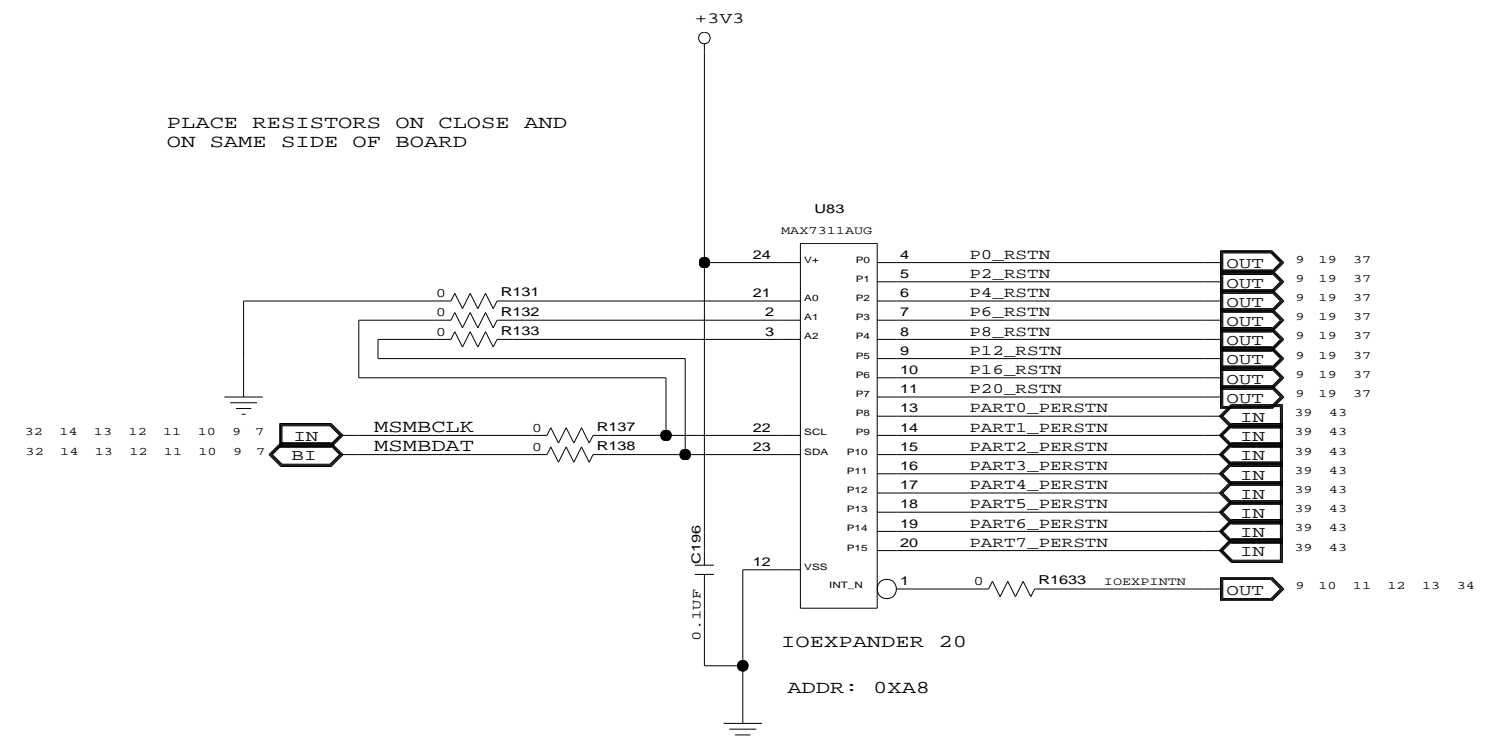
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IOEXPANDER 16-19

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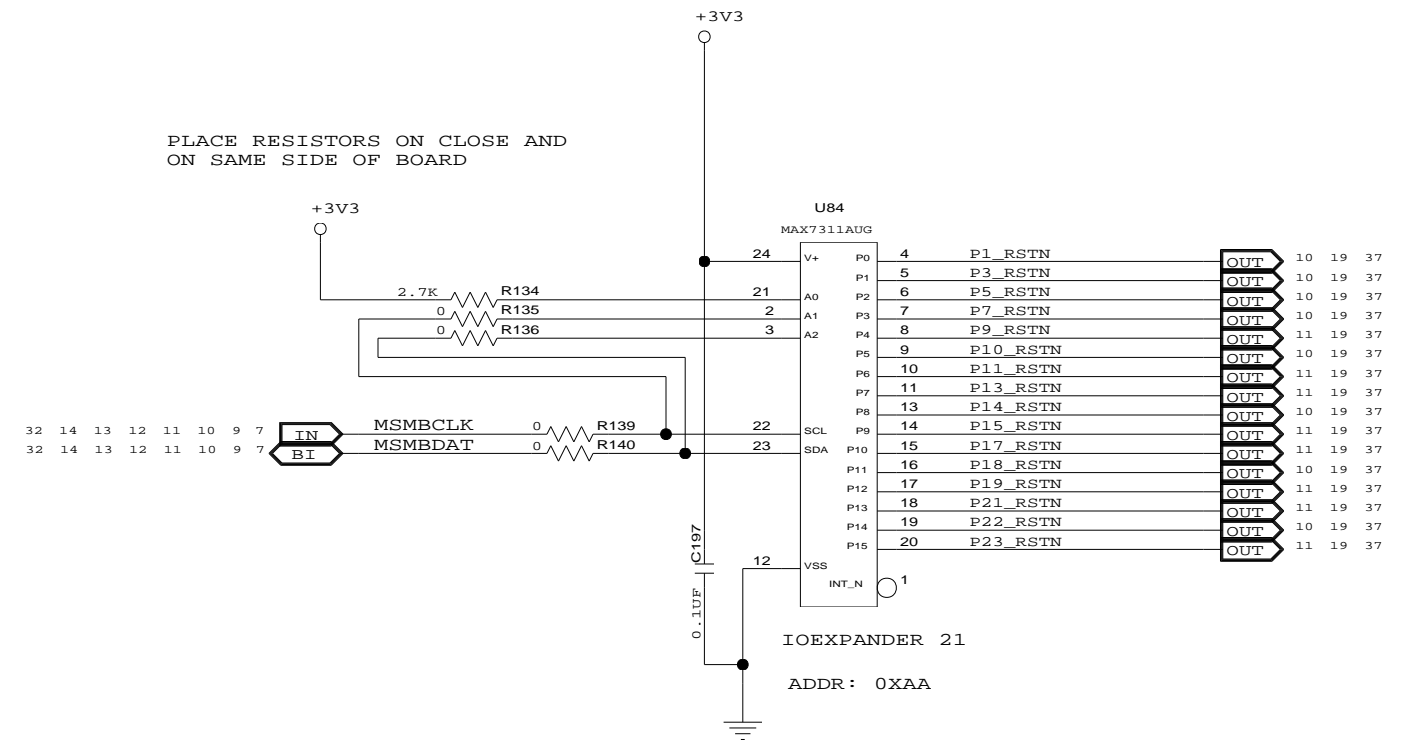
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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD




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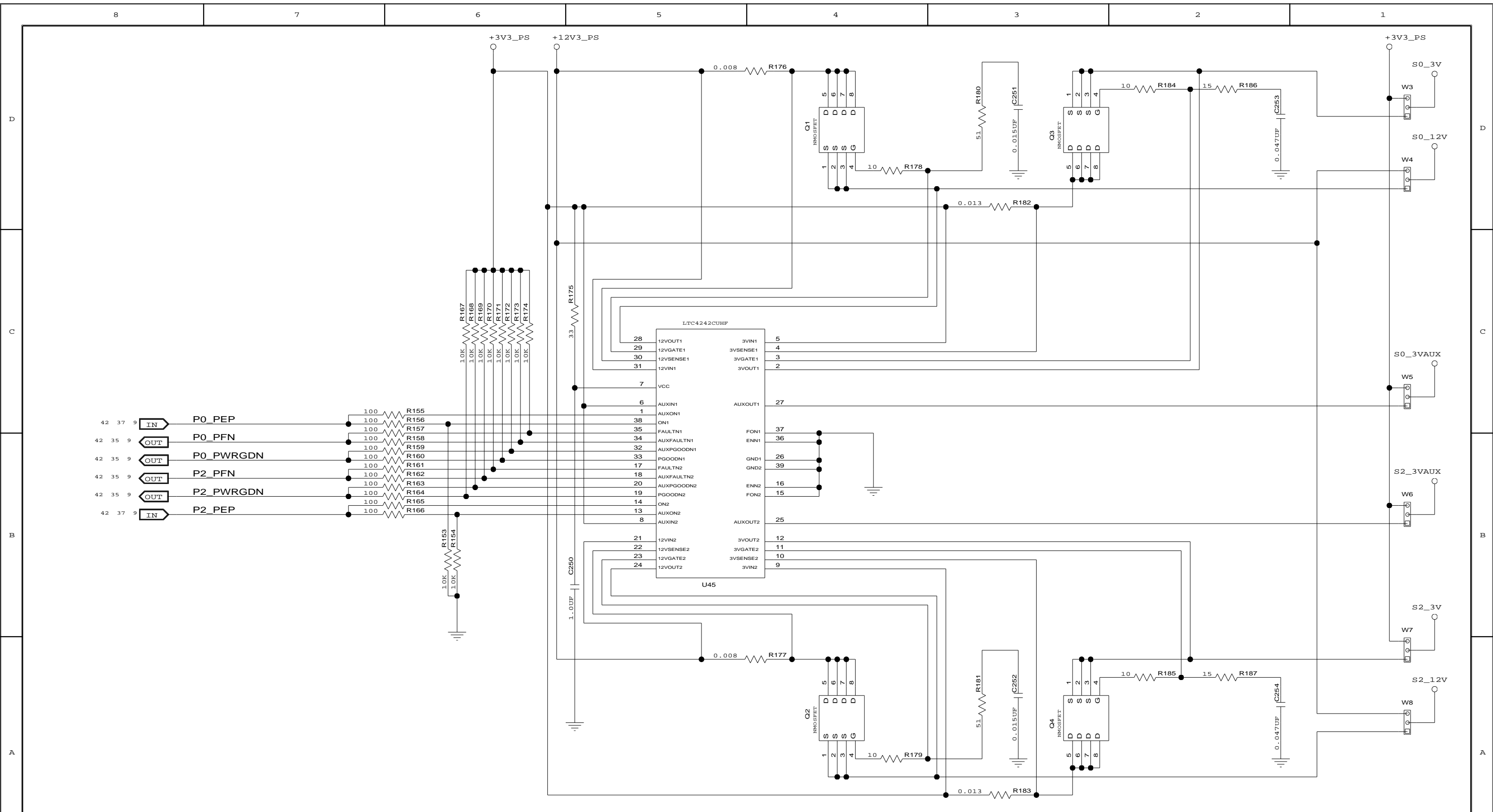



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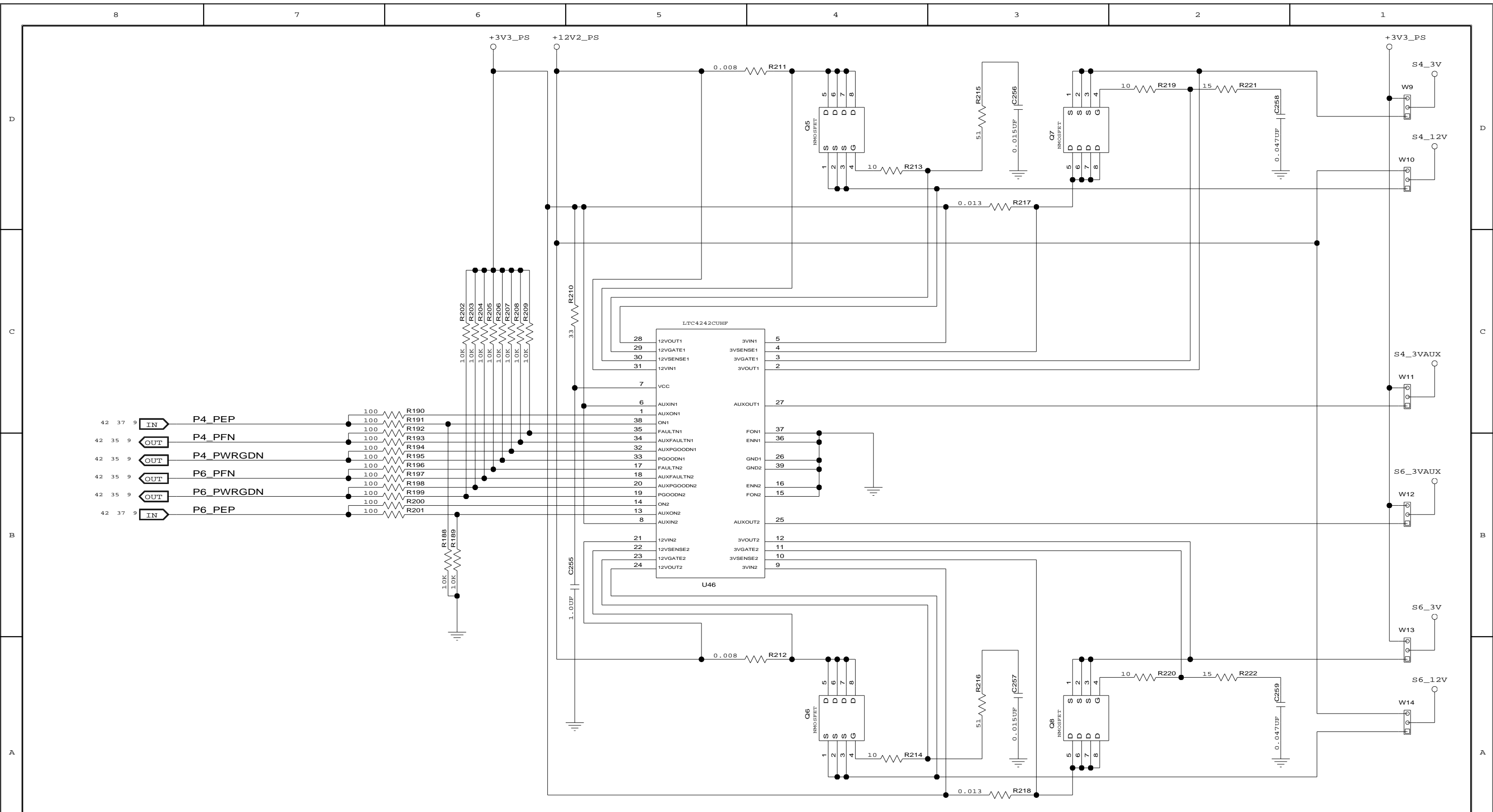



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HOT PLUG CONTROL PORTS 0-2

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AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
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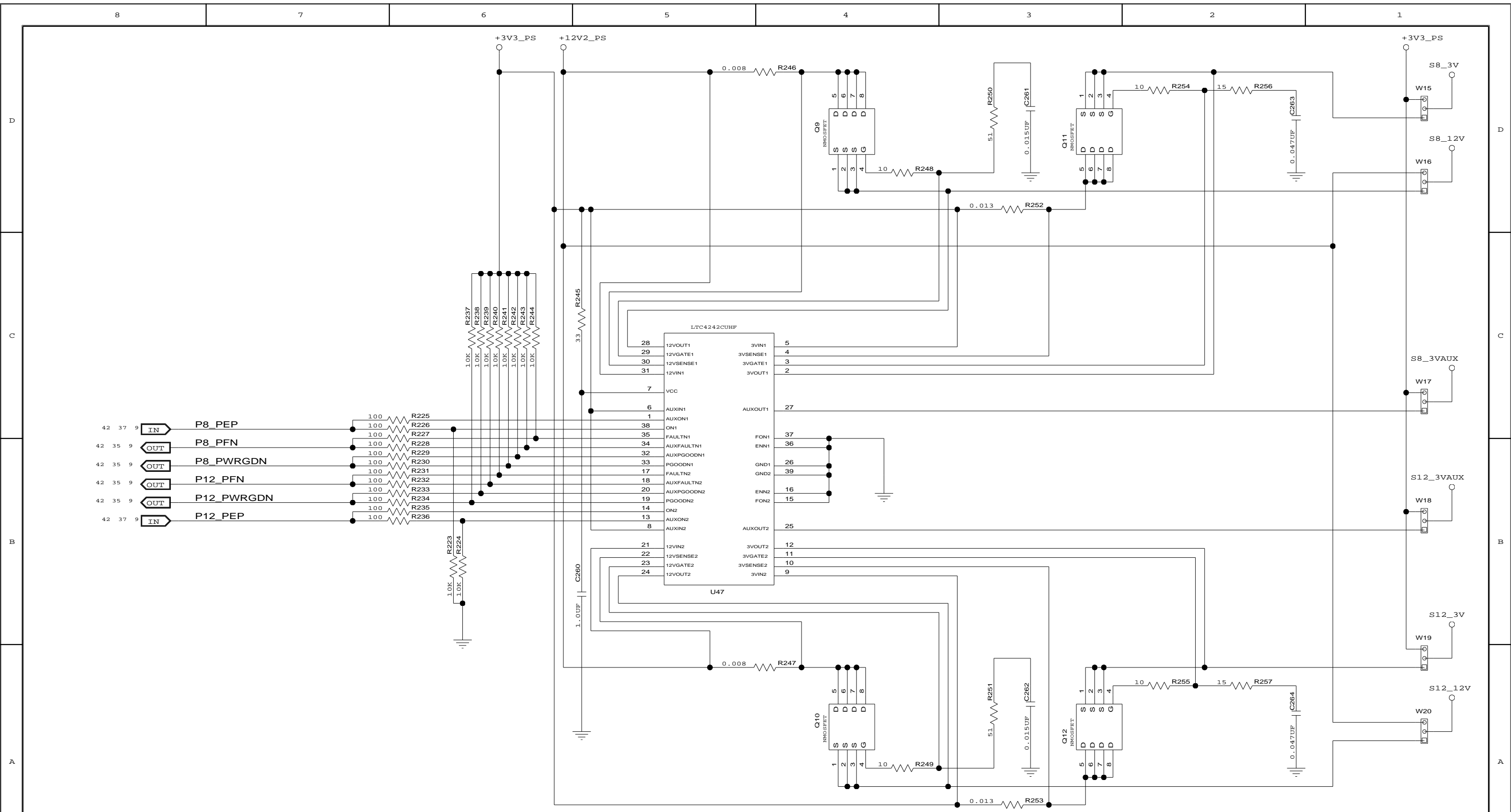



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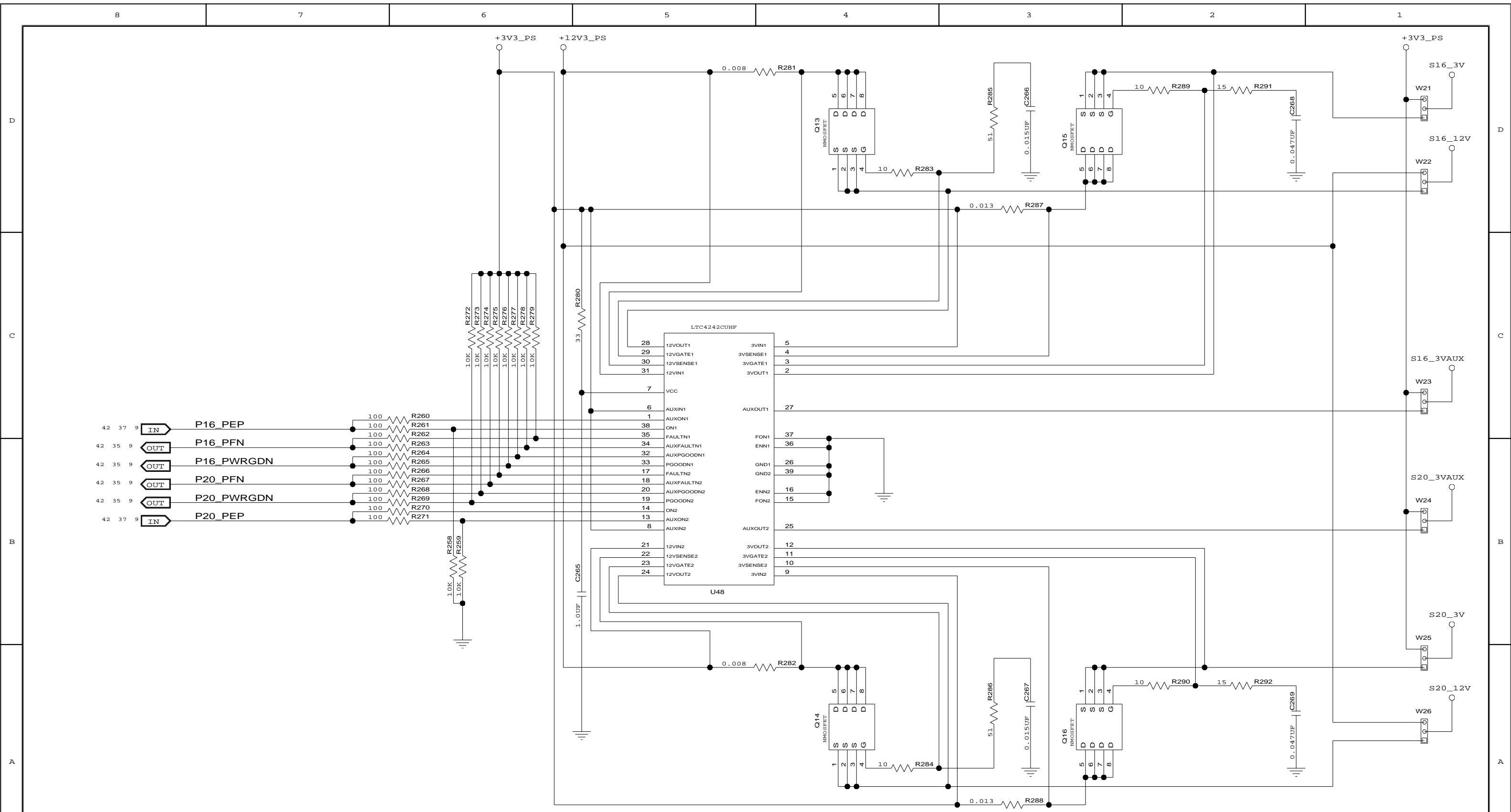
HOT PLUG CONTROL PORTS 4-6


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B	SCH-PESEB-001	18-691-001	2.0
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TITLE EB-LOGAN-23			
HOT PLUG CONTROL PORTS 8-12			
SIZE	DRAWING NO.	FAB P/N	REV.
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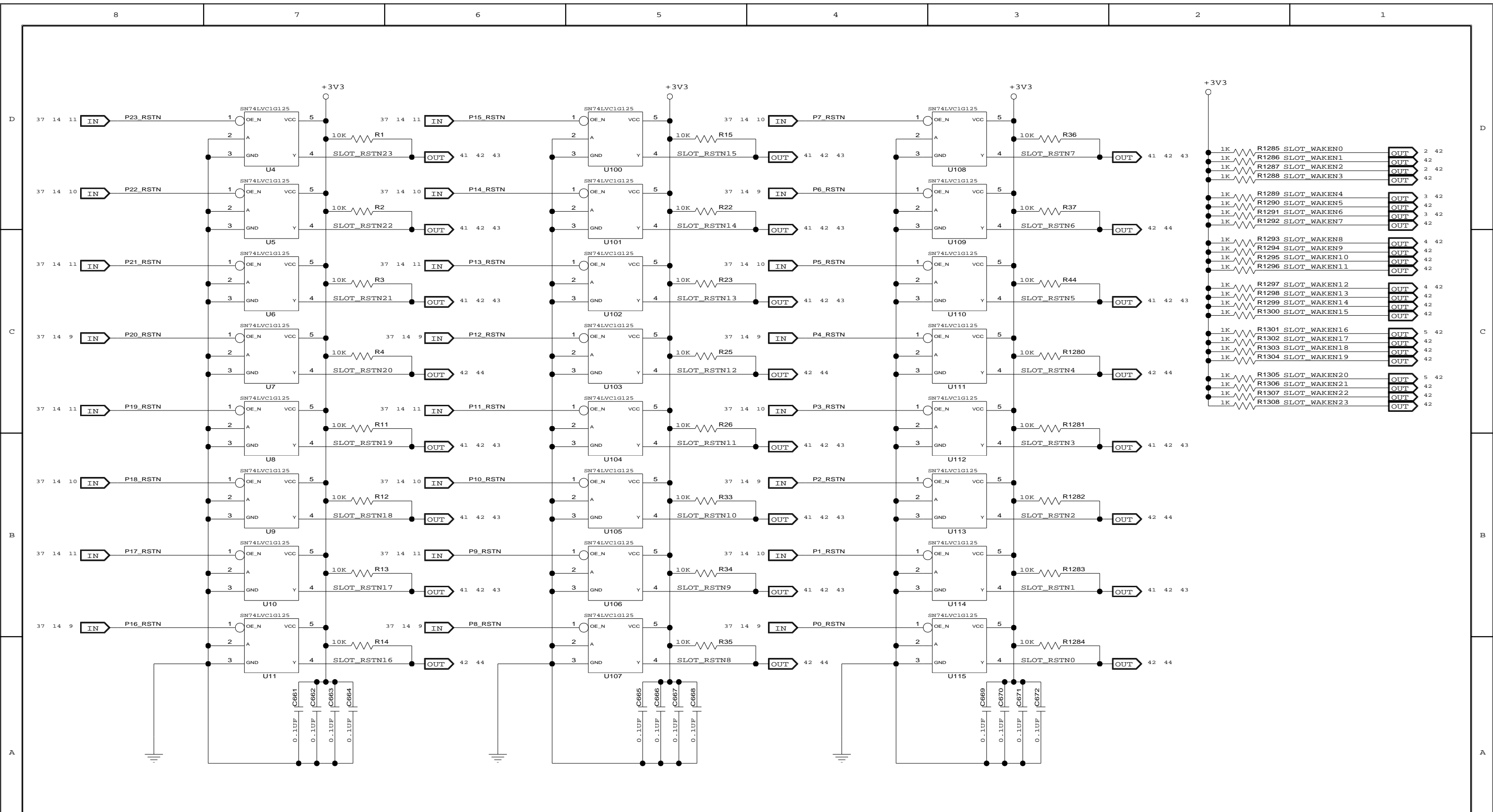



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HOT PLUG CONTROL PORTS 16-20

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AUTHOR Tony Tran		CHECKED BY Derek Huang	
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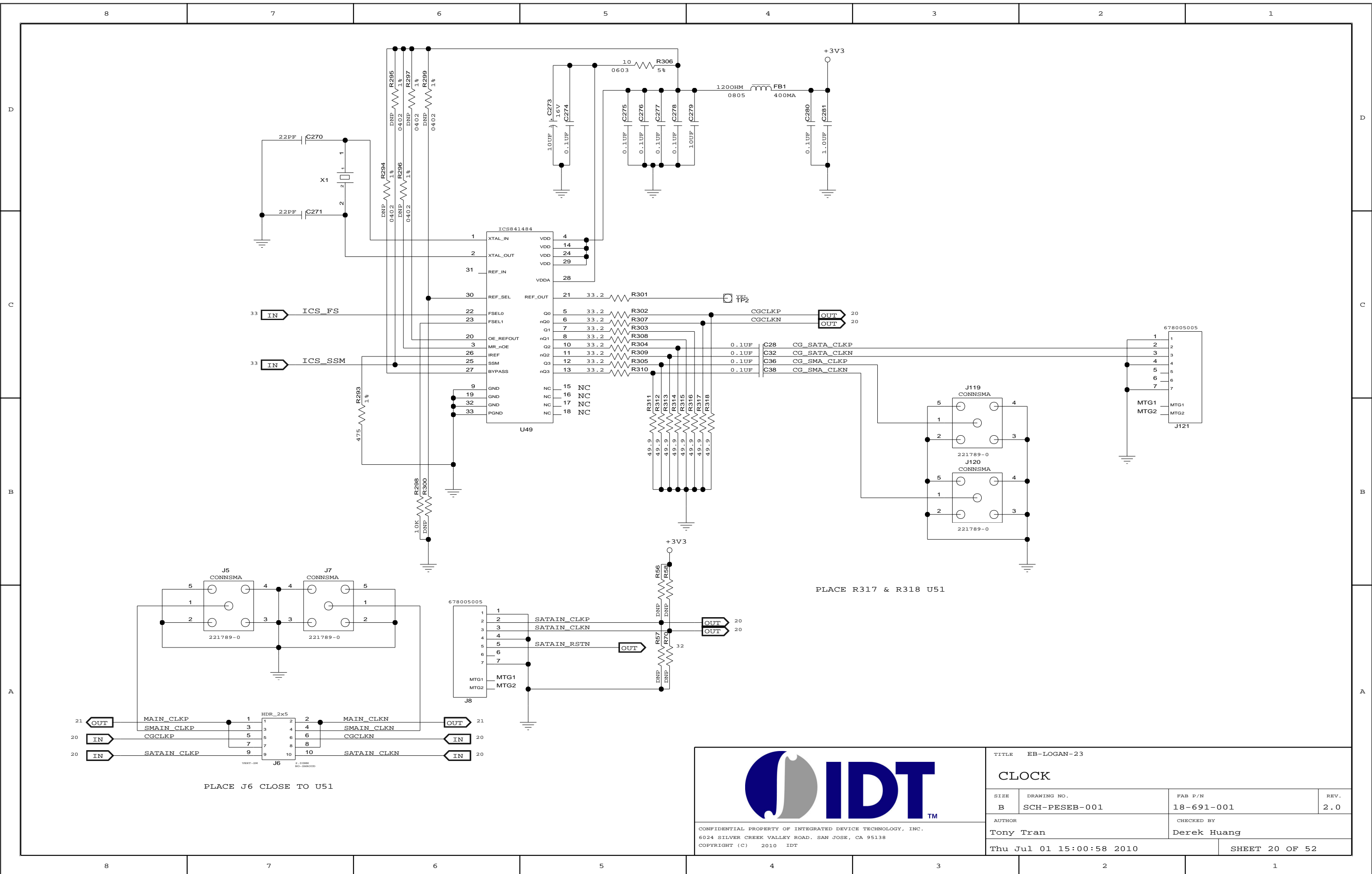



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SLOT RESETS AND WAKE PULL-UPS

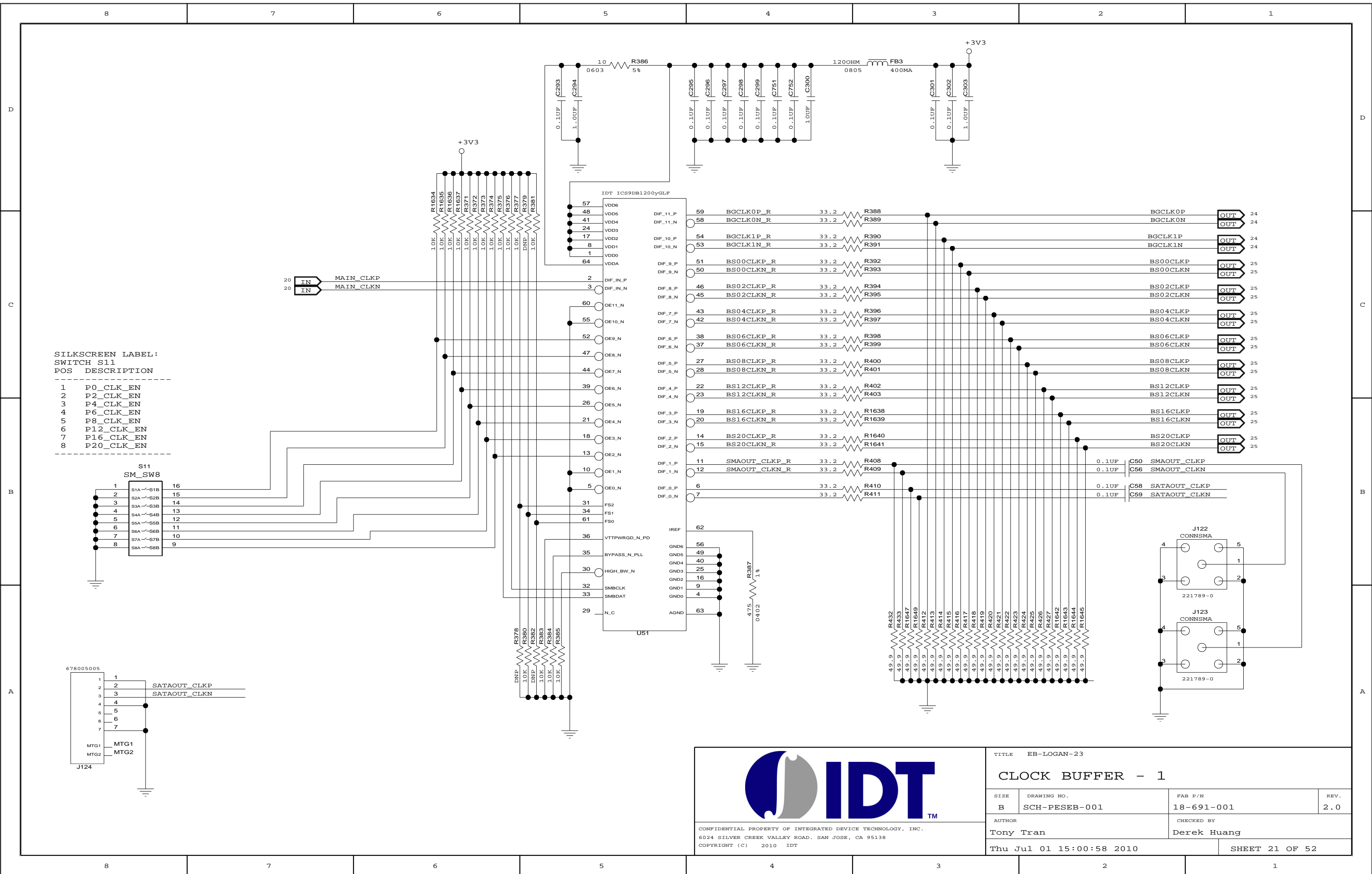
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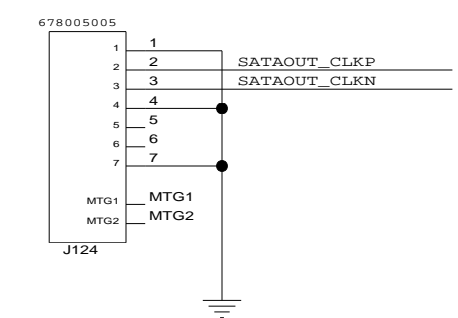
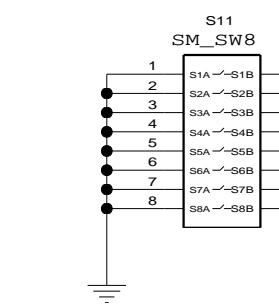
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TITLE EB-LOGAN-23			
CLOCK			
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B	SCH-PESEB-001	18-691-001	2.0
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Tony Tran		Derek Huang	
Thu Jul 01 15:00:58 2010			SHEET 20 OF 52



SILKSCREEN LABEL:
SWITCH S11

POS	DESCRIPTION
1	P0_CLK_EN
2	P2_CLK_EN
3	P4_CLK_EN
4	P6_CLK_EN
5	P8_CLK_EN
6	P12_CLK_EN
7	P16_CLK_EN
8	P20_CLK_EN

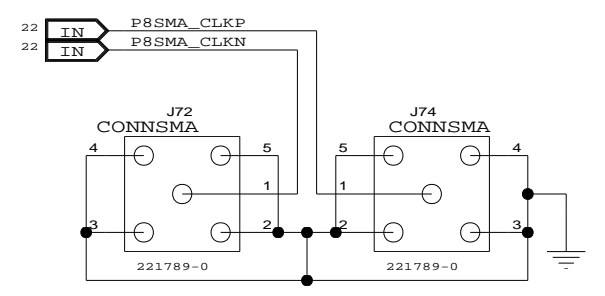
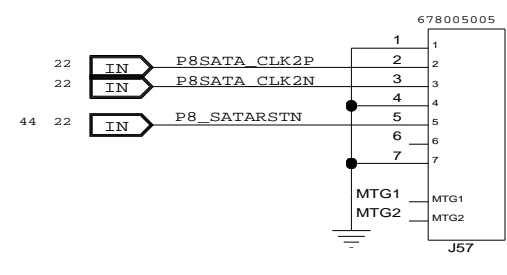
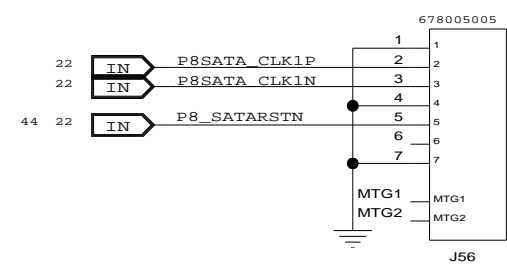
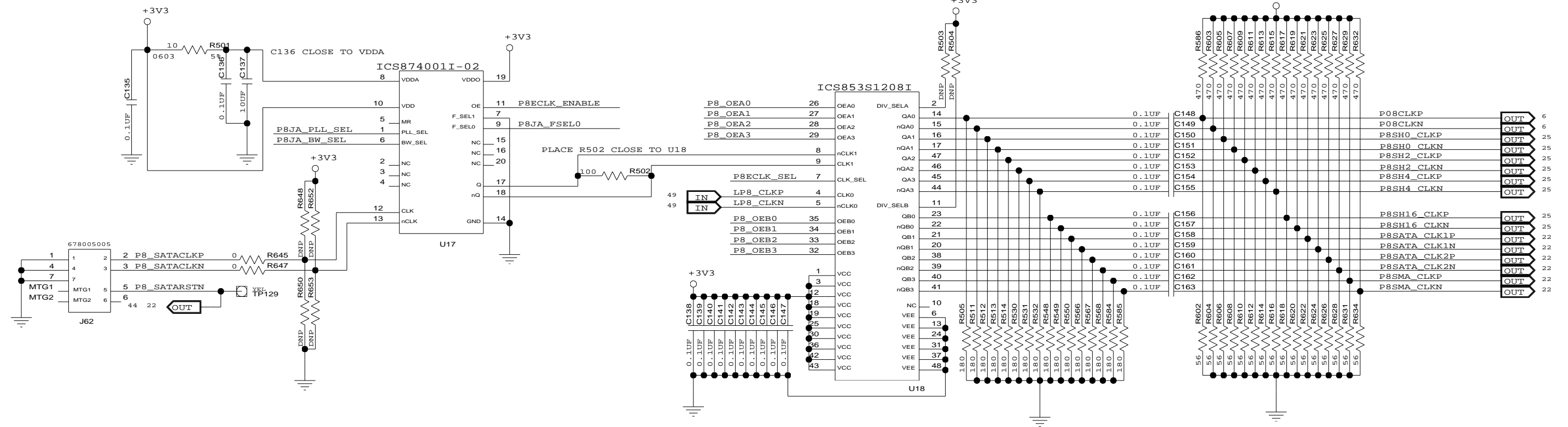


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TITLE EB-LOGAN-23			
CLOCK BUFFER - 1			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:00:58 2010			SHEET 21 OF 52

P8CLK - DUT PORT 8 CLK
 LP8CLK - LOCAL CLOCK GEN. PORT 8 CLK
 P8SHXCLK - TO SLOT CLK HEADERS

PLACE 470 AND 56 OHM RESISTORS CLOSE TO DESTINATION.

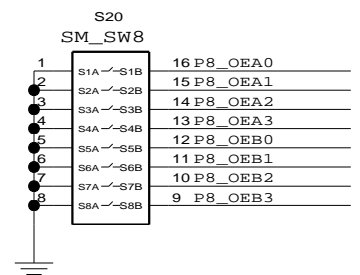
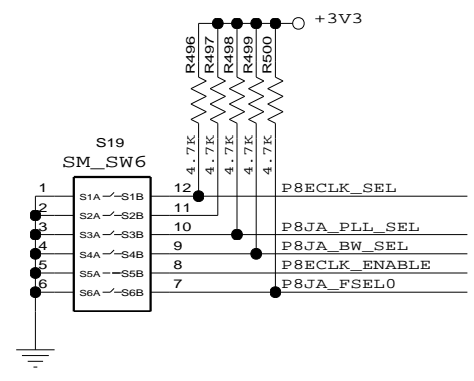


DEFAULT DIPSW SETTING

- S19:1 OFF (SATACLK)
- S19:3 OFF (PLL)
- S19:4 OFF (2.2MHZ)
- S19:5 OFF (U17 OUTPUT ON)
- S19:6 ON (100MHZ)

U18 OUTPUTS

- OFF (ENABLE)
- ON (DISABLE)

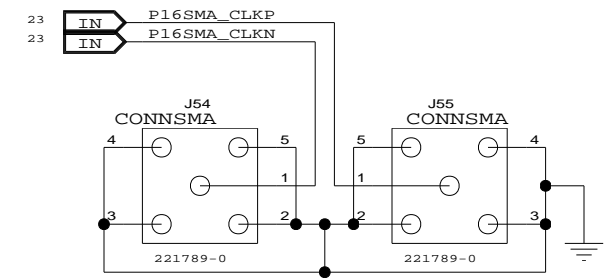
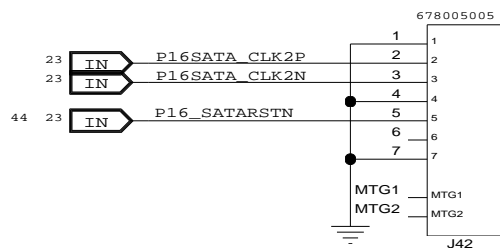
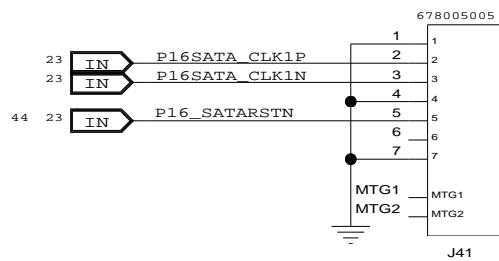
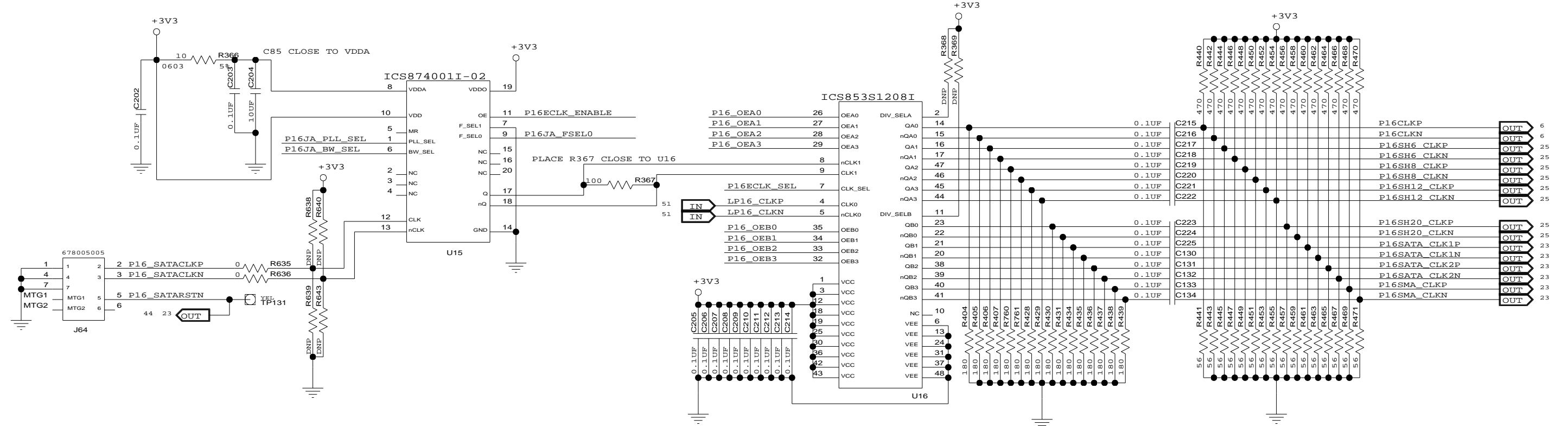


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TITLE EB-LOGAN-23			
CLOCK SELECTOR DUT PCLK 8			
SIZE B	DRAWING NO. SCH-PESEB-001	FAB P/N 18-691-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Tue Aug 10 13:51:12 2010			SHEET 22 OF 52

P16CLK - DUT PORT 16 CLK
 LP16CLK - LOCAL CLOCK GEN. PORT 16 CLK
 P16SHXCLK - TO SLOT CLK HEADERS

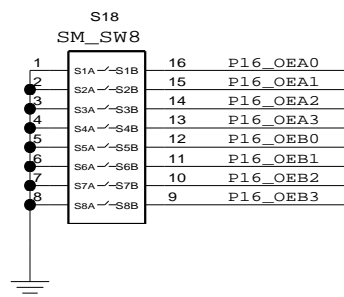
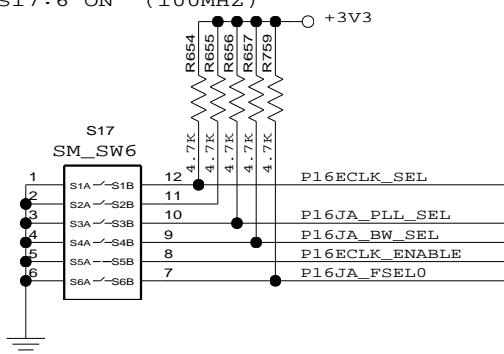
PLACE 470 AND 56 OHM RESISTORS CLOSE TO DESTINATION.



DEFAULT DIPSW SETTING

- S17:1 OFF (SATACLK)
- S17:3 OFF (PLL)
- S17:4 OFF (2.2MHZ)
- S17:5 OFF (U15 OUTPUT ON)
- S17:6 ON (100MHZ)

U16 OUTPUTS
 OFF (ENABLE)
 ON (DISABLE)



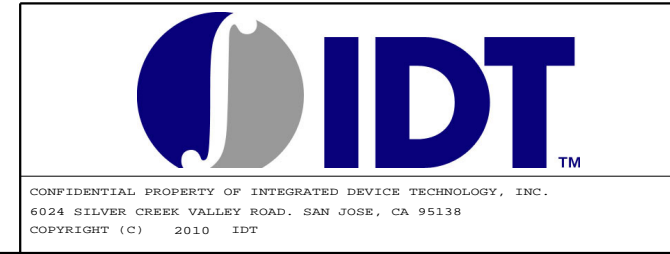
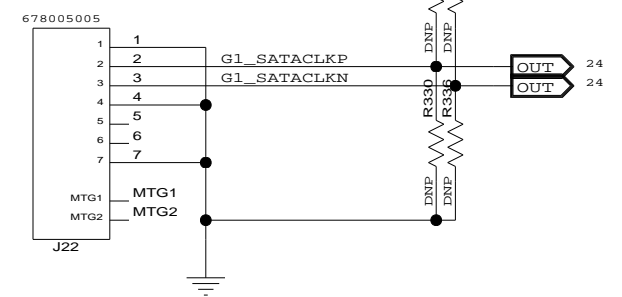
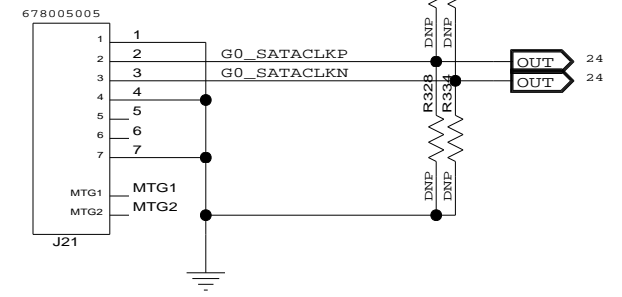
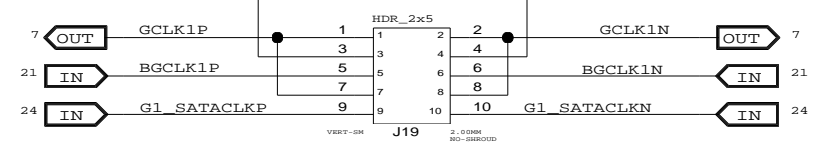
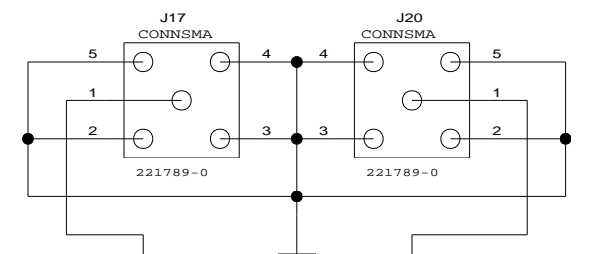
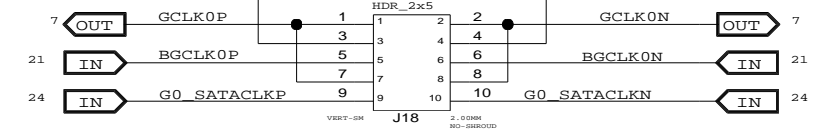
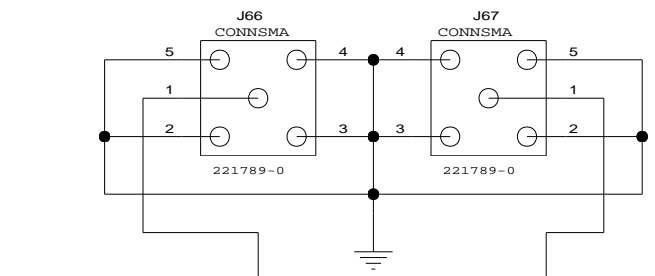
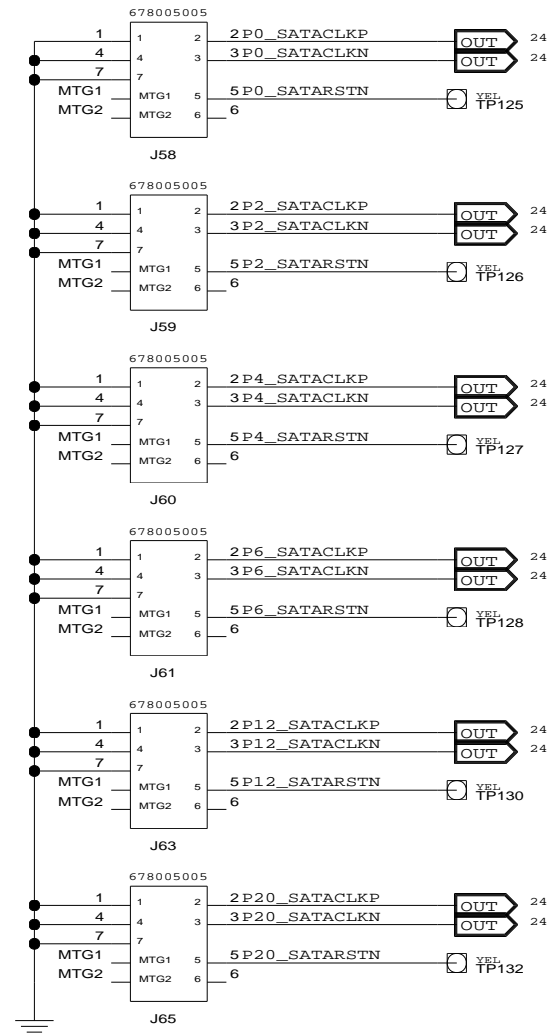
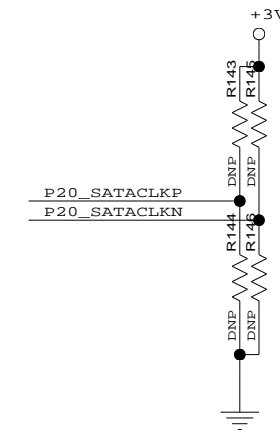
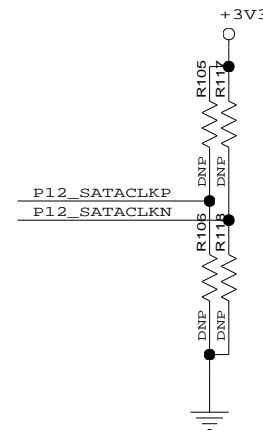
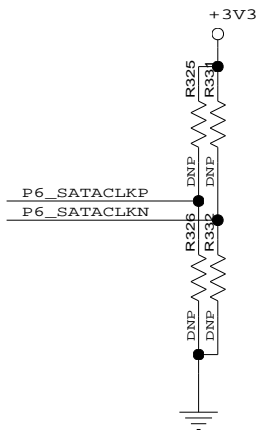
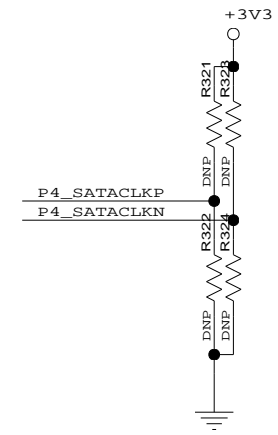
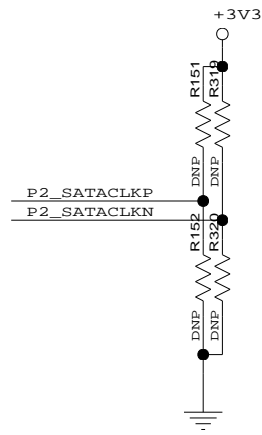
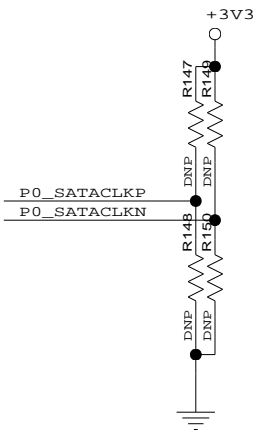
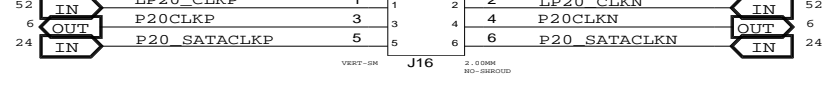
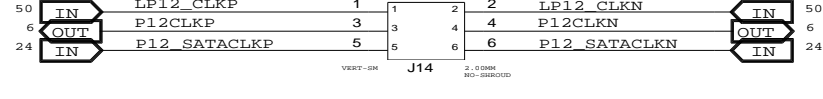
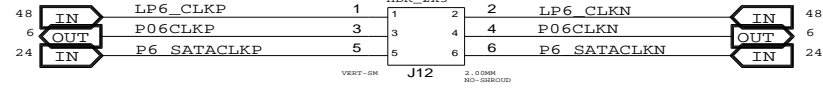
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TITLE EB-LOGAN-23

CLOCK SELECTOR DUT PCLK 16

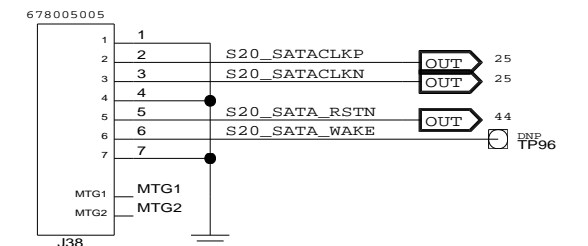
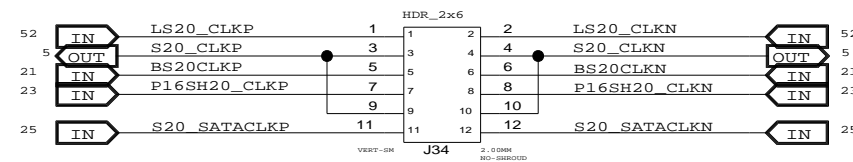
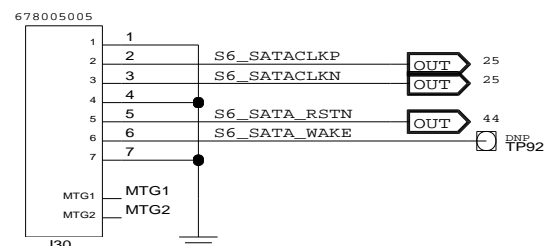
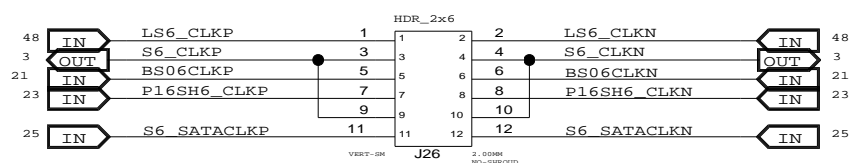
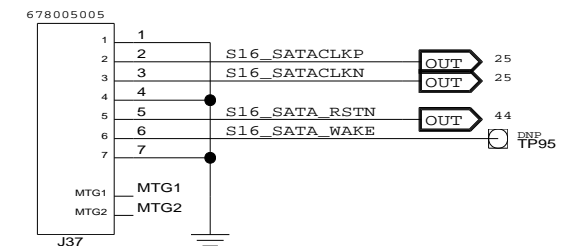
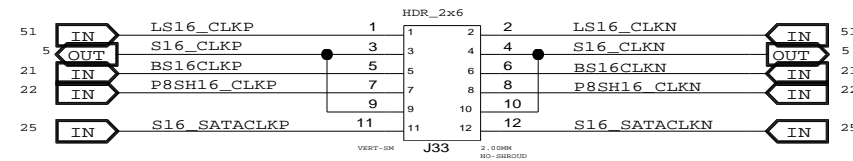
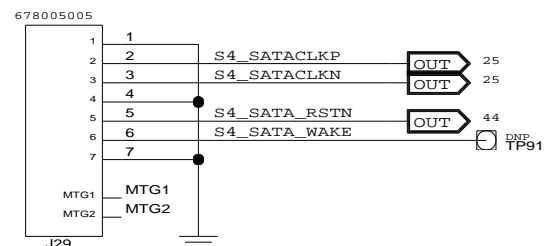
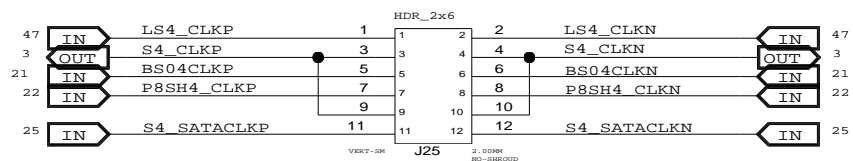
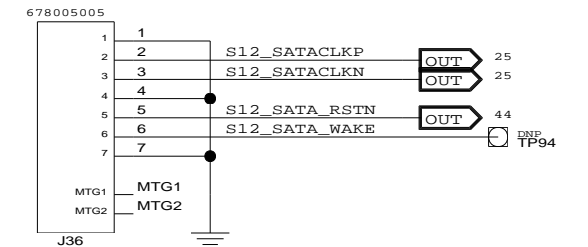
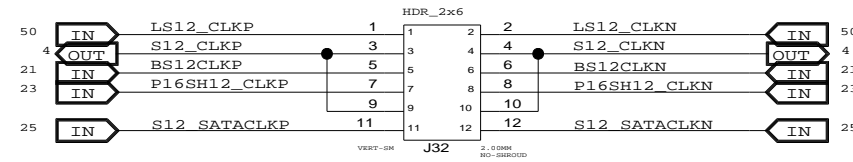
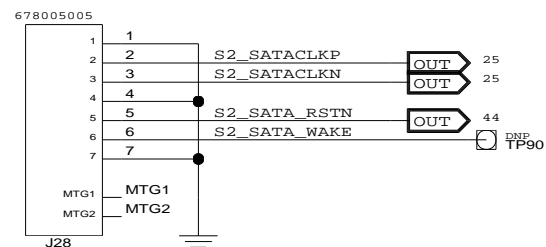
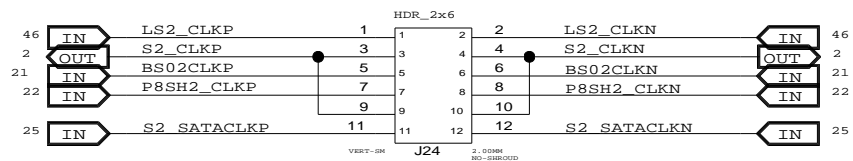
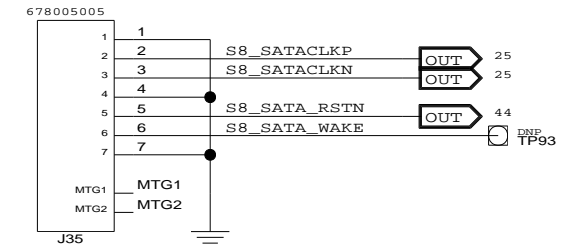
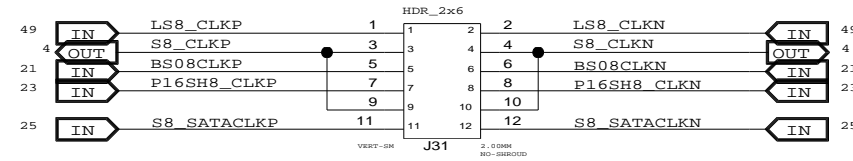
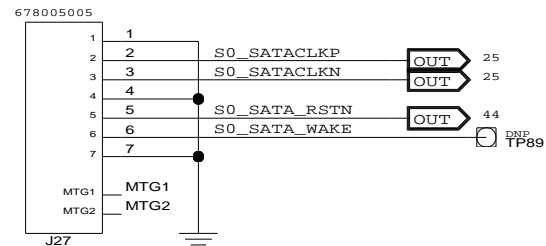
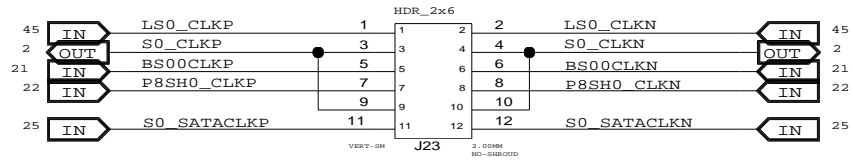
SIZE B	DRAWING NO. SCH-PESEB-001	FAB P/N 18-691-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Tue Aug 10 13:51:21 2010			SHEET 23 OF 52

EXXCLK - DUT CLK
 LPXXCLK - LOCAL CLOCK GEN. PORT CLK
 SHXXCLK - SLOT HDR. CLK



TITLE EB-LOGAN-23			
CLOCK SELECTOR DUT PCLK 0-20, GCLK 0-1			
SIZE B	DRAWING NO. SCH-PESEB-001	FAB P/N 18-691-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jul 01 15:00:59 2010			SHEET 24 OF 52

SXXCLK - SLOT CLK
 BSXXCLK - BUFFER SLOT CLK
 LSXXCLK - LOCAL CLOCK GEN. SLOT CLK
 SHXXCLK - SLOT HDR.CLK



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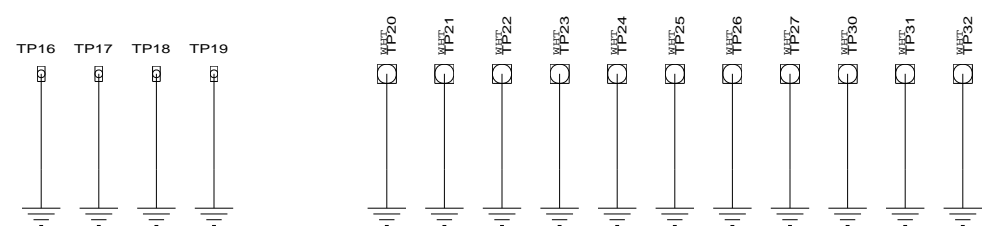
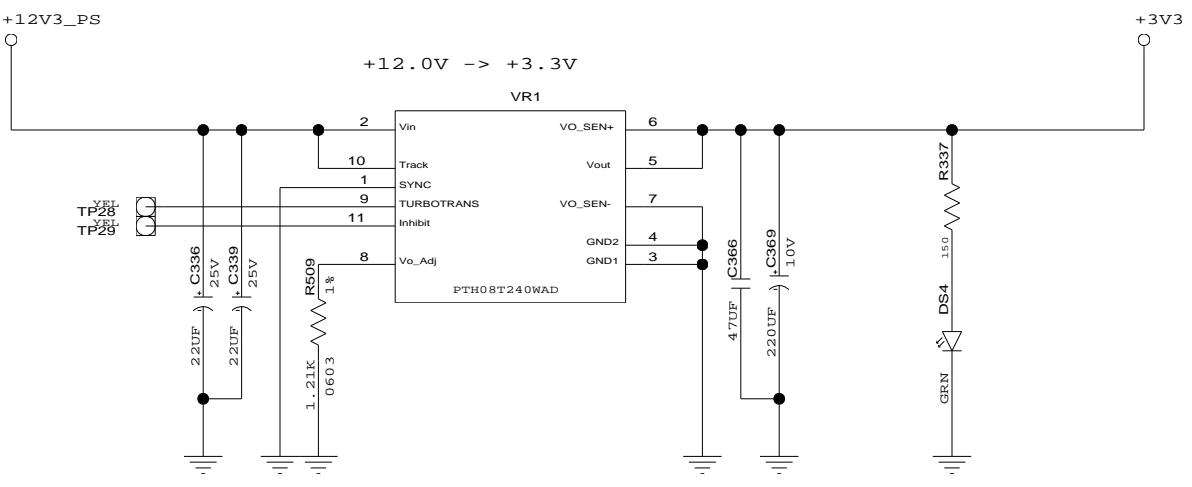
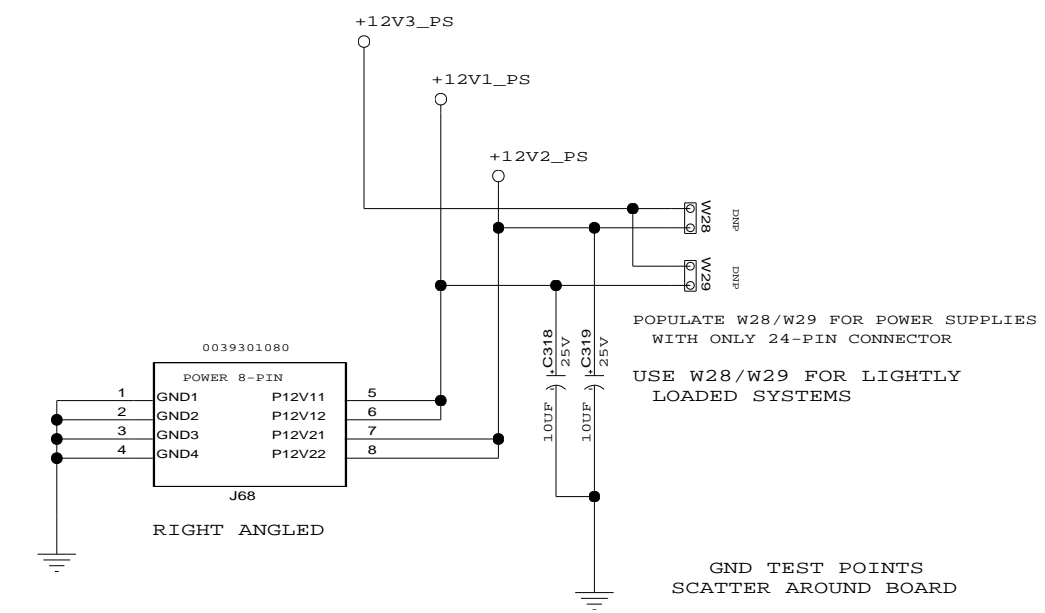
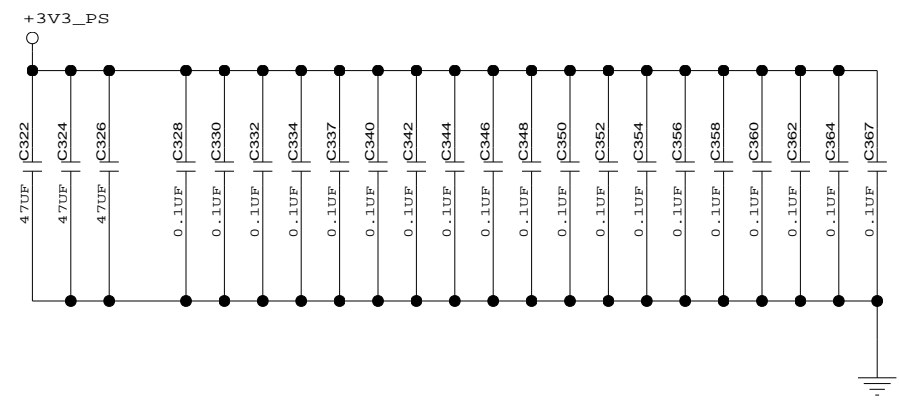
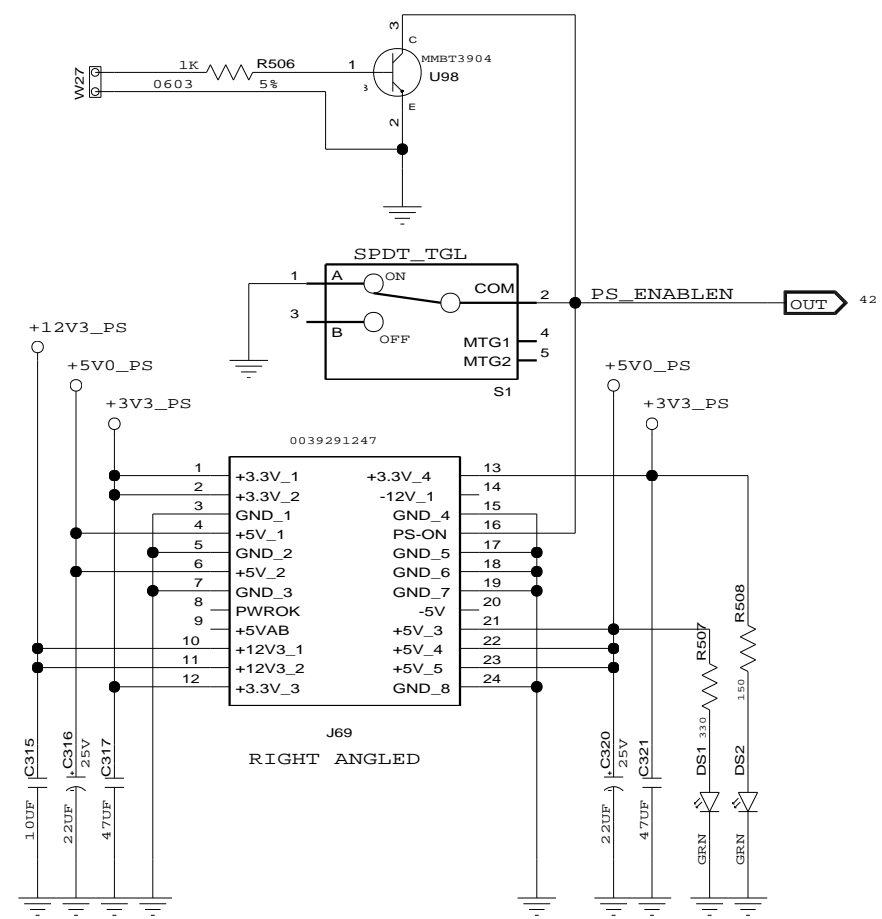
TITLE EB-LOGAN-23

CLOCK SELECTOR SLOTS 0-20

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	

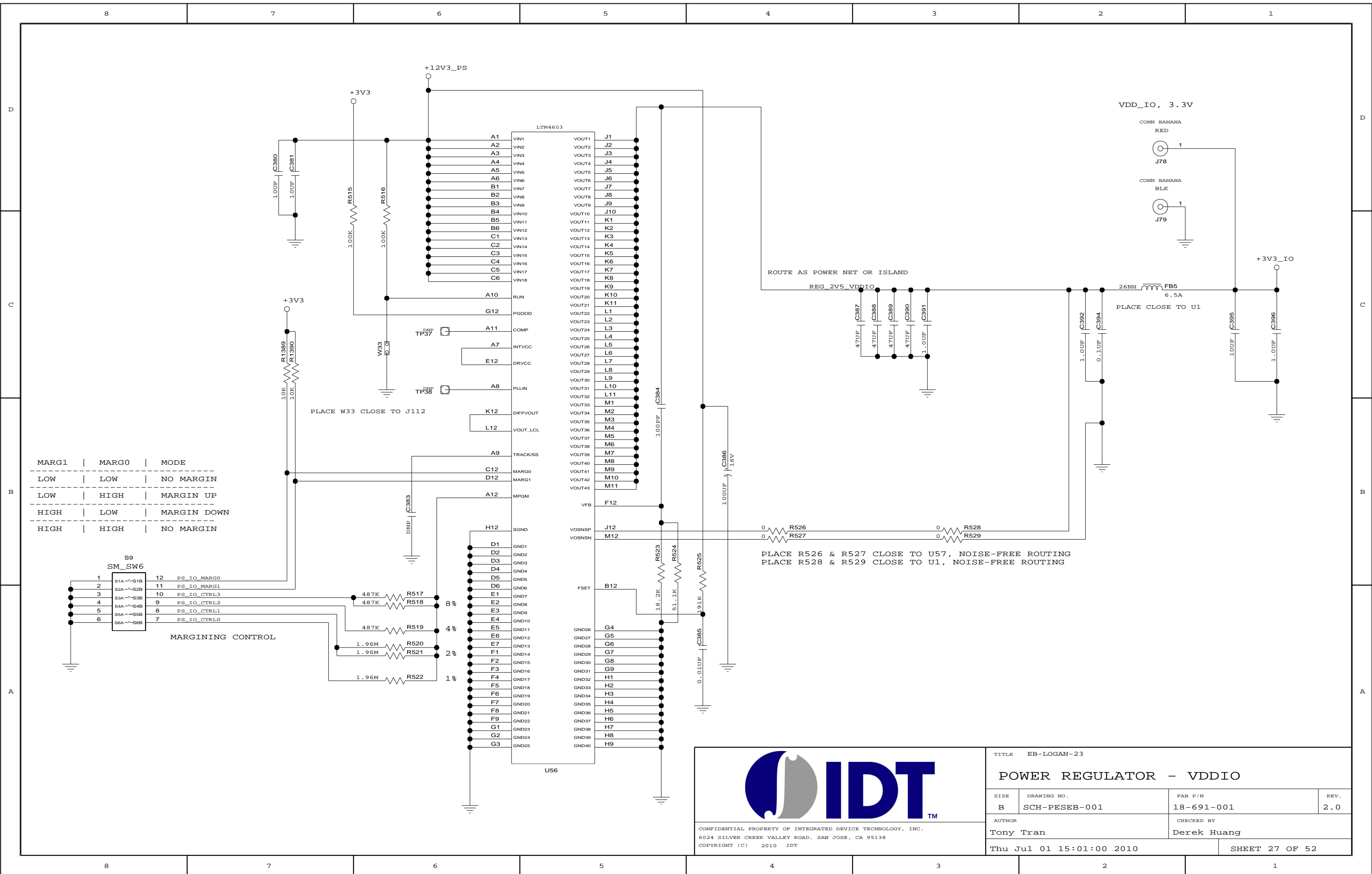
Thu Jul 01 15:00:59 2010

SHEET 25 OF 52



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TITLE EB-LOGAN-23			
POWER CONNECTORS			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:01:00 2010			SHEET 26 OF 52

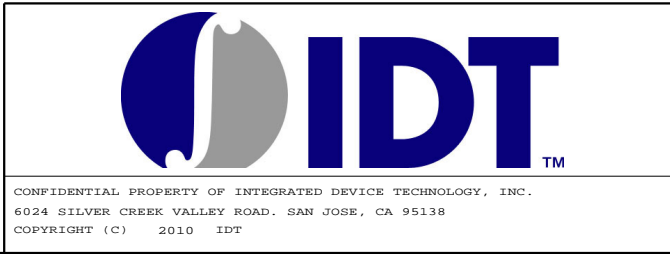
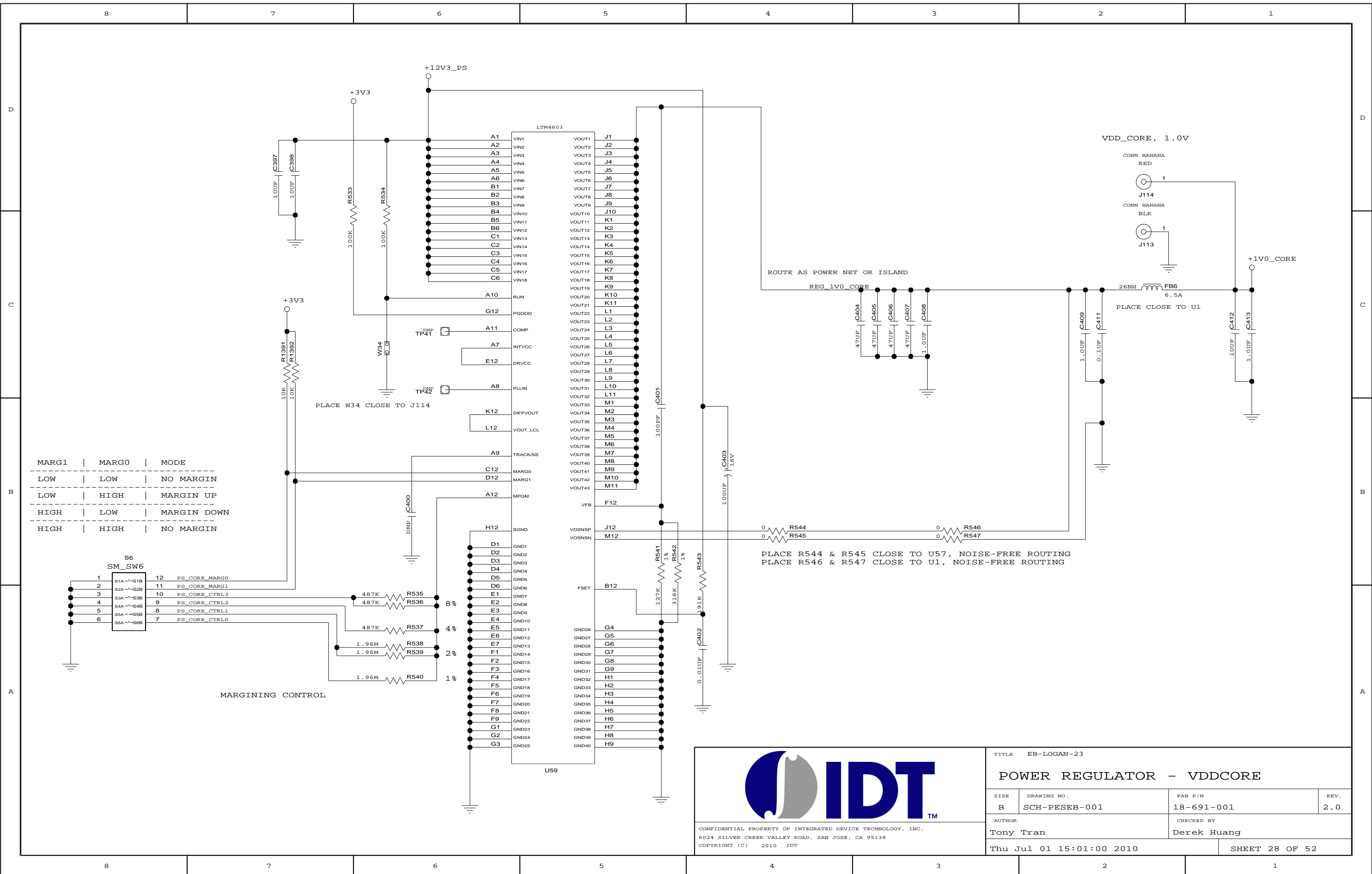


MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

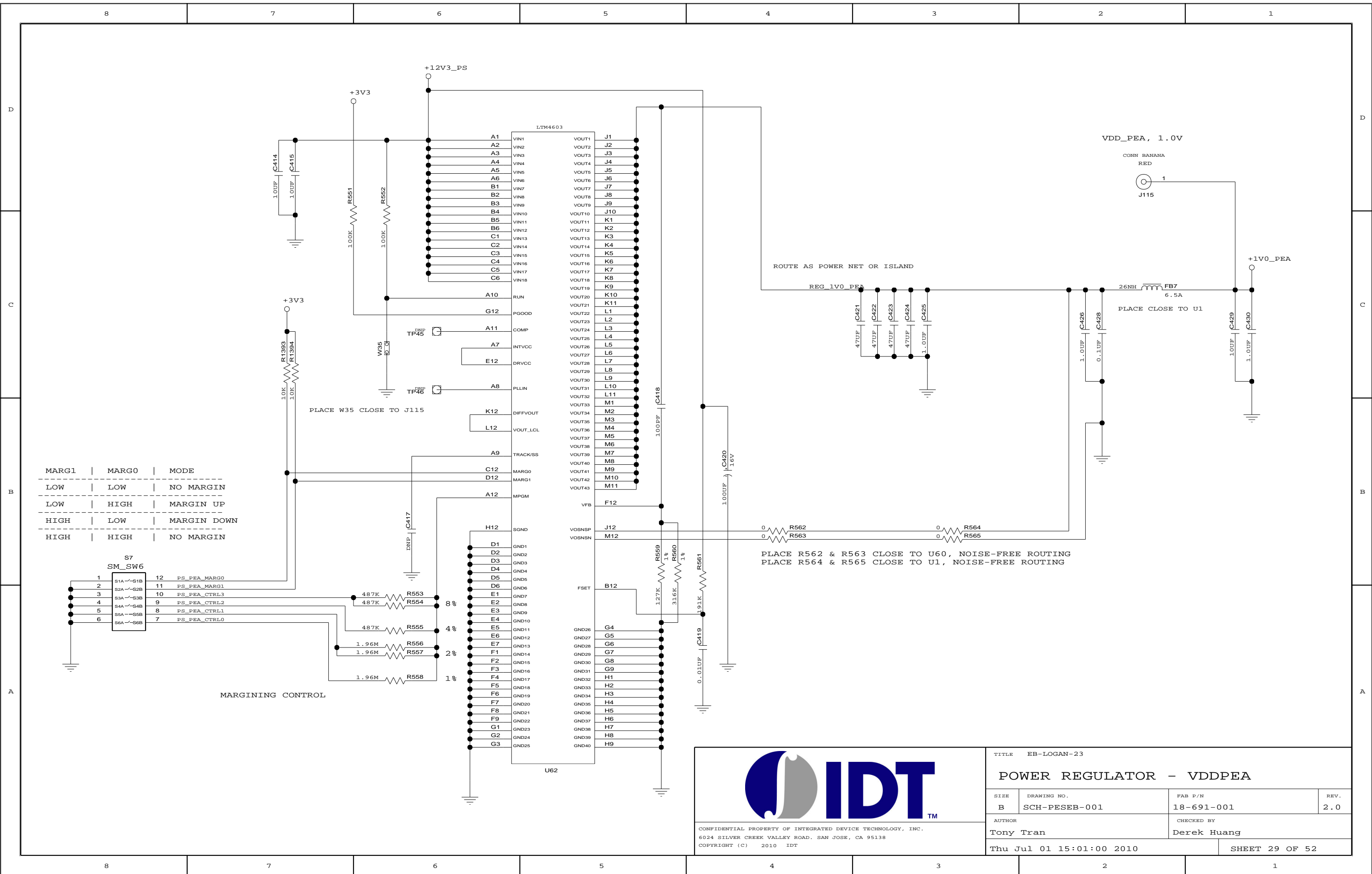
MARGINING CONTROL

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TITLE EB-LOGAN-23			
POWER REGULATOR - VDDIO			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:01:00 2010			SHEET 27 OF 52




TITLE EB-LOGAN-23			
POWER REGULATOR - VDDCORE			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:01:00 2010			SHEET 28 OF 52



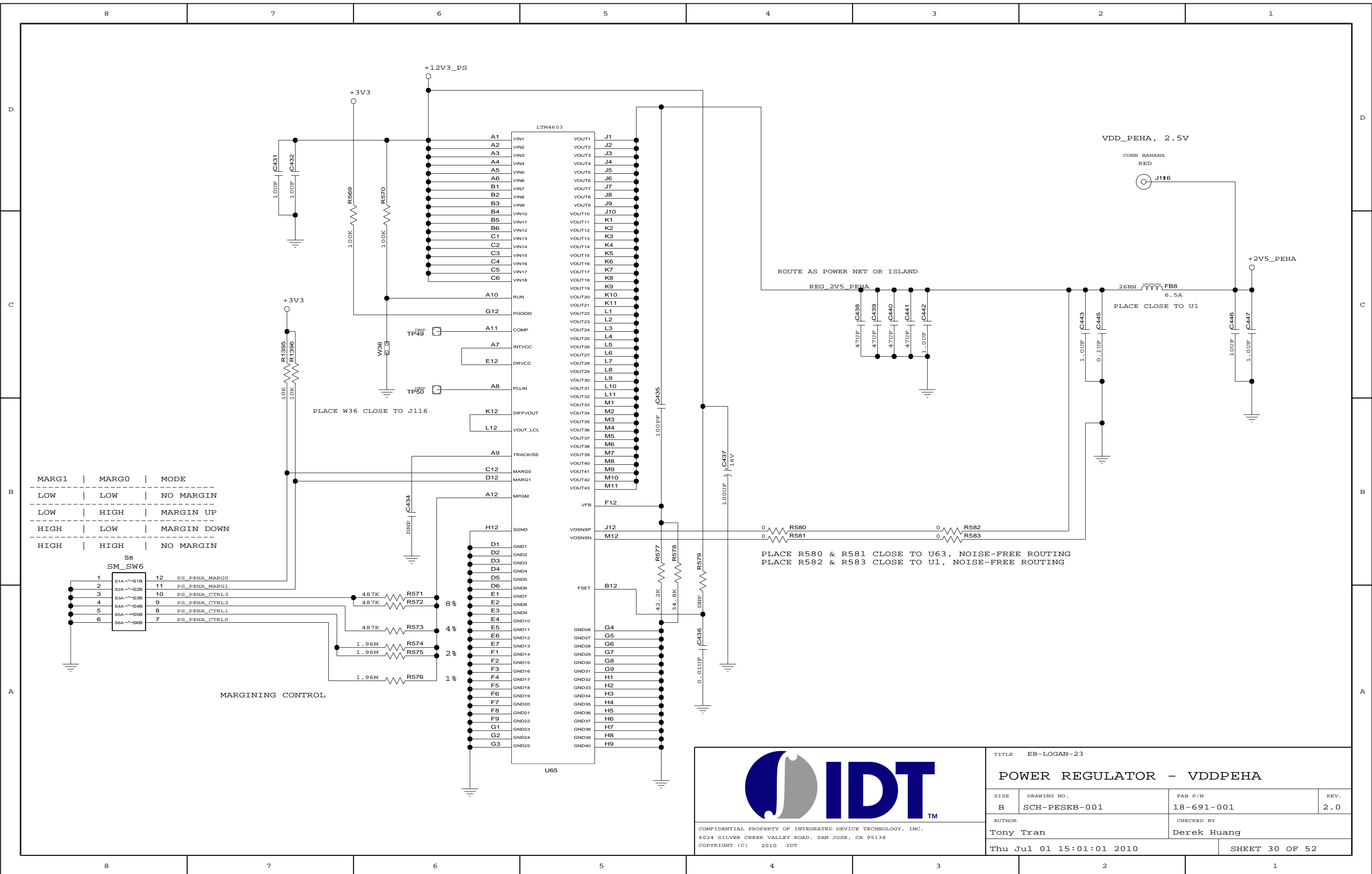
MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

MARGINING CONTROL



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TITLE EB-LOGAN-23			
POWER REGULATOR - VDDPEA			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:01:00 2010			SHEET 29 OF 52

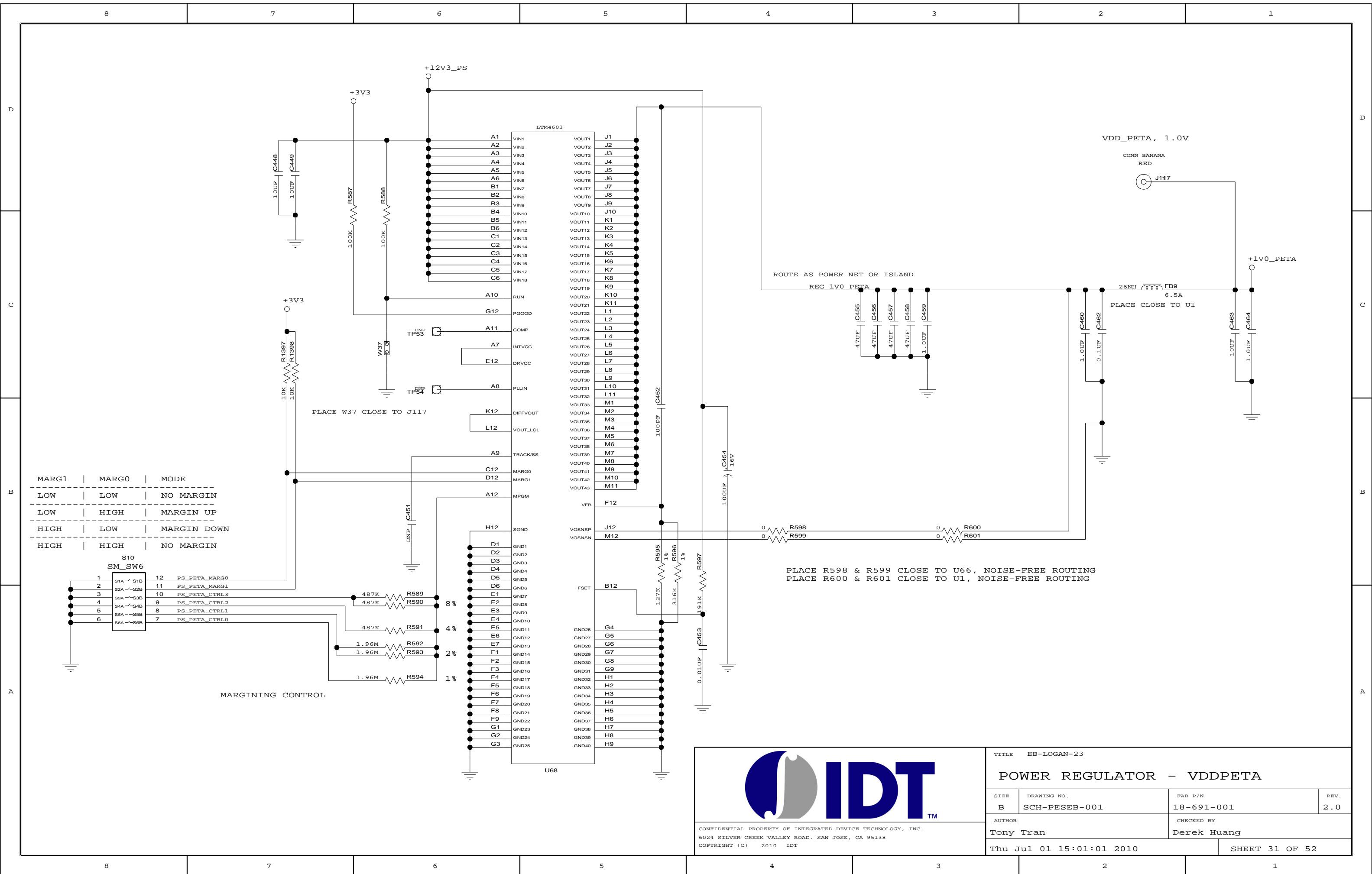


MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

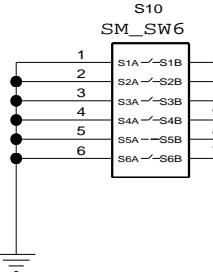
MARGINING CONTROL

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TITLE EB-LOGAN-23			
POWER REGULATOR - VDDPEHA			
SIZE B	DRAWING NO. SCH-PESEB-001	FAB P/N 18-691-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jul 01 15:01:01 2010			SHEET 30 OF 52



MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

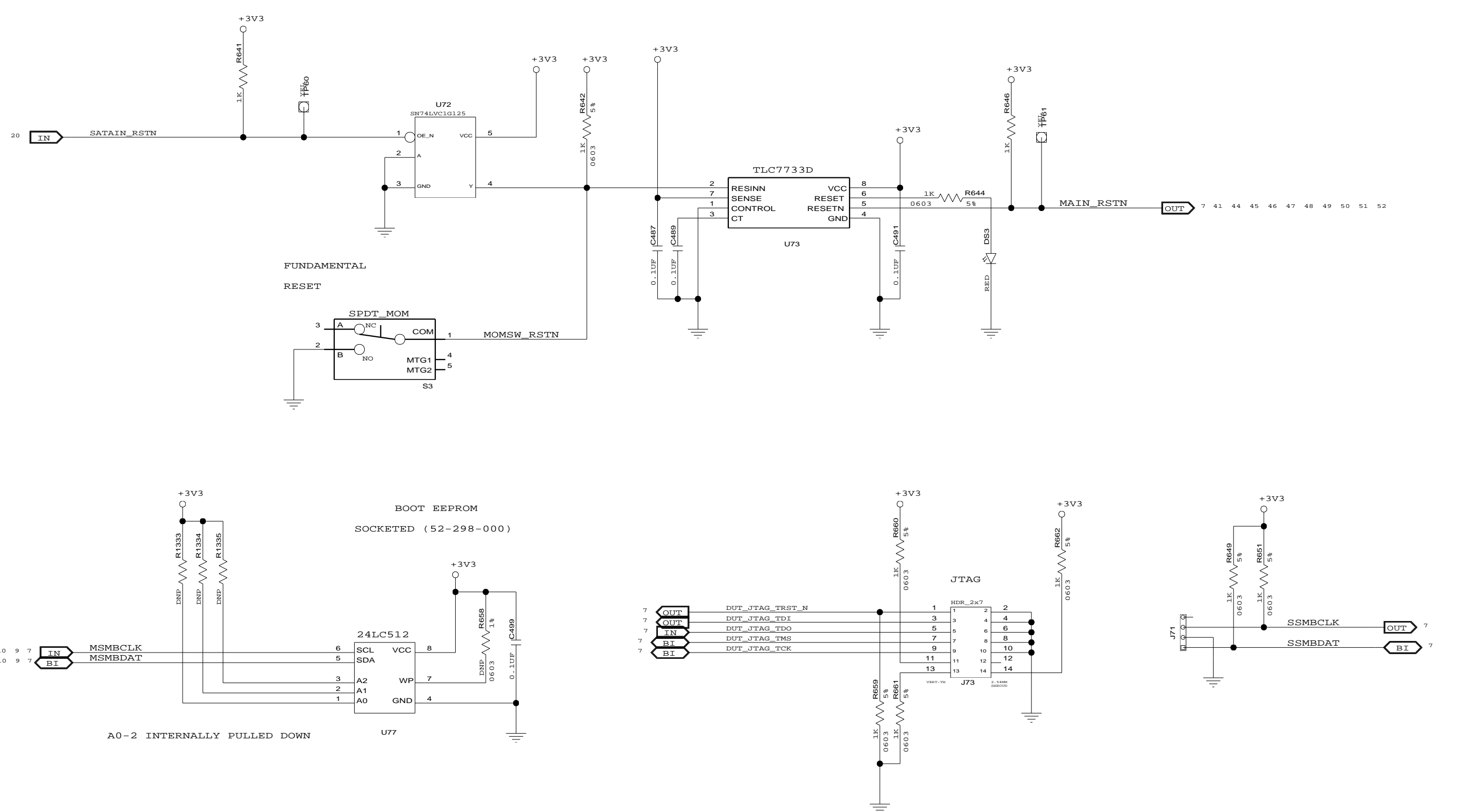



MARGINING CONTROL

PLACE R598 & R599 CLOSE TO U66, NOISE-FREE ROUTING
 PLACE R600 & R601 CLOSE TO U1, NOISE-FREE ROUTING

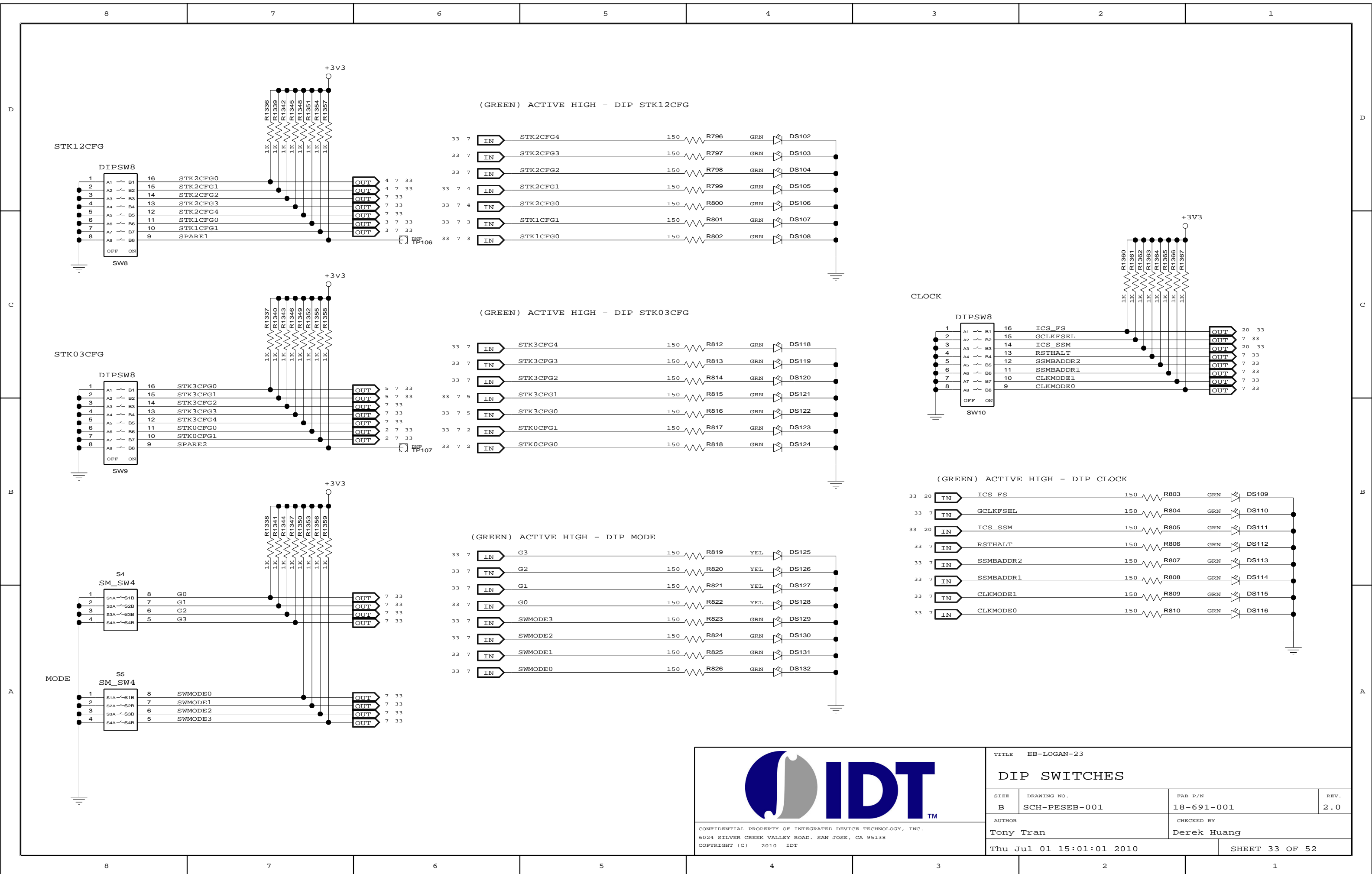
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TITLE EB-LOGAN-23			
POWER REGULATOR - VDDPETA			
SIZE B	DRAWING NO. SCH-PESEB-001	FAB P/N 18-691-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jul 01 15:01:01 2010			SHEET 31 OF 52



		TITLE EB-LOGAN-23		
		RESET, SMBUS, EEPROM, JTAG		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	SCH-PESEB-001	18-691-001	2.0	
AUTHOR		CHECKED BY		
Tony Tran		Derek Huang		
Thu Jul 01 15:01:01 2010			SHEET 32 OF 52	

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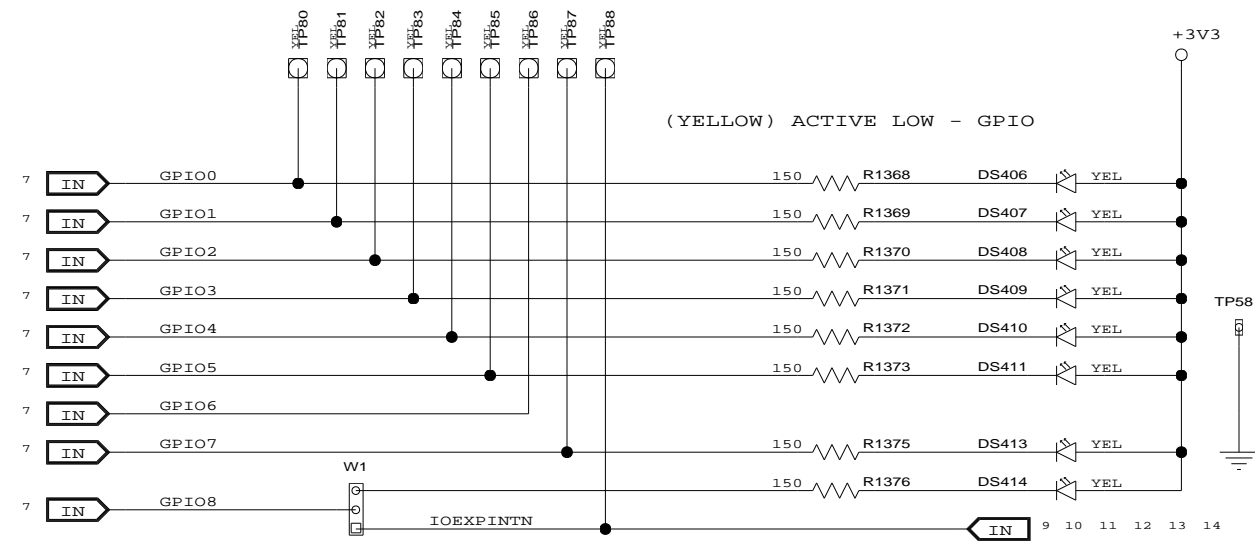


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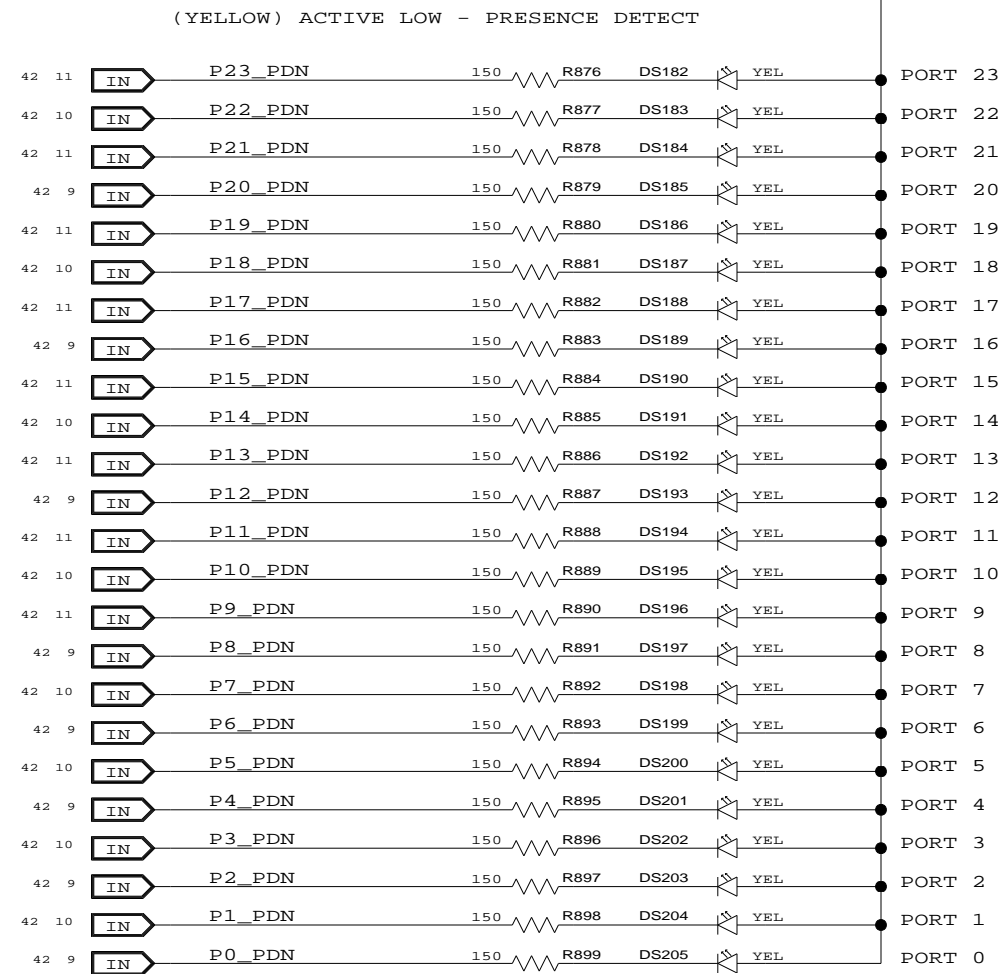
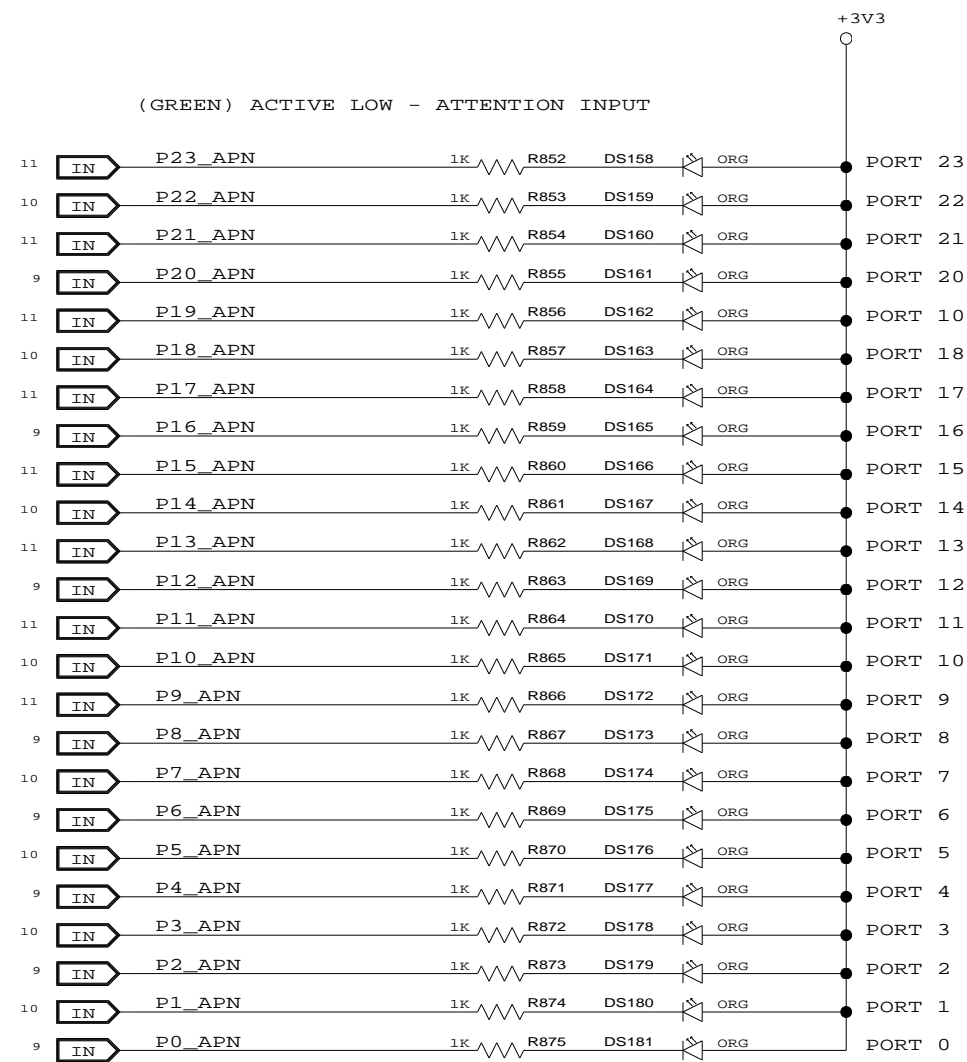
TITLE EB-LOGAN-23

DIP SWITCHES

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:01:01 2010			SHEET 33 OF 52



GPIO	ALT0	ALT1
0	PART0PERSTN	P16LINKUPN
1	PART1PERSTN	P16ACTIVEN
2	PART2PERSTN	P4LINKUPN
3	PART3PERSTN	P4ACTIVEN
4	FAILOVER0	P0LINKUPN
5	GPEN	P0ACTIVEN
6	FAILOVER1	FAILOVER3
7	FAILOVER2	P8LINKUPN
8	IOEXPINTN W1:1-2	P8ACTIVEN W1:2-3



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TITLE EB-LOGAN-23

LED - PORT STATUS (1 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jul 01 15:01:02 2010			SHEET 34 OF 52

D

D

C

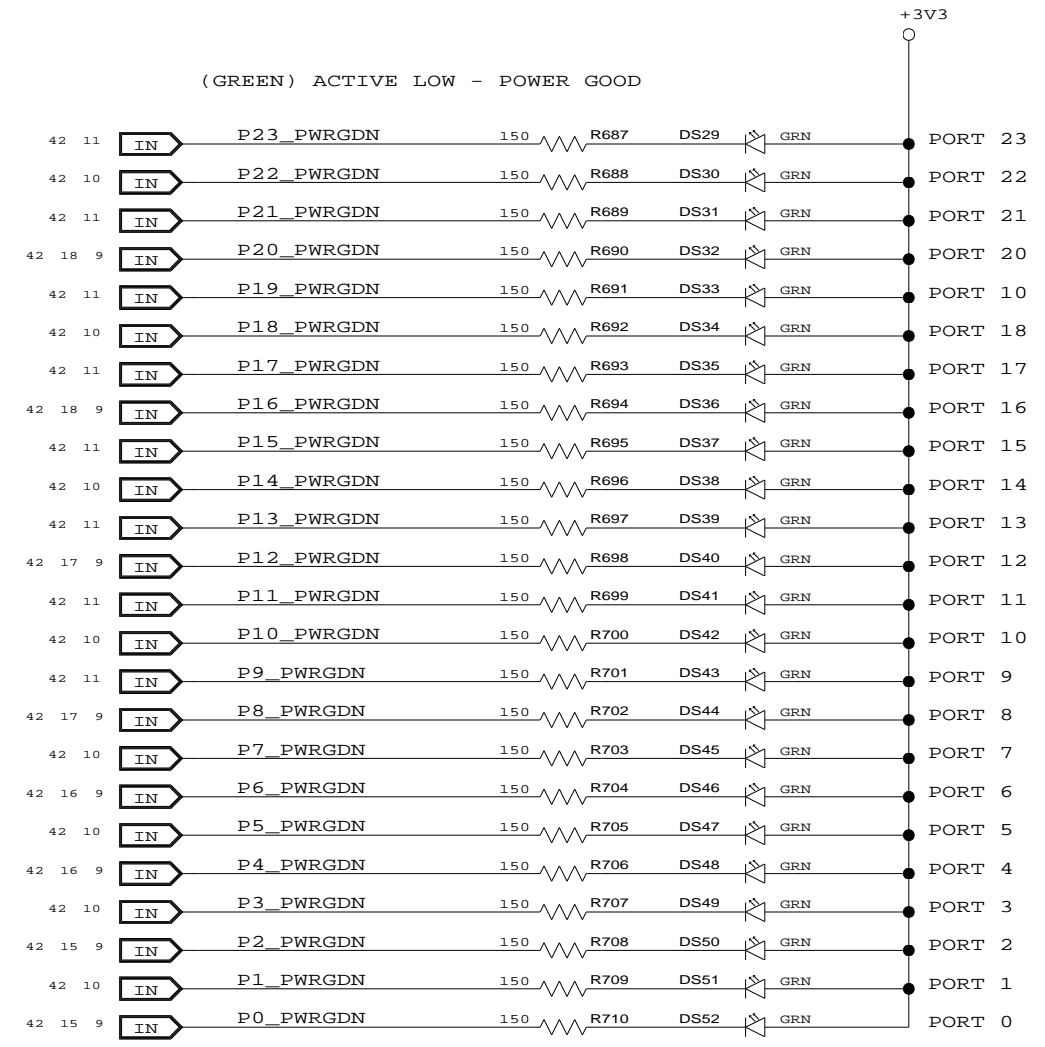
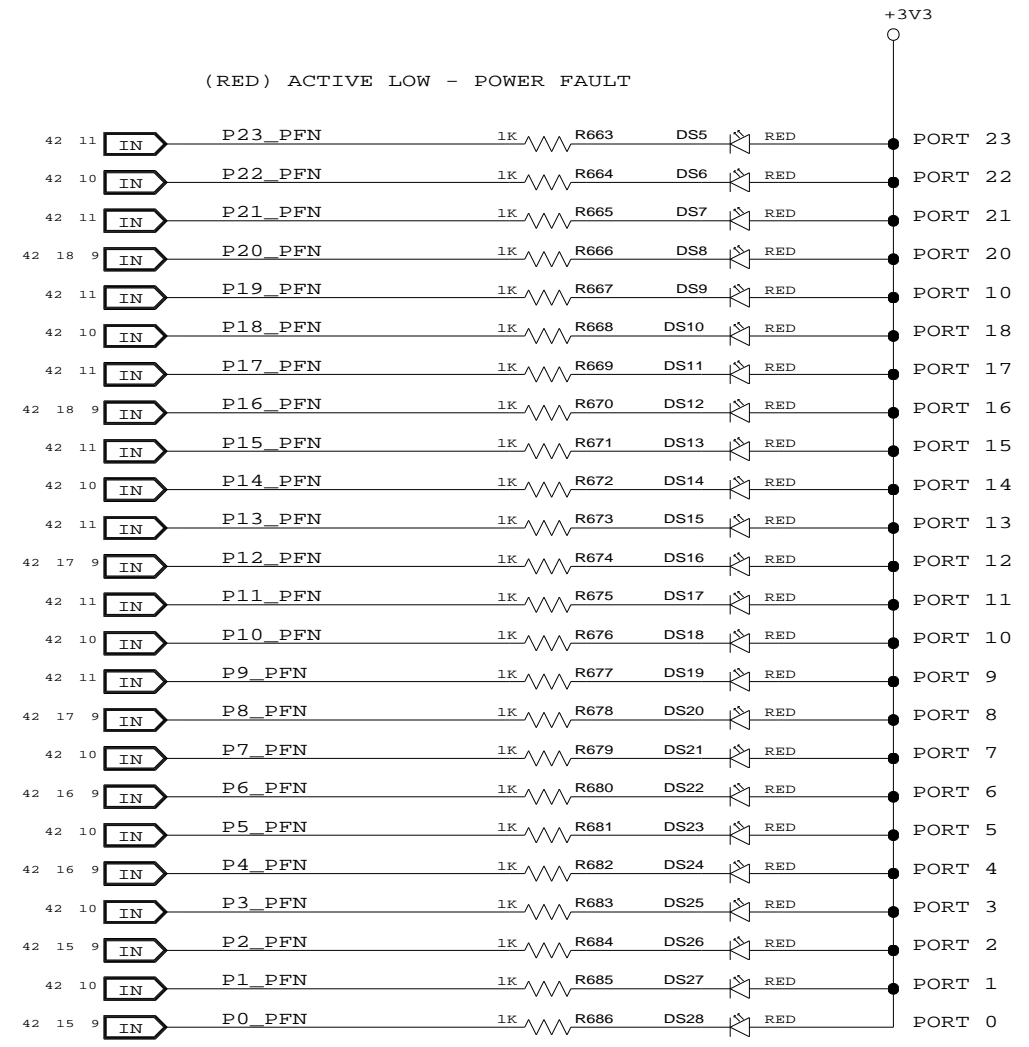
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B

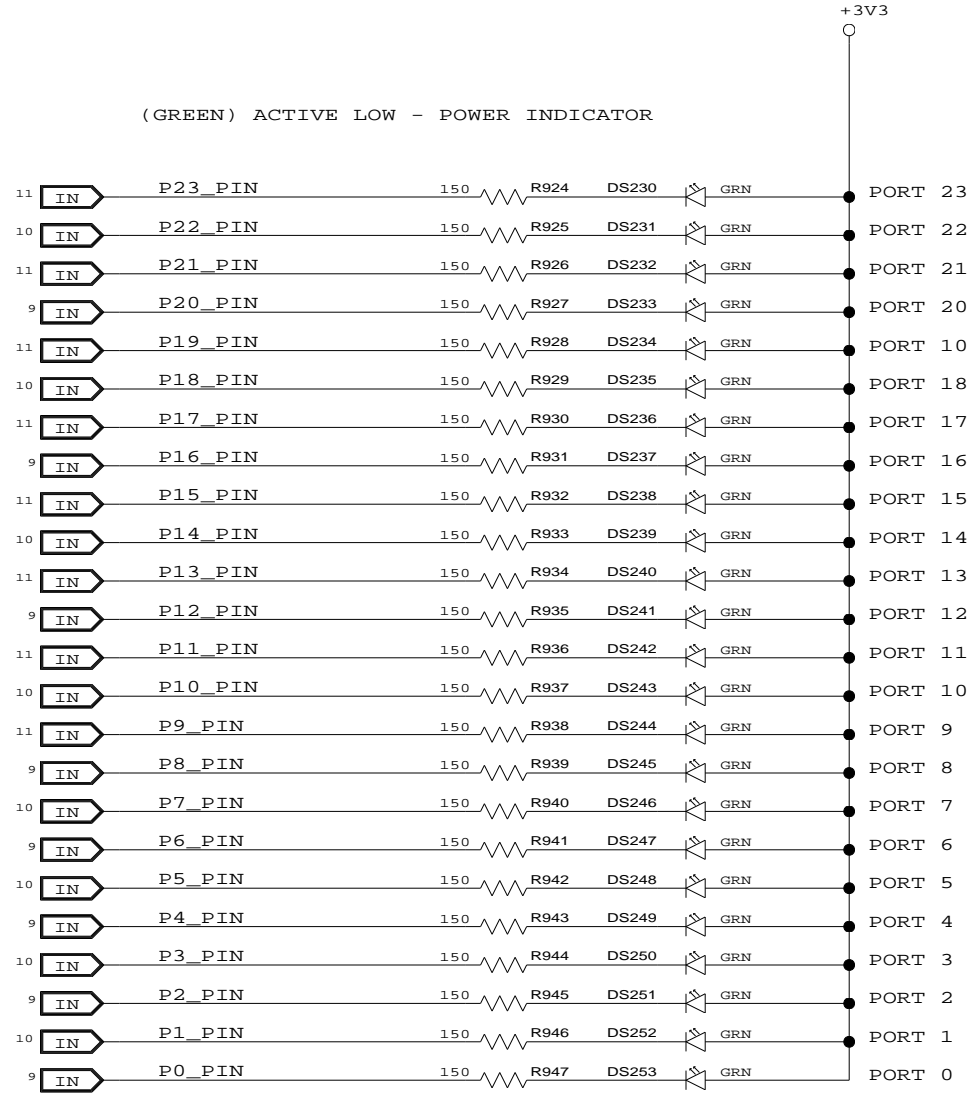
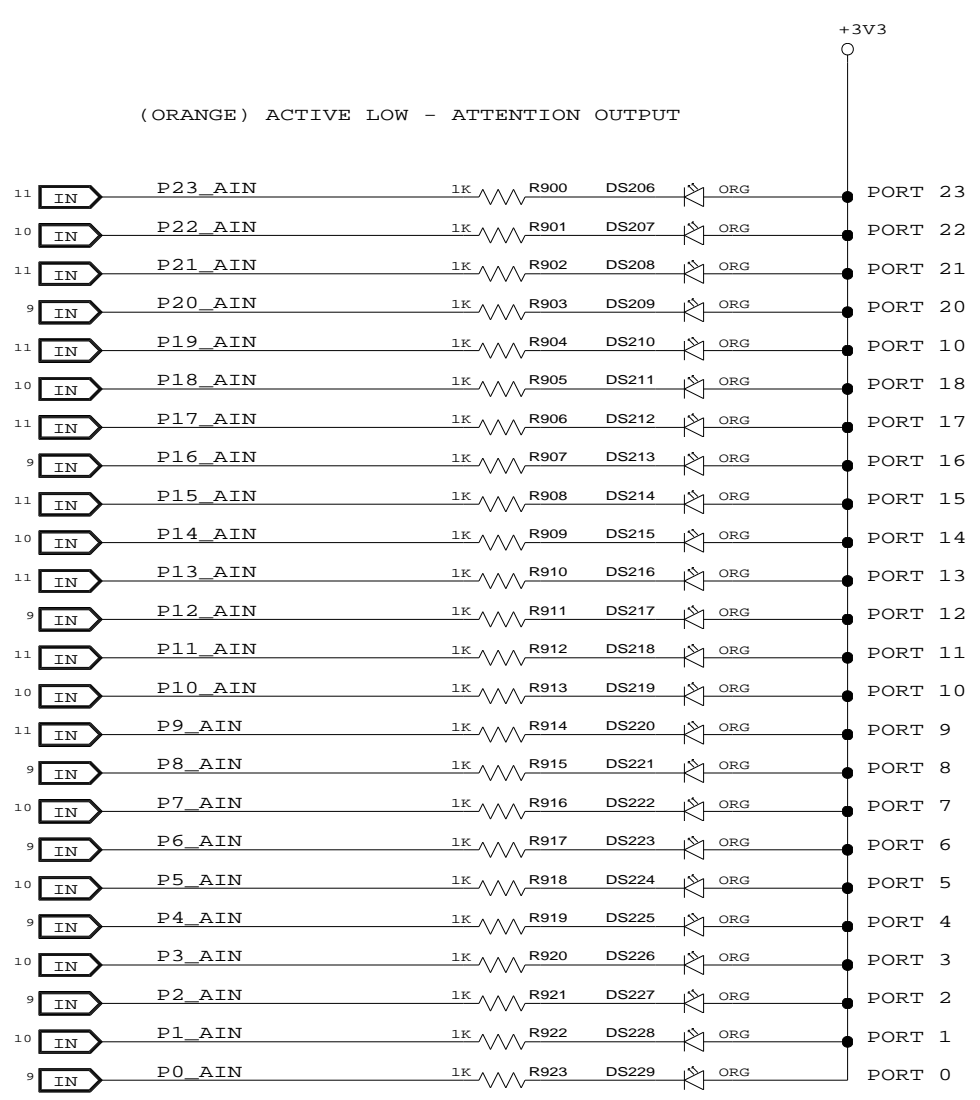
B

A

A



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	LED - PORT STATUS (2 OF 7)		
	SIZE	DRAWING NO.	FAB P/N
	B	SCH-PESEB-001	18-691-001
AUTHOR		CHECKED BY	REV.
Tony Tran		Derek Huang	2.0
Thu Jul 01 15:01:02 2010			SHEET 35 OF 52



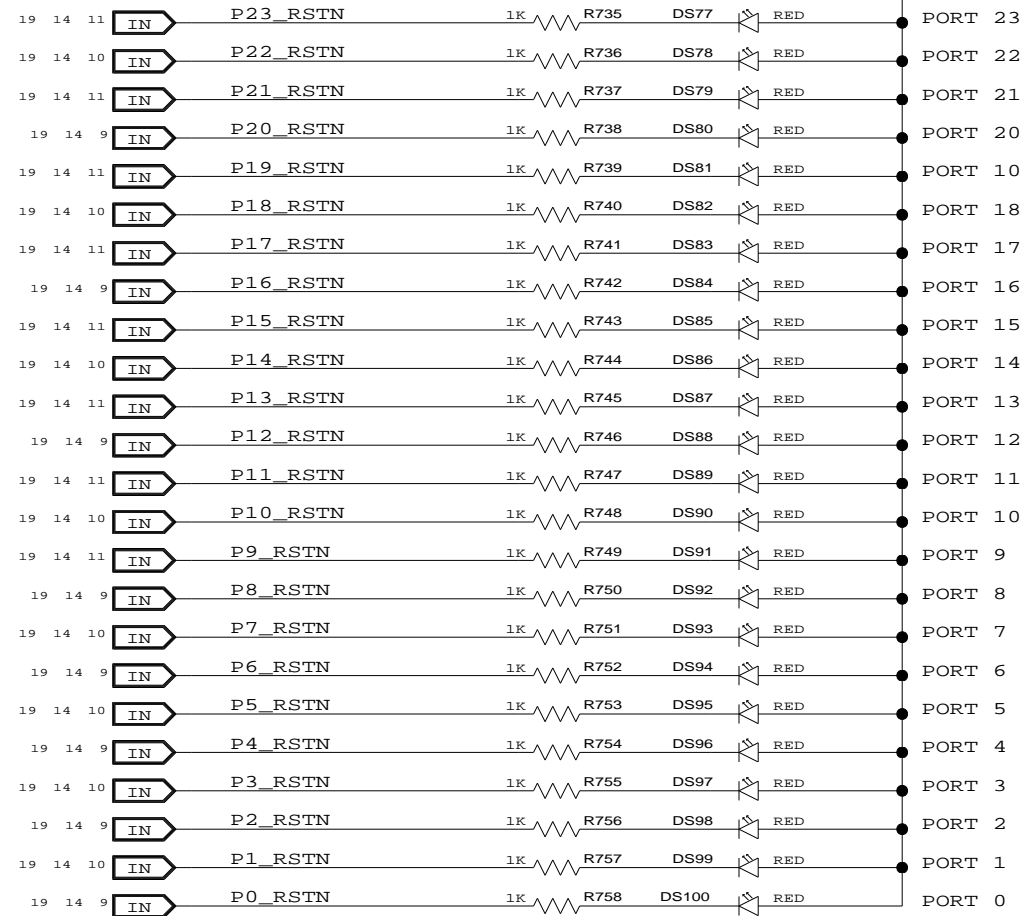
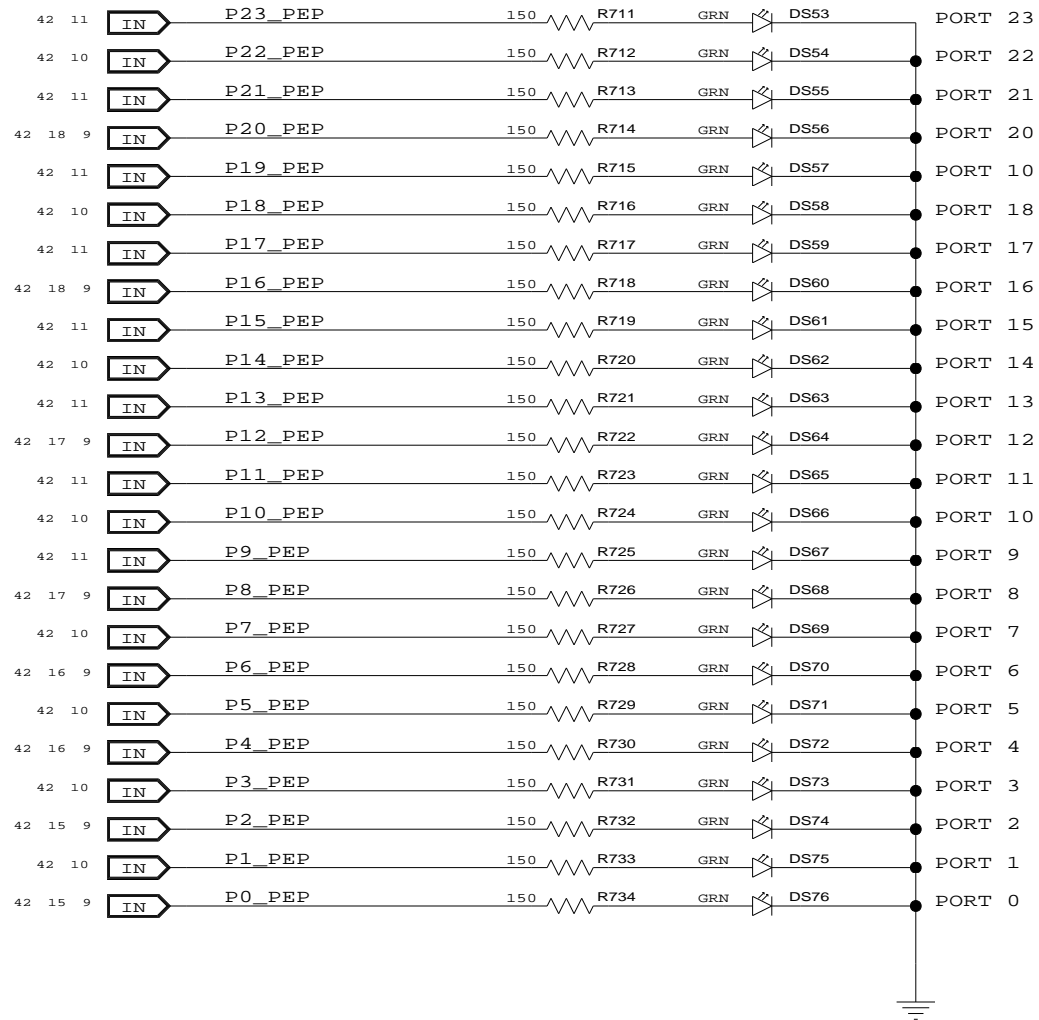
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TITLE EB-LOGAN-23			
LED - PORT STATUS (3 OF 7)			
SIZE B	DRAWING NO. SCH-PESEB-001	FAB P/N 18-691-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jul 01 15:01:02 2010			SHEET 36 OF 52

(GREEN) ACTIVE HIGH - POWER ENABLE

(RED) ACTIVE LOW - HP SLOT RST

+3V3



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TITLE EB-LOGAN-23

LED - PORT STATUS (4 OF 7)

SIZE B	DRAWING NO. SCH-PESEB-001	FAB P/N 18-691-001	REV. 2.0
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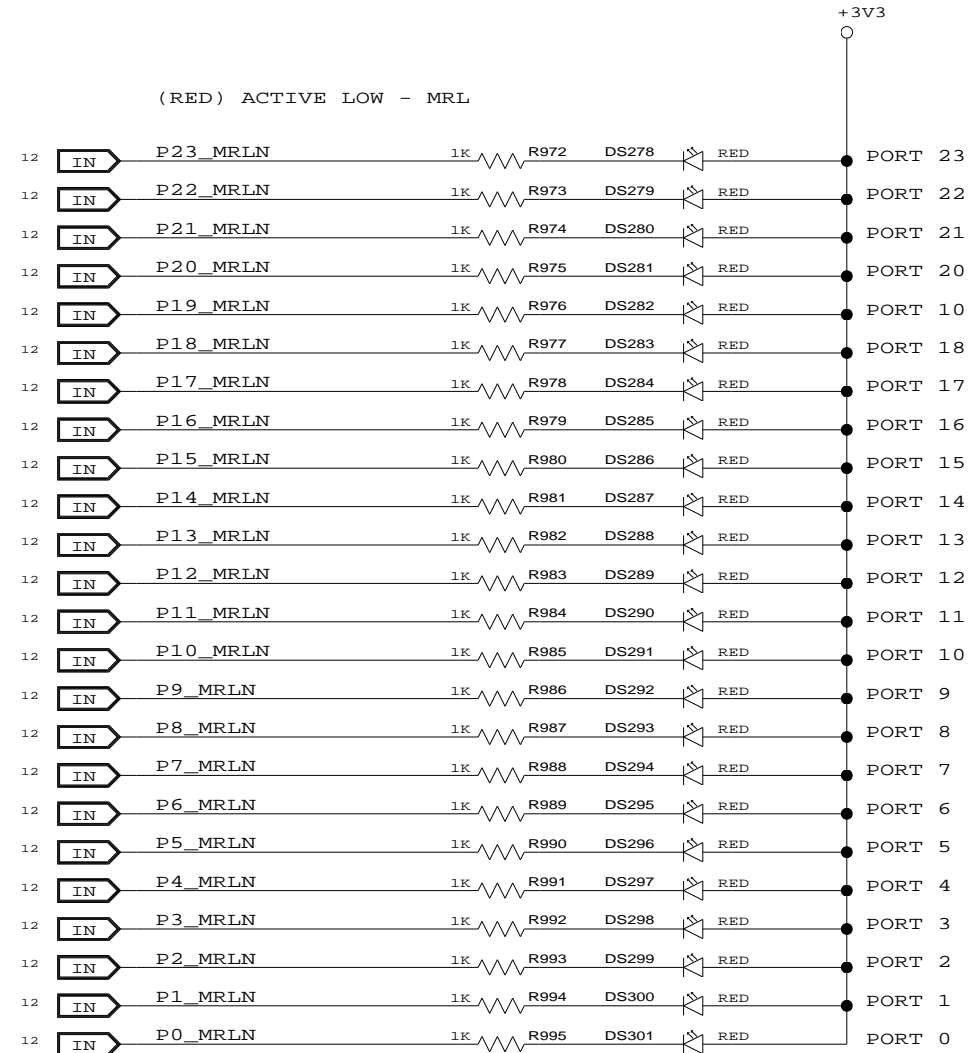
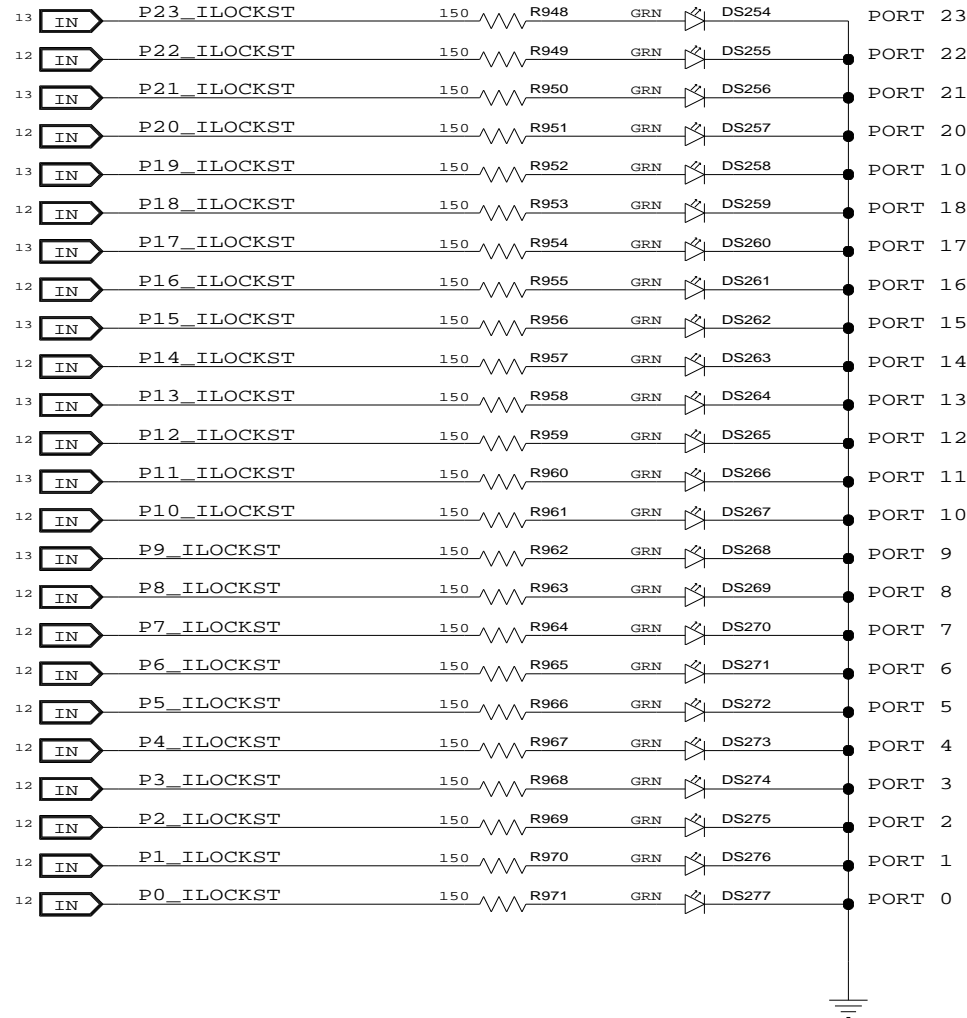
AUTHOR Tony Tran	CHECKED BY Derek Huang
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Thu Jul 01 15:01:03 2010

SHEET 37 OF 52

(GREEN) ACTIVE HIGH - INTERLOCK INPUT

(RED) ACTIVE LOW - MRL



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TITLE EB-LOGAN-23

LED - PORT STATUS (5 OF 7)

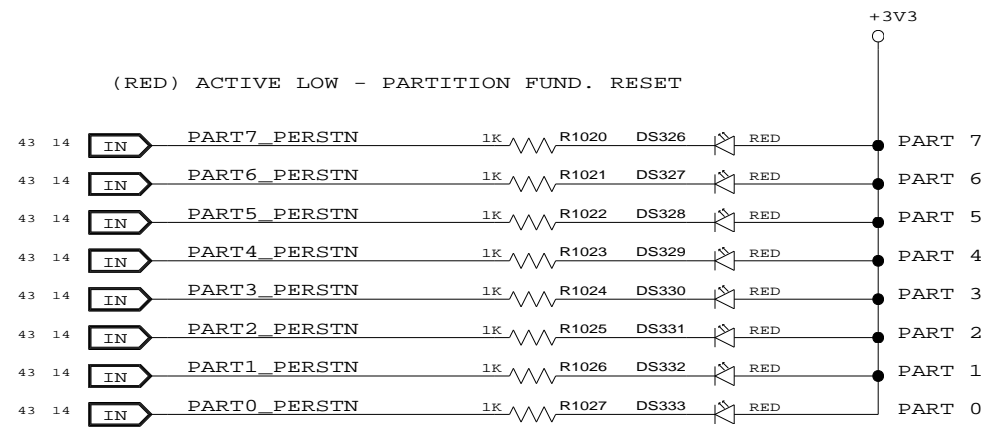
SIZE B	DRAWING NO. SCH-PESEB-001	FAB P/N 18-691-001	REV. 2.0
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AUTHOR Tony Tran	CHECKED BY Derek Huang
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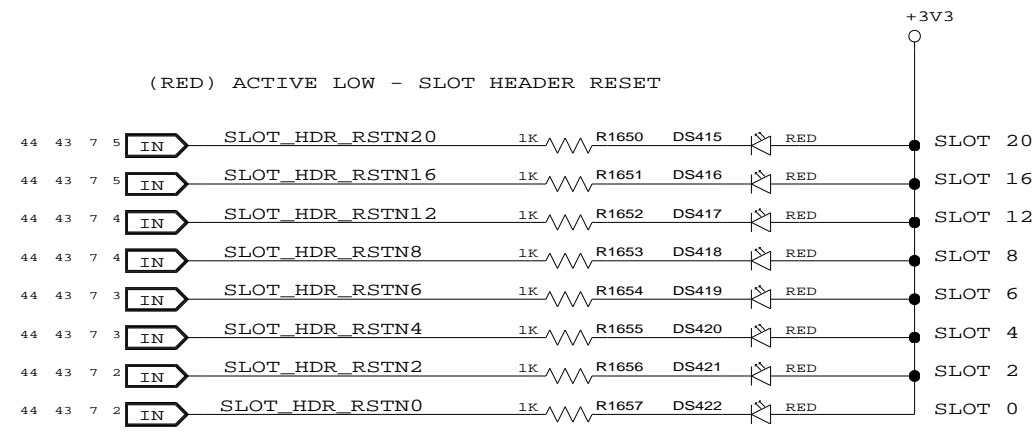
Thu Jul 01 15:01:03 2010

SHEET 38 OF 52

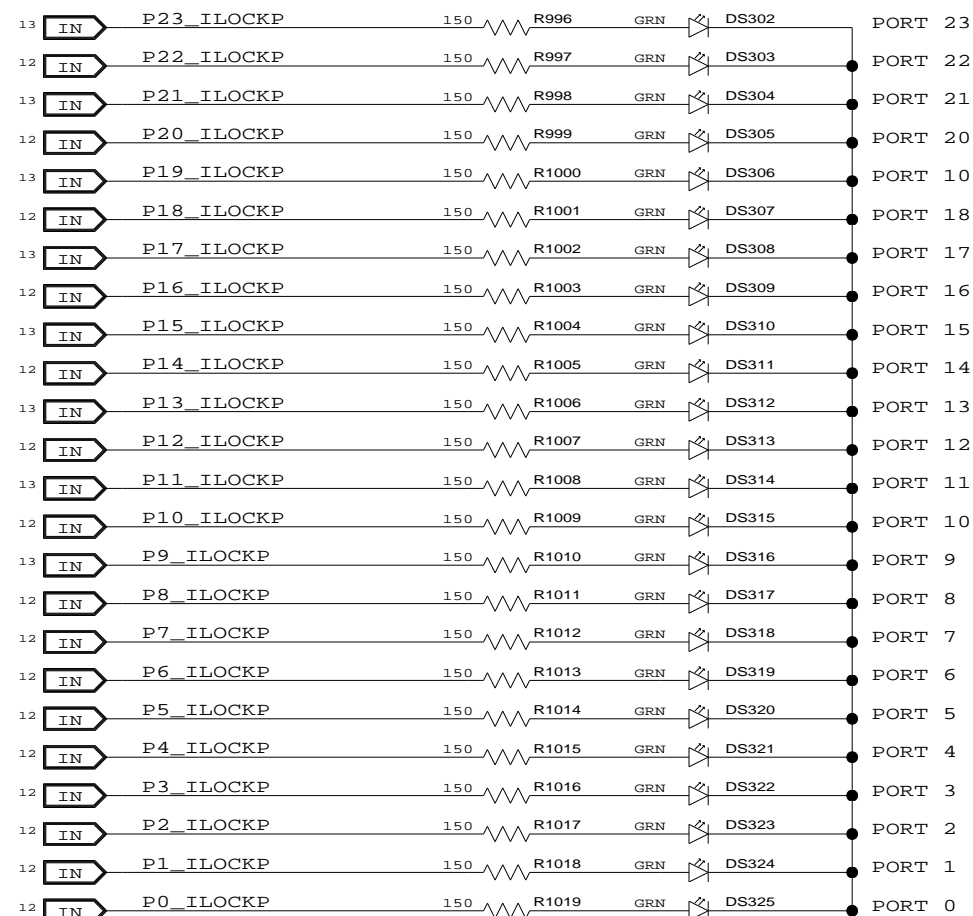
(RED) ACTIVE LOW - PARTITION FUND. RESET



(RED) ACTIVE LOW - SLOT HEADER RESET



(GREEN) ACTIVE HIGH - INTERLOCK OUTPUT



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TITLE EB-LOGAN-23

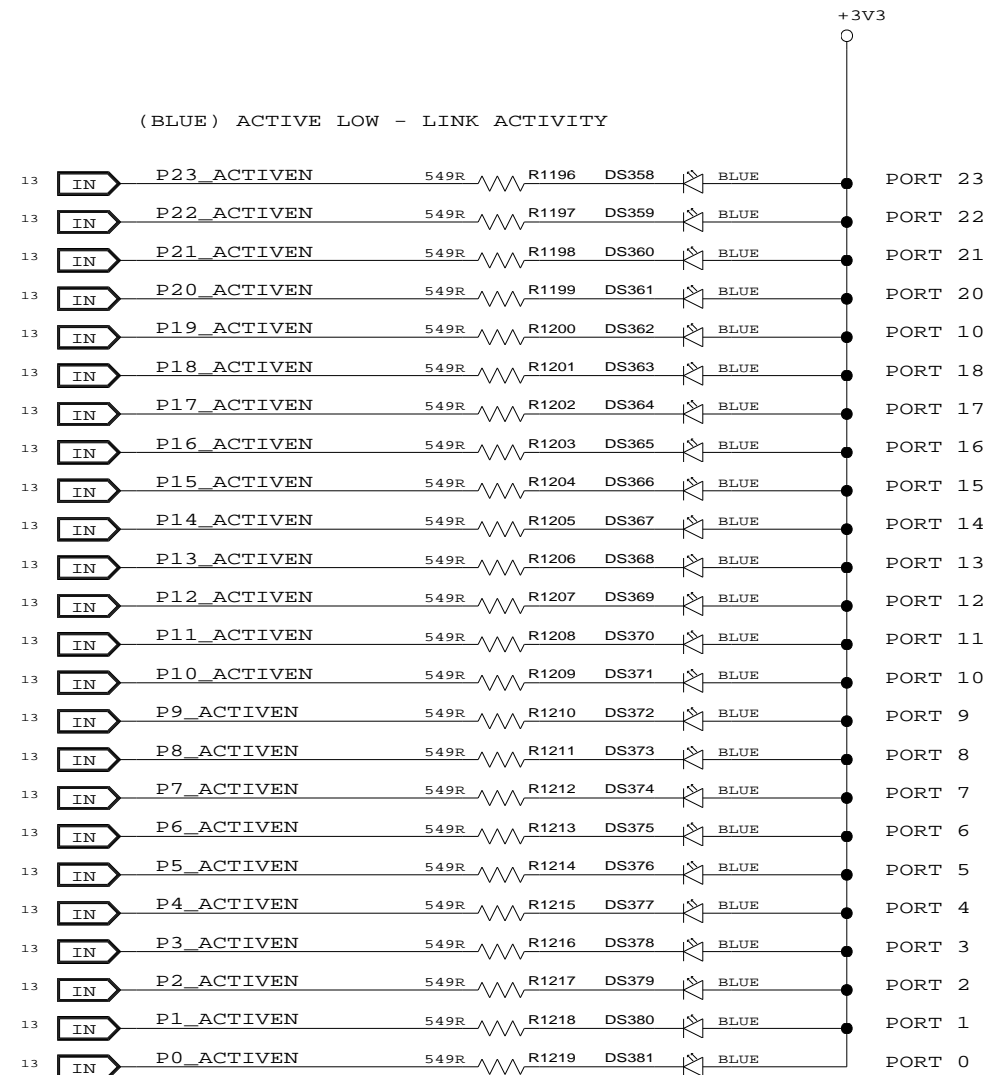
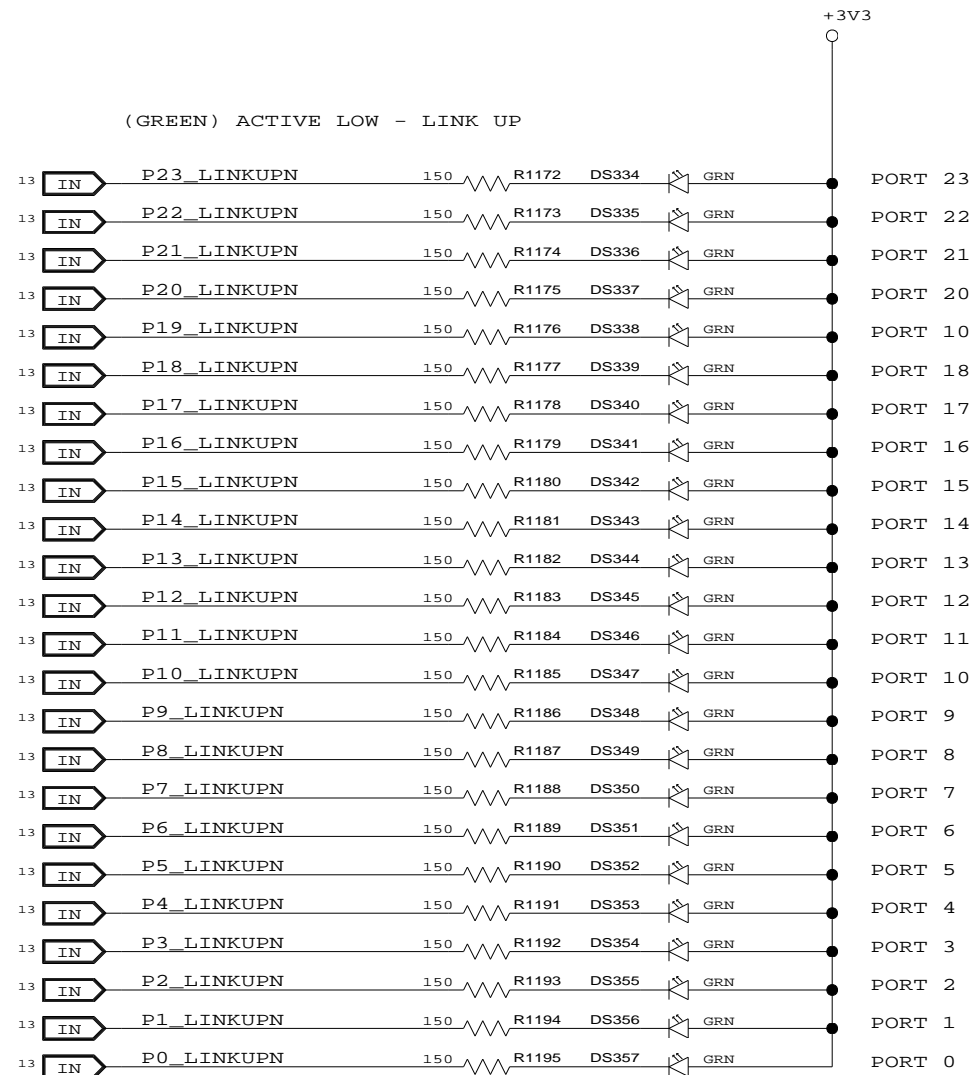
LED - PORT STATUS (6 OF 7)

SIZE B	DRAWING NO. SCH-PESEB-001	FAB P/N 18-691-001	REV. 2.0
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AUTHOR Tony Tran	CHECKED BY Derek Huang
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Thu Jul 01 15:01:03 2010

SHEET 39 OF 52



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TITLE EB-LOGAN-23

LED - PORT STATUS (7 OF 7)

SIZE B	DRAWING NO. SCH-PESEB-001	FAB P/N 18-691-001	REV. 2.0
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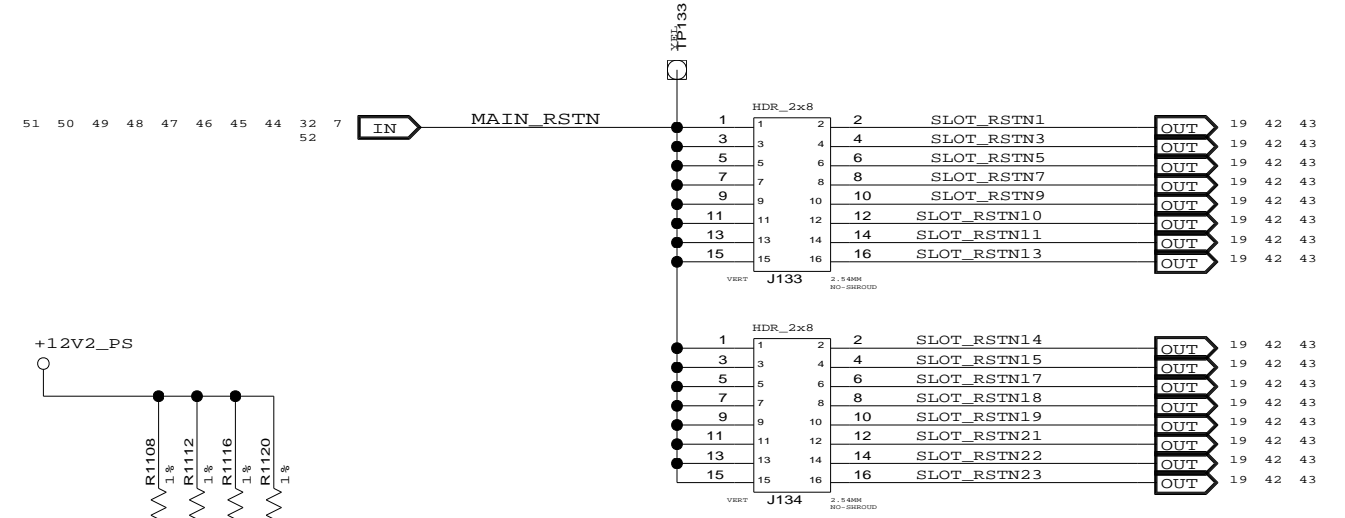
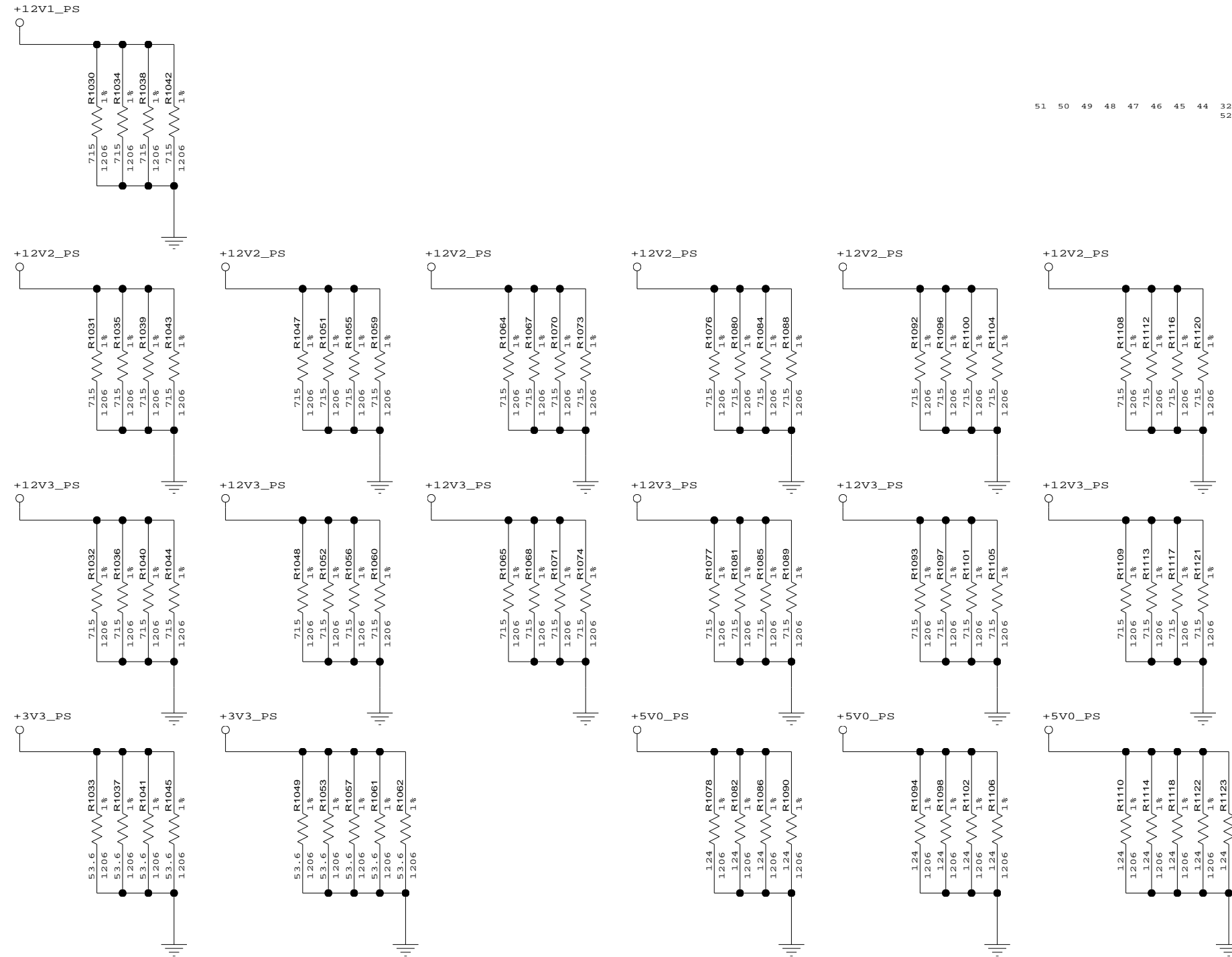
AUTHOR Tony Tran	CHECKED BY Derek Huang
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Thu Jul 01 15:01:04 2010

SHEET 40 OF 52

MINIMUM POWER SUPPLY LOADS

NOTE: DNP JUMPERS WHEN IOEXPANDER IS ENABLED

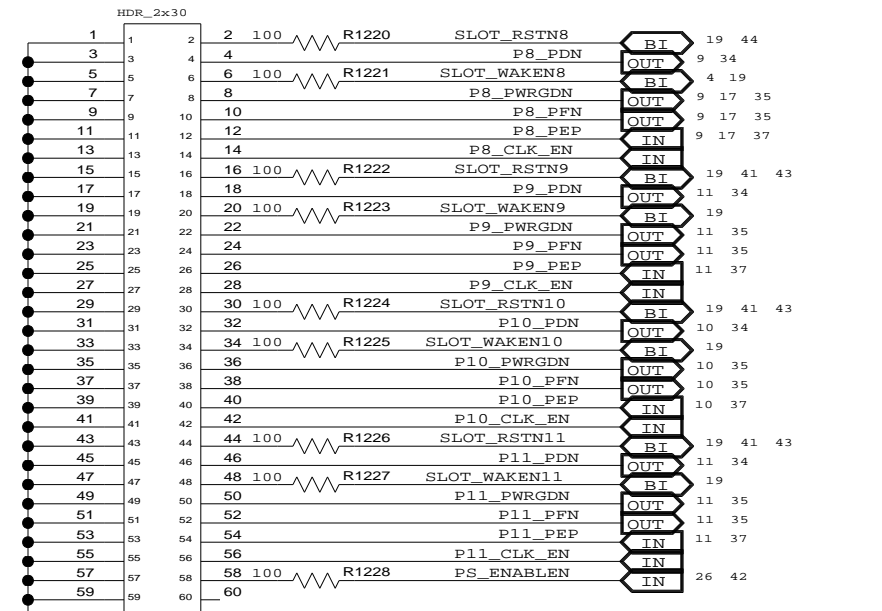


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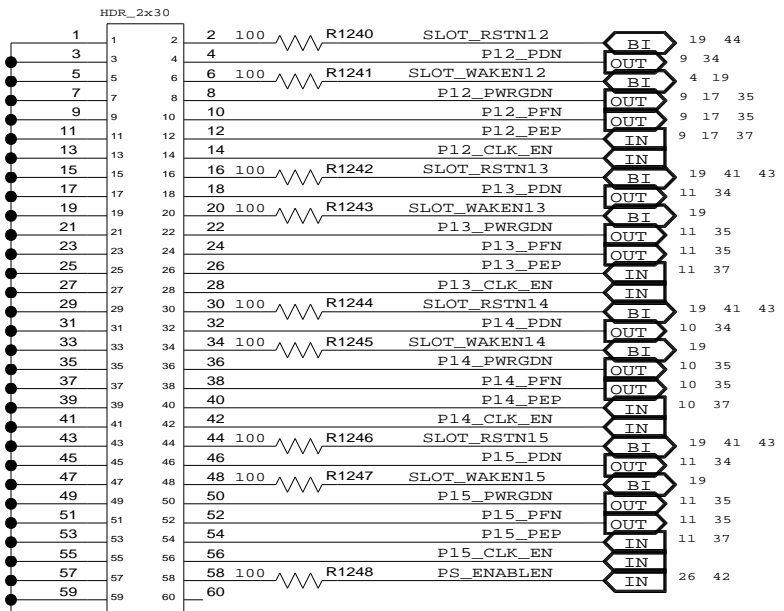
TITLE EB-LOGAN-23			
MIN LOAD RESISTORS			
SIZE B	DRAWING NO. SCH-PESEB-001	FAB P/N 18-691-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jul 01 15:01:04 2010			SHEET 41 OF 52

SLOT_RESETN
CARD_PRESENTN
WAKEN
POWERGOOD
PWR_FLTN
PWR_ENABLE
CLOCK_ENABLEN

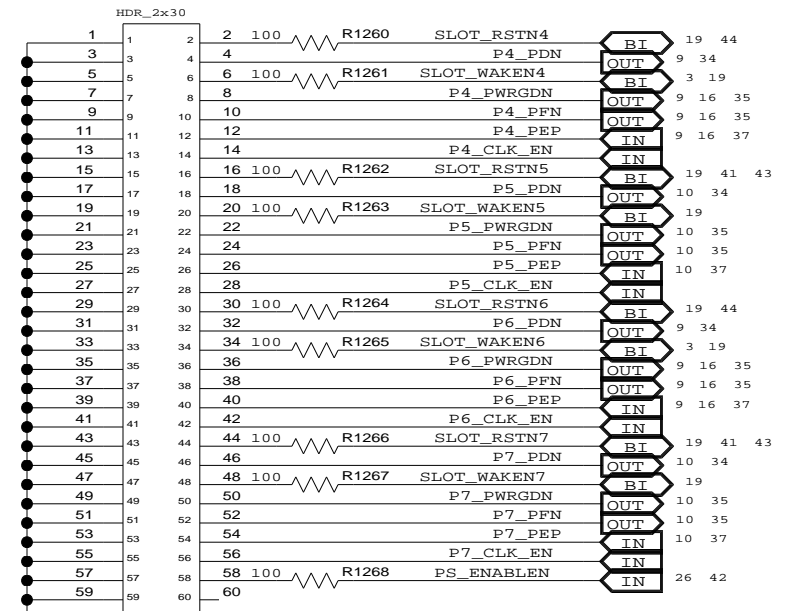
PS_ENABLEN
CABLE SENSE



PORTS 8,9,10,11



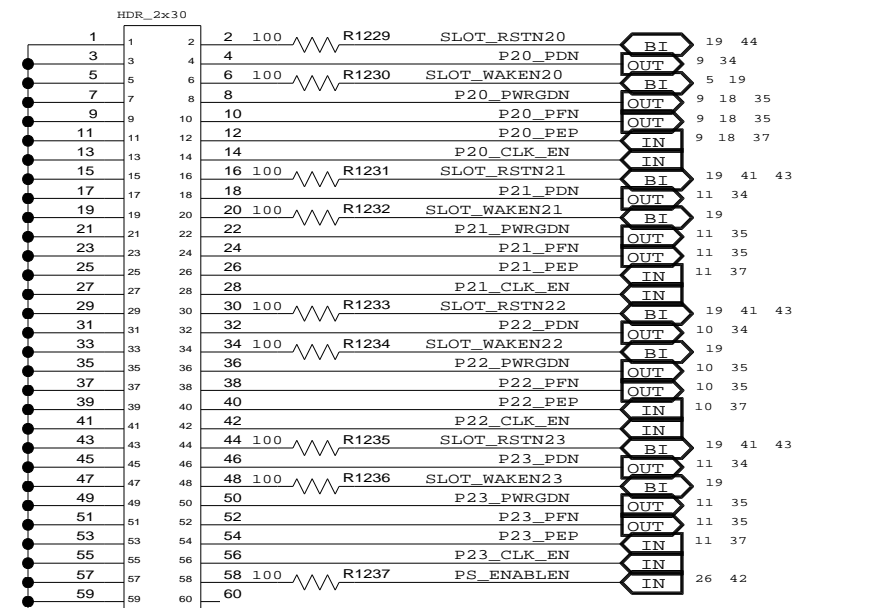
PORTS 12,13,14,15



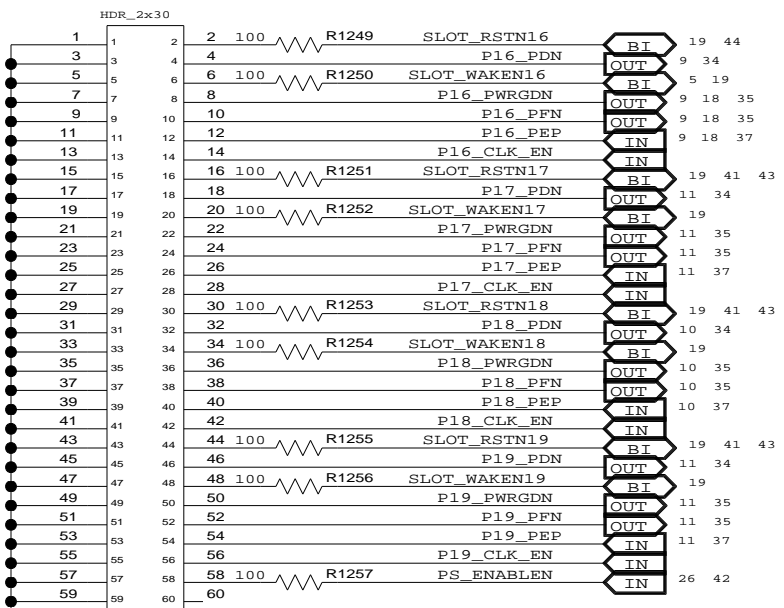
PORTS 4,5,6,7

SLOT_RESETN
CARD_PRESENTN
WAKEN
POWERGOOD
PWR_FLTN
PWR_ENABLE
CLOCK_ENABLEN

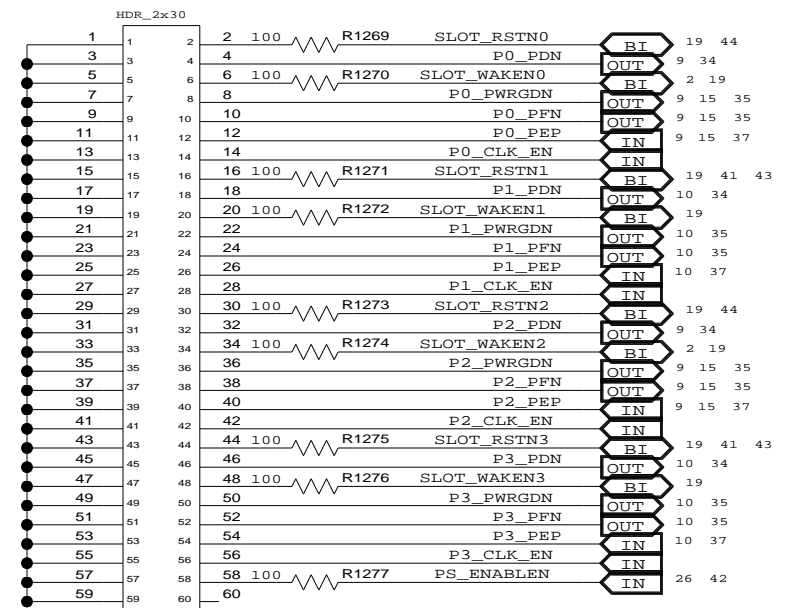
PS_ENABLEN
CABLE SENSE

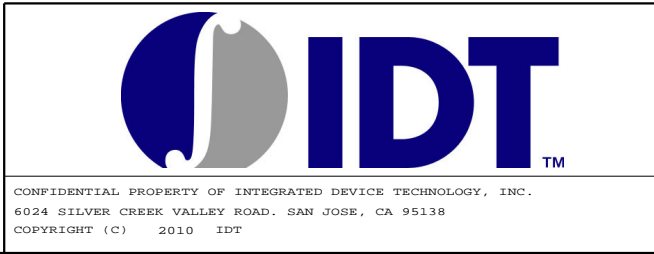
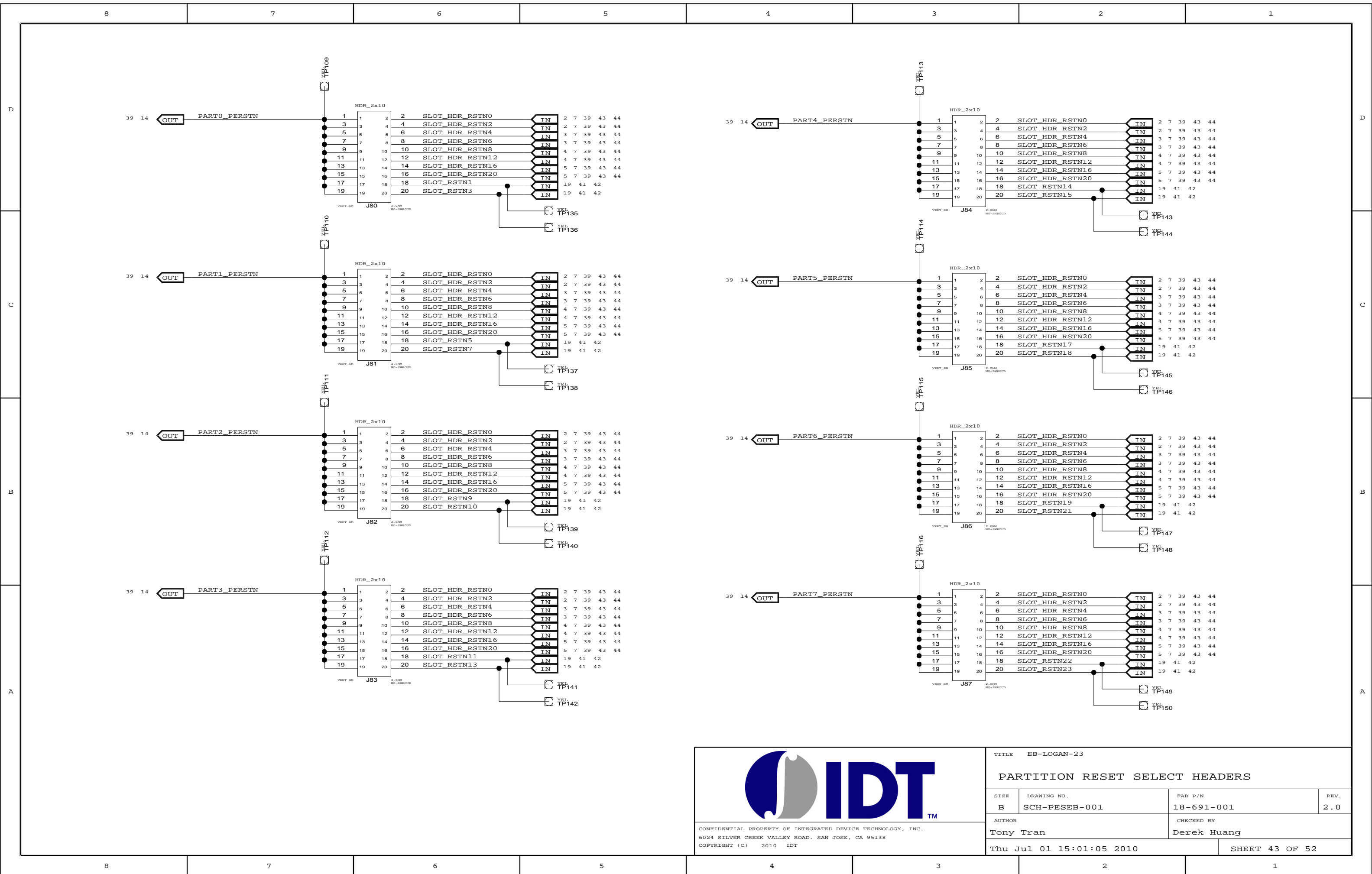


PORTS 20,21,22,23

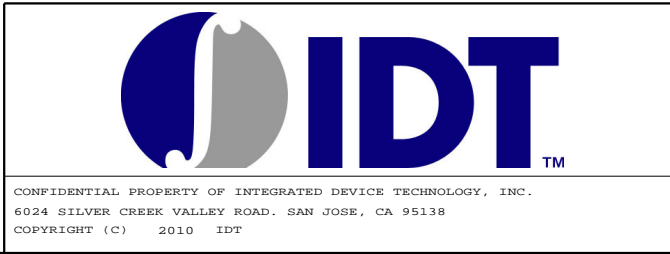
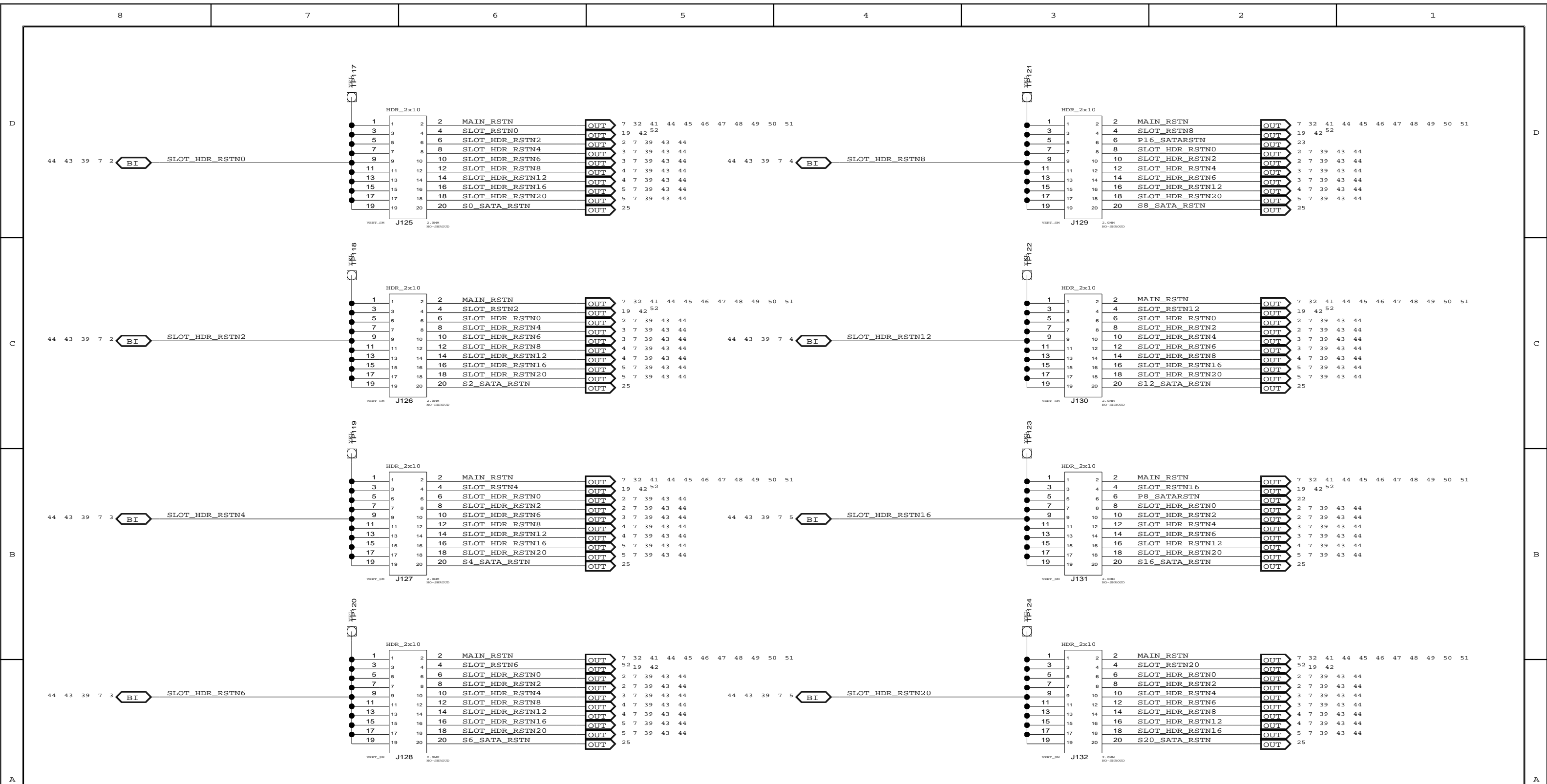


PORTS 16,17,18,19

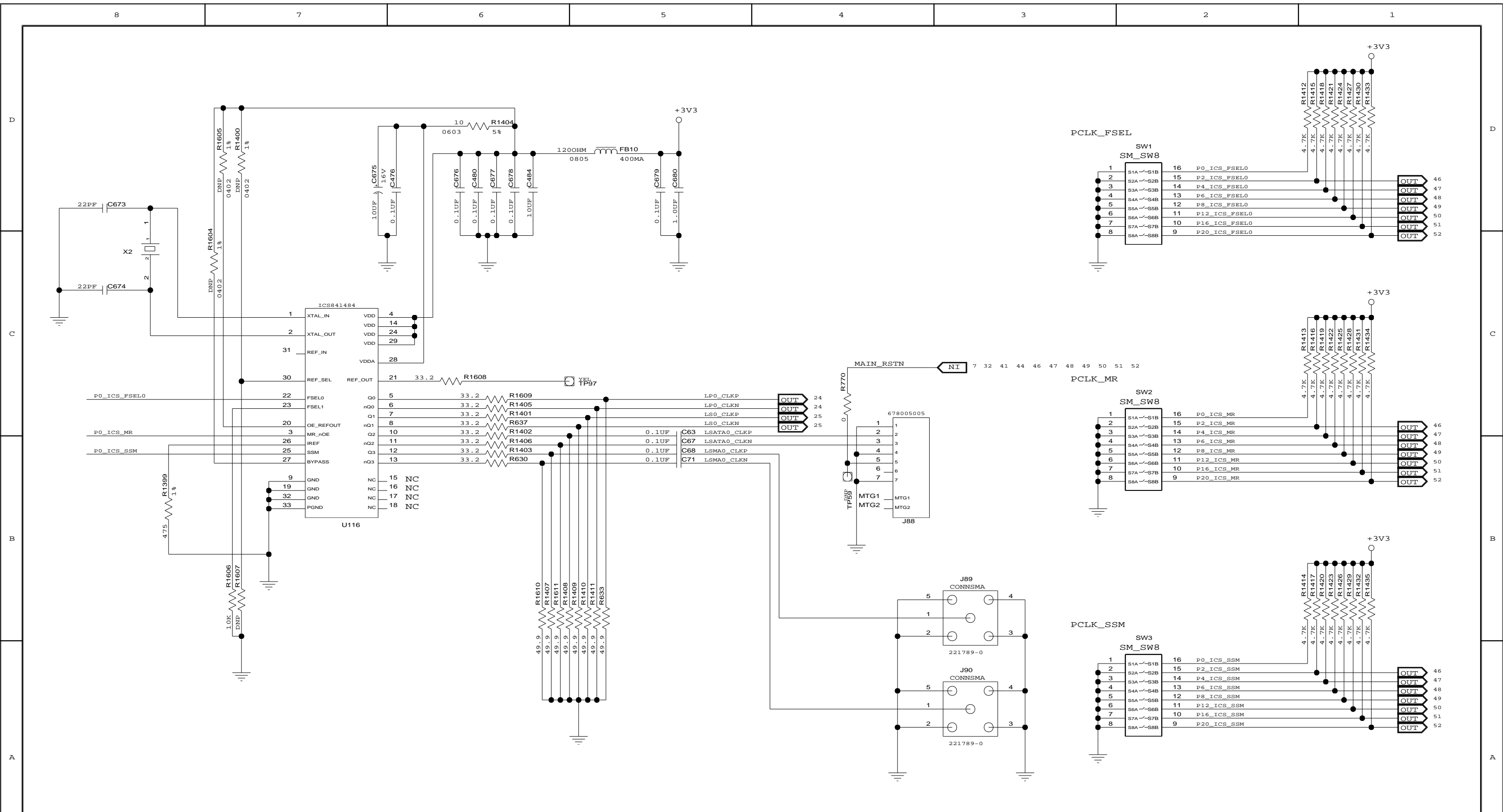





TITLE EB-LOGAN-23			
PARTITION RESET SELECT HEADERS			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:01:05 2010			SHEET 43 OF 52



TITLE EB-LOGAN-23			
SLOT RESET SELECT HEADERS			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:01:05 2010			SHEET 44 OF 52



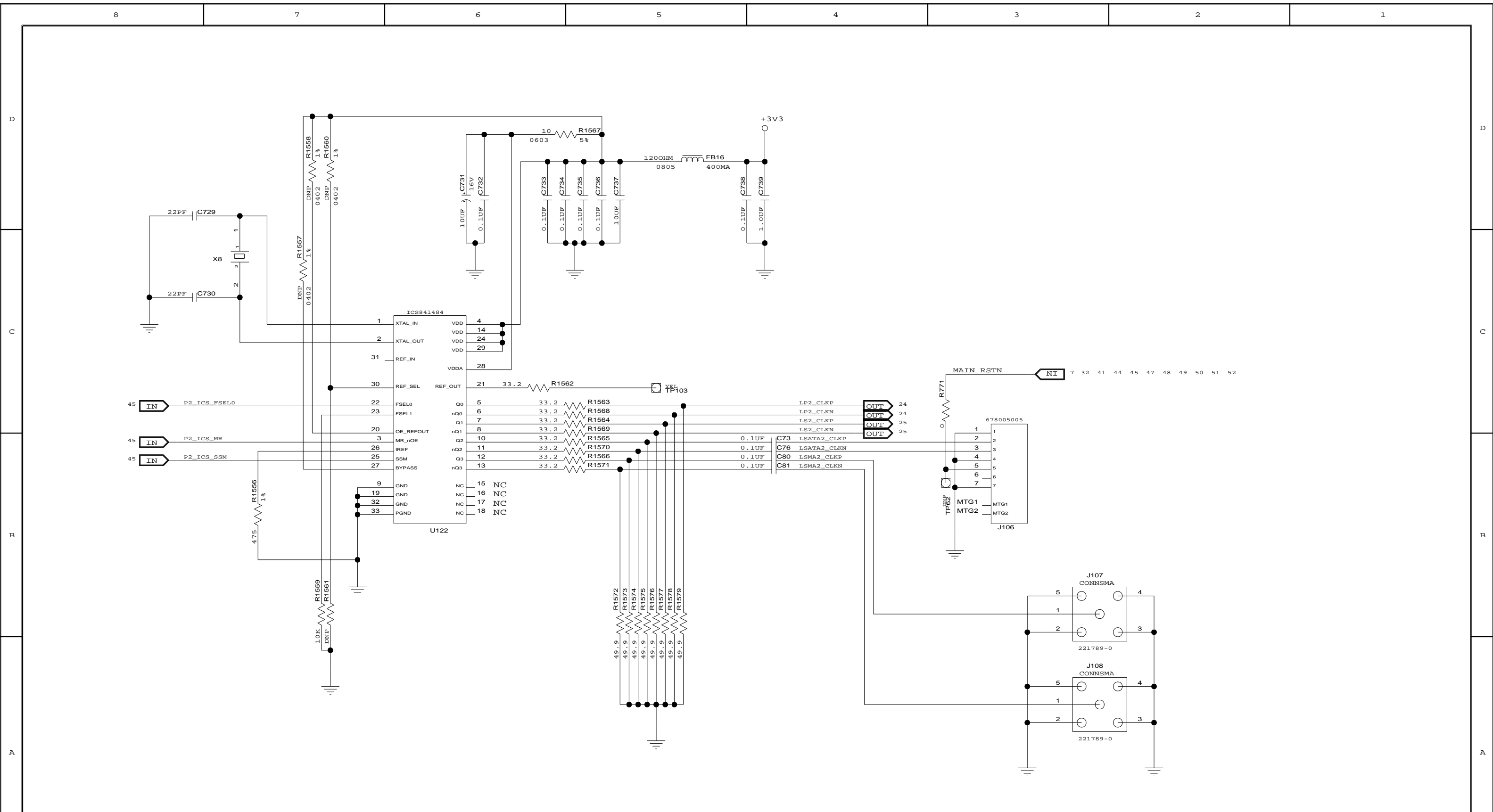



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TITLE EB-LOGAN-23

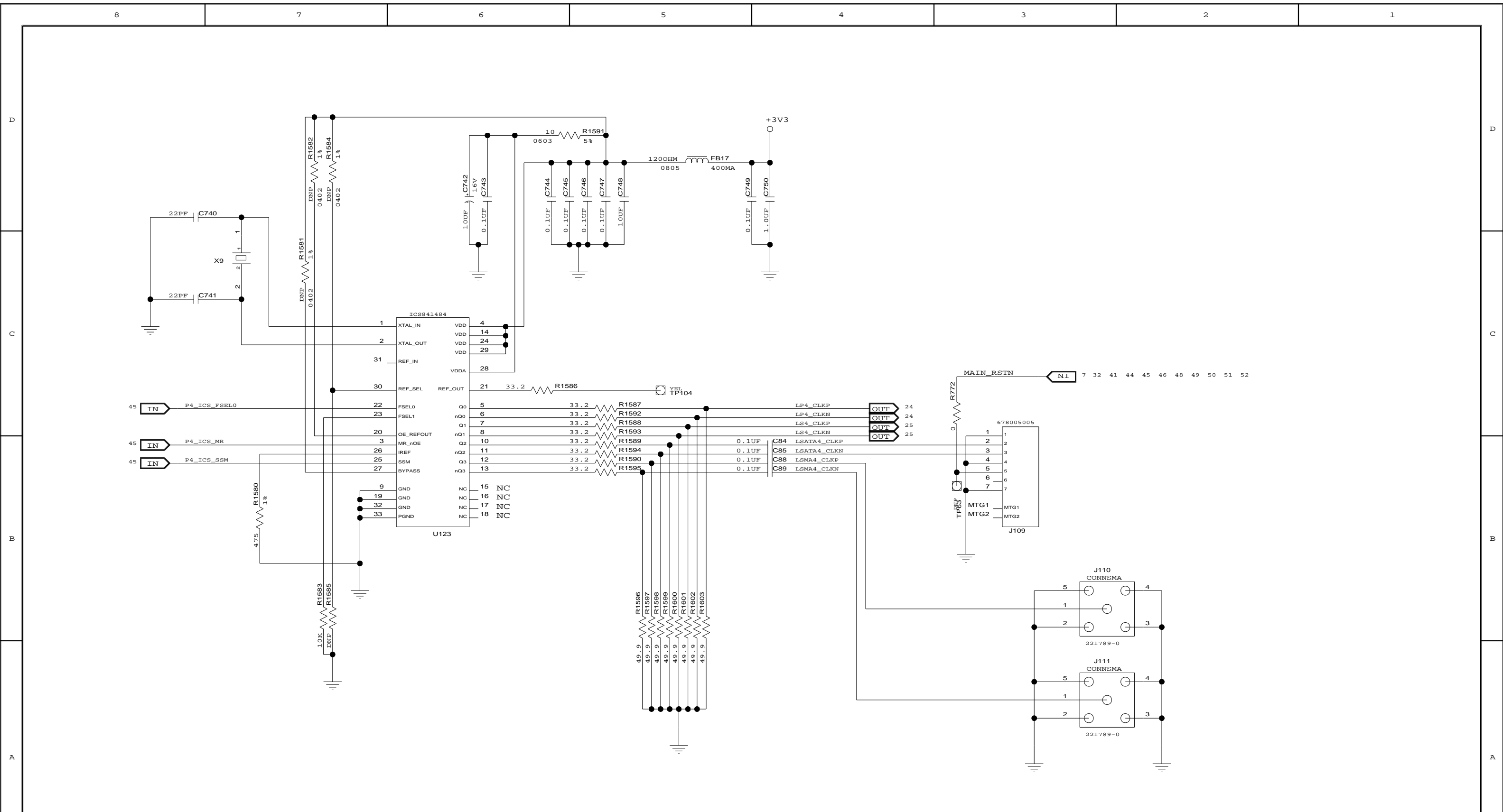
PORT 0 CLOCK GENERATOR


SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jul 01 15:01:05 2010			SHEET 45 OF 52



		TITLE EB-LOGAN-23		
		PORT 2 CLOCK GENERATOR		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	SCH-PESEB-001	18-691-001	2.0	
AUTHOR		CHECKED BY		
Tony Tran		Derek Huang		
Thu Jul 01 15:01:06 2010			SHEET 46 OF 52	

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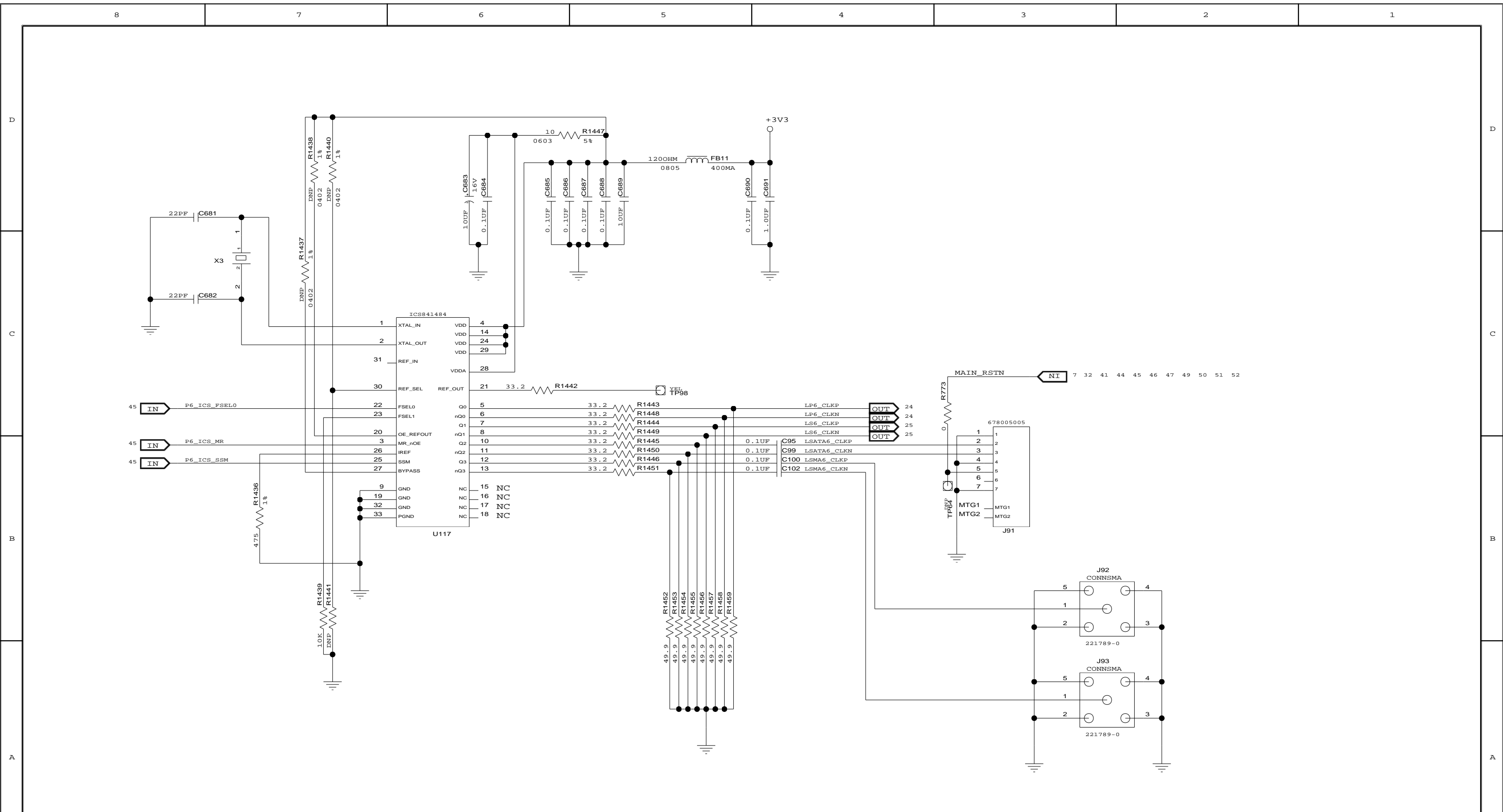



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TITLE EB-LOGAN-23

PORT 4 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:01:06 2010			SHEET 47 OF 52



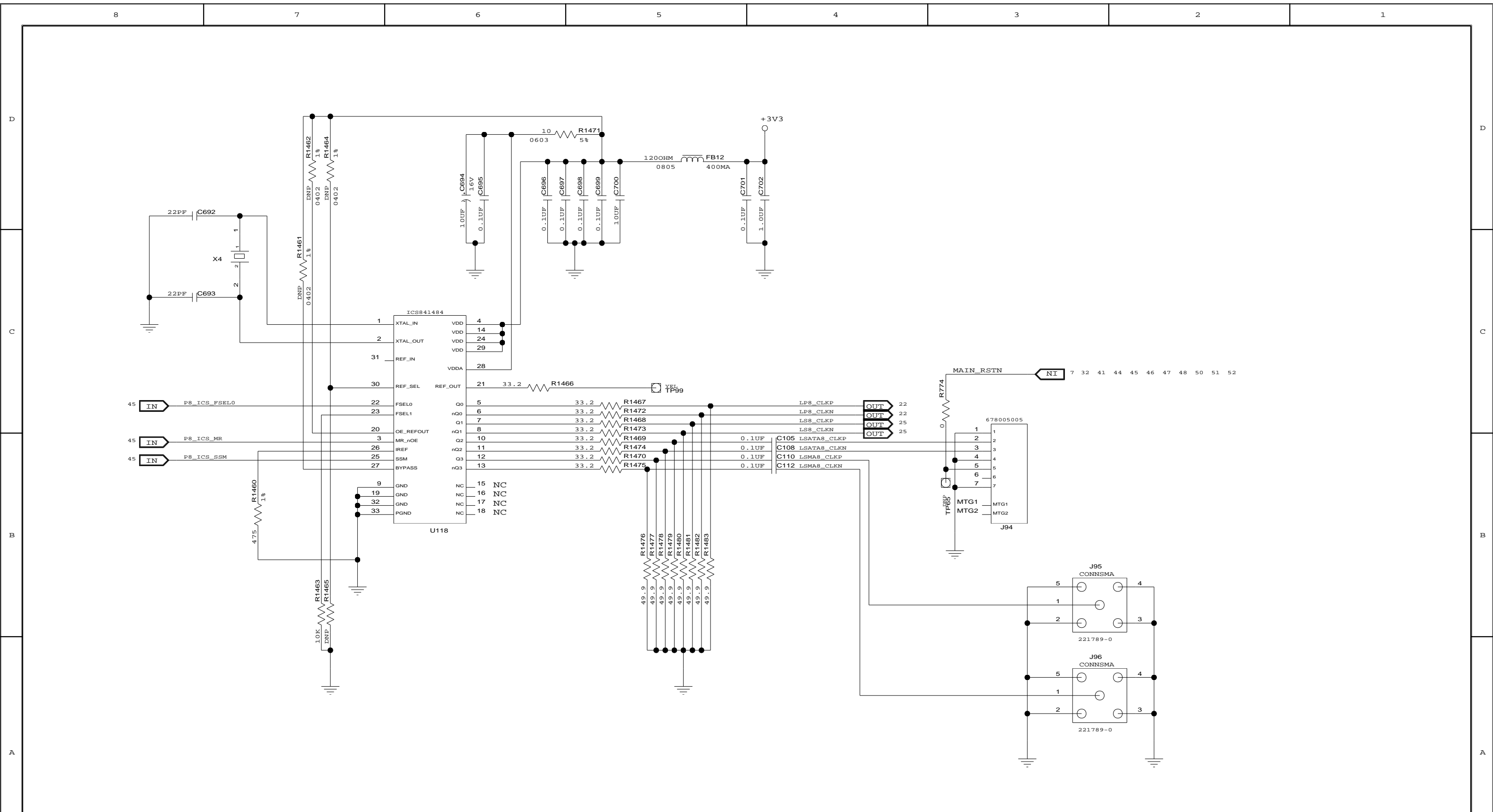



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TITLE EB-LOGAN-23

PORT 6 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:01:06 2010			SHEET 48 OF 52



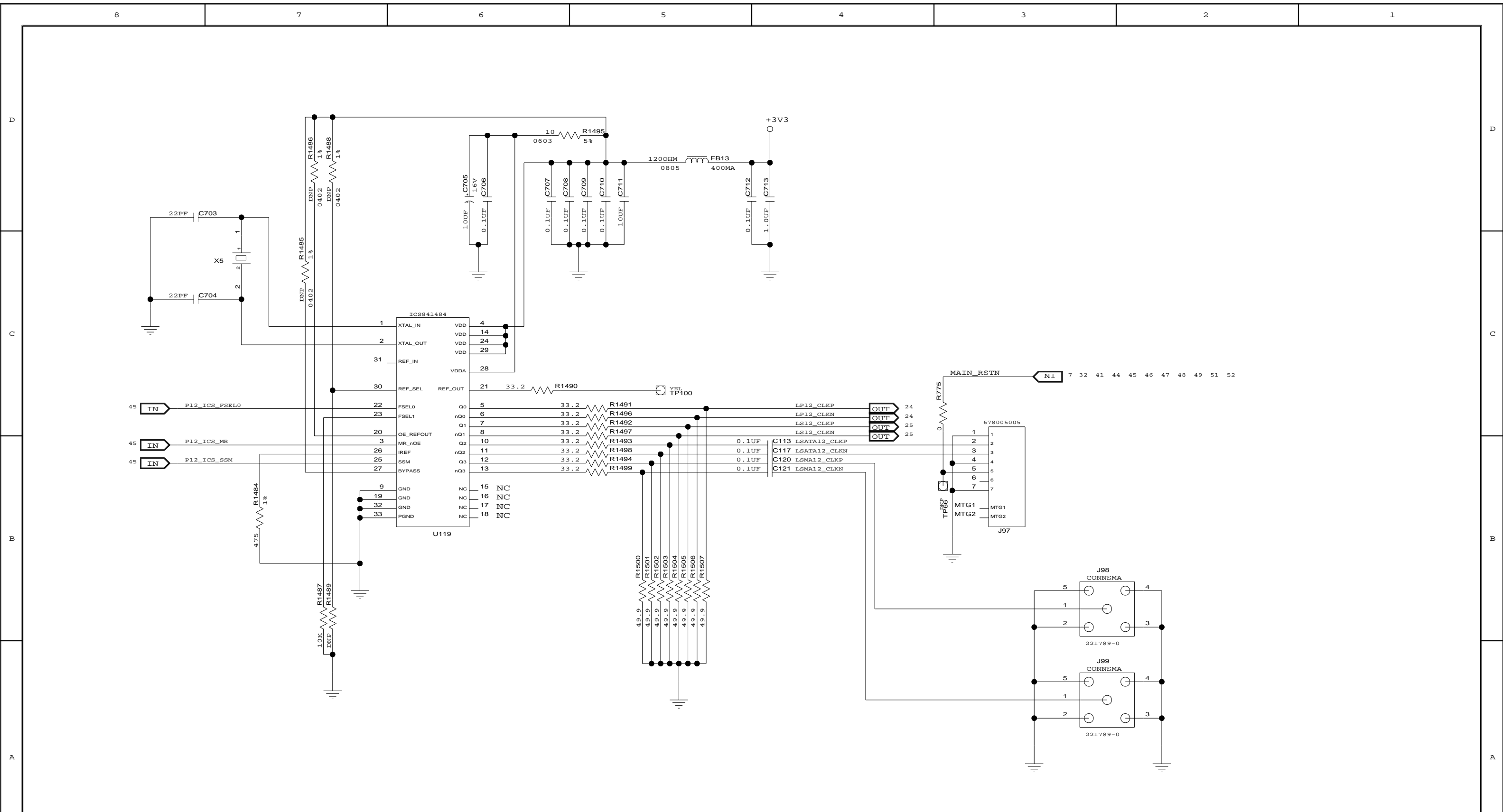



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TITLE EB-LOGAN-23

PORT 8 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:01:06 2010			SHEET 49 OF 52



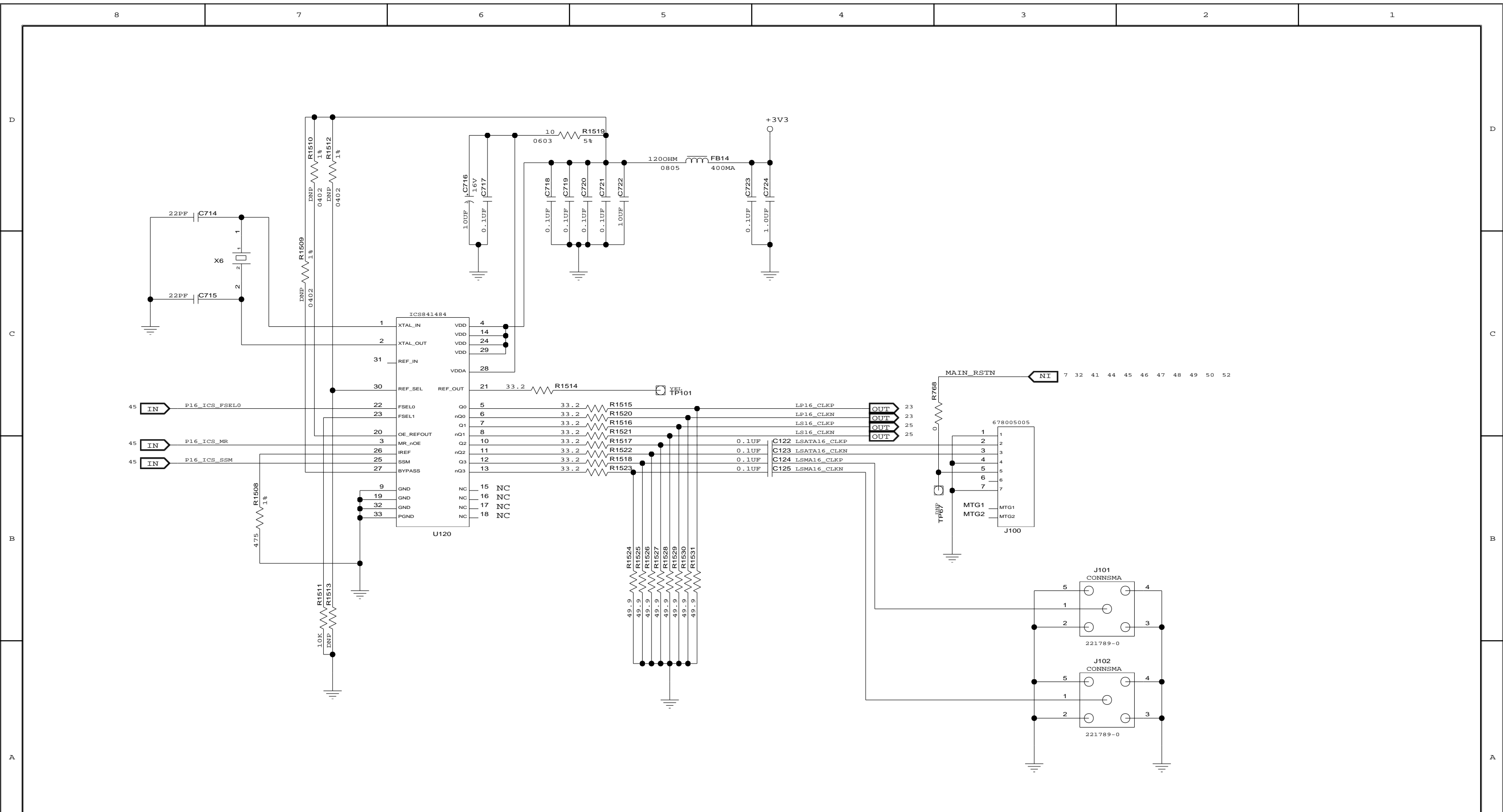



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TITLE EB-LOGAN-23

PORT 12 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:01:07 2010			SHEET 50 OF 52



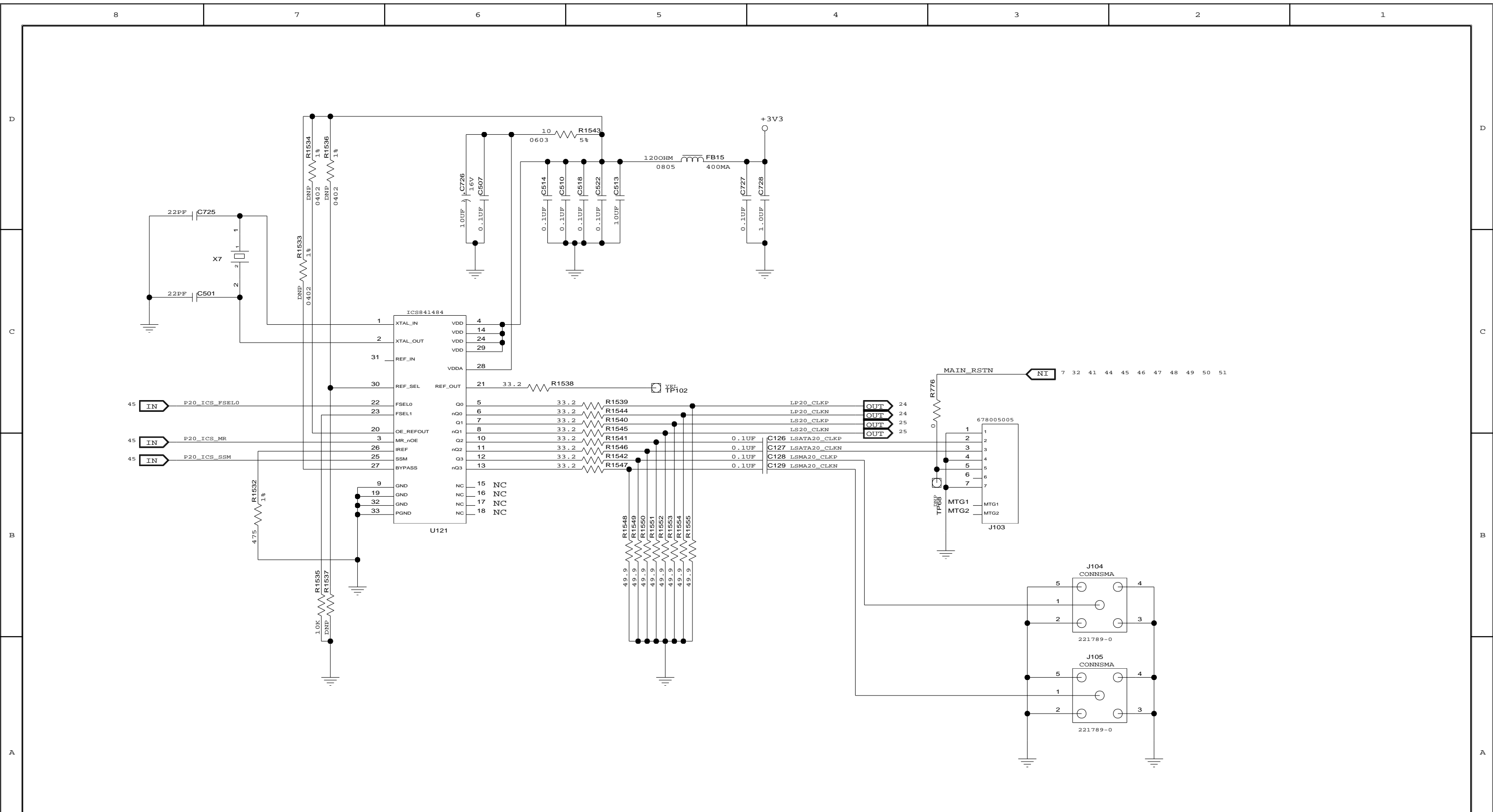



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TITLE EB-LOGAN-23

PORT 16 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jul 01 15:01:07 2010			SHEET 51 OF 52





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TITLE EB-LOGAN-23

PORT 20 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-001	18-691-001	2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jul 01 15:01:07 2010			SHEET 52 OF 52