

REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
	1.0	INITIAL RELEASE	2009-12-05	T. TRAN

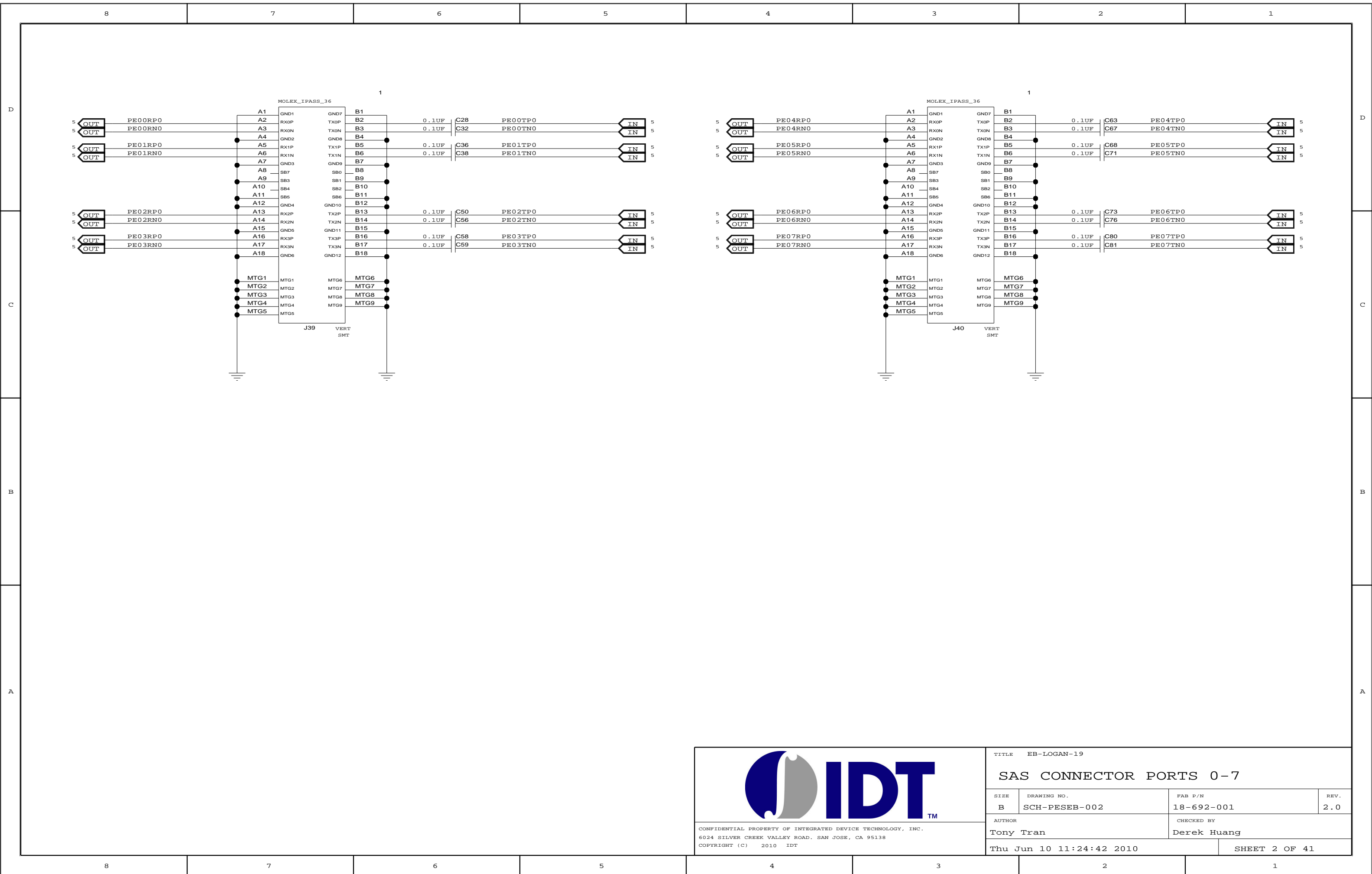
1. TITLE PAGE / TABLE OF CONTENTS


- | | |
|---------------------------------------|--|
| 2. SAS CONNECTOR PORTS 0-7 | 22. POWER CONNECTORS, MIN LOAD RESISTORS |
| 3. MEZZANINE CONNECTOR PORTS 8, 12 | 23. POWER REGULATOR - VDDIO |
| 4. MEZZANINE CONNECTOR PORTS 16, 20 | 24. POWER REGULATOR - VDDCORE |
| 5. 24NT24G2 - SERDES | 25. POWER REGULATOR - VDDPEA |
| 6. 24NT24G2 - CLK, CONFIG, GPIO | 26. POWER REGULATOR - VDDPEHA |
| 7. 24NT24G2 - POWER, GND | 27. POWER REGULATOR - VDDPETA |
| 8. IOEXPANDER 0-3 | 28. RESET, SMBUS, EEPROM, JTAG |
| 9. IOEXPANDER 4-7 | 29. DIP SWITCHES |
| 10. IOEXPANDER 8-11 | 30. LED - PORT STATUS (1 OF 7) |
| 11. IOEXPANDER 12-13 | 31. LED - PORT STATUS (2 OF 7) |
| 12. IOEXPANDER 16-19 | 32. LED - PORT STATUS (3 OF 7) |
| 13. IOEXPANDER 20-21 | 33. LED - PORT STATUS (4 OF 7) |
| 14. HOT PLUG CONTROL PORTS 8-12 | 34. LED - PORT STATUS (5 OF 7) |
| 15. HOT PLUG CONTROL PORTS 16-20 | 35. LED - PORT STATUS (6 OF 7) |
| 16. SLOT RESETS AND WAKE PULL-UPS | 36. LED - PORT STATUS (7 OF 7) |
| 17. CLOCK | 37. 12PK RIBBON CONNECTORS |
| 18. CLOCK BUFFER | 38. PARTITION RESET SELECT HEADERS |
| 19. CLOCK SELECTOR - DUT PCLK 8 | 39. SLOT RESET SELECT HEADERS |
| 20. CLOCK SELECTOR - DUT PCLK 16 | 40. PORT 8 CLOCK GENERATOR |
| 21. CLOCK SELECTOR - SLOTS 0-20, GCLK | 41. PORT 16 CLOCK GENERATOR |



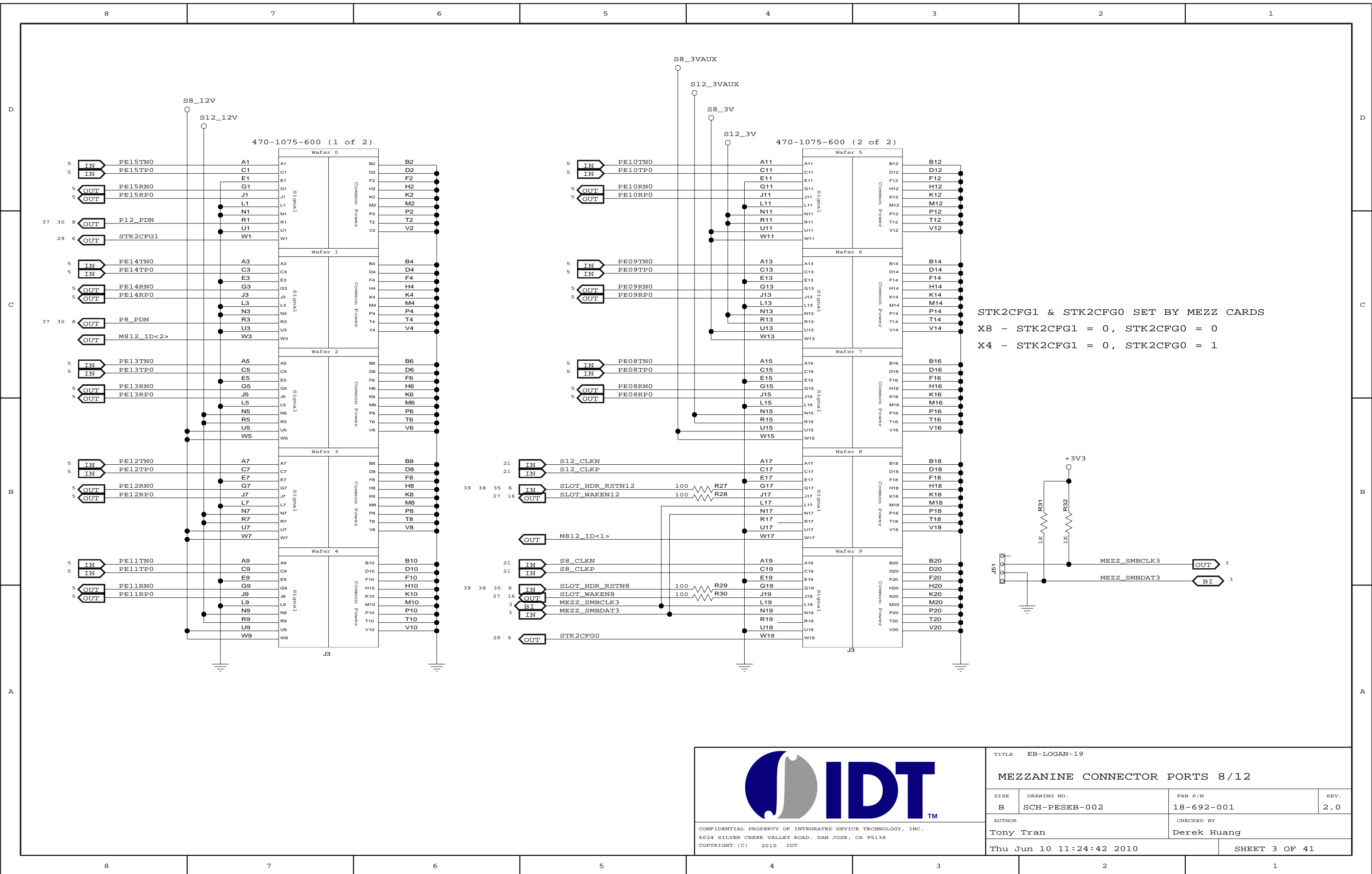
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TITLE EB-LOGAN-19			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:42 2010			SHEET 1 OF 41



		TITLE EB-LOGAN-19		
		SAS CONNECTOR PORTS 0-7		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	SCH-PESEB-002	18-692-001	2.0	
AUTHOR		CHECKED BY		
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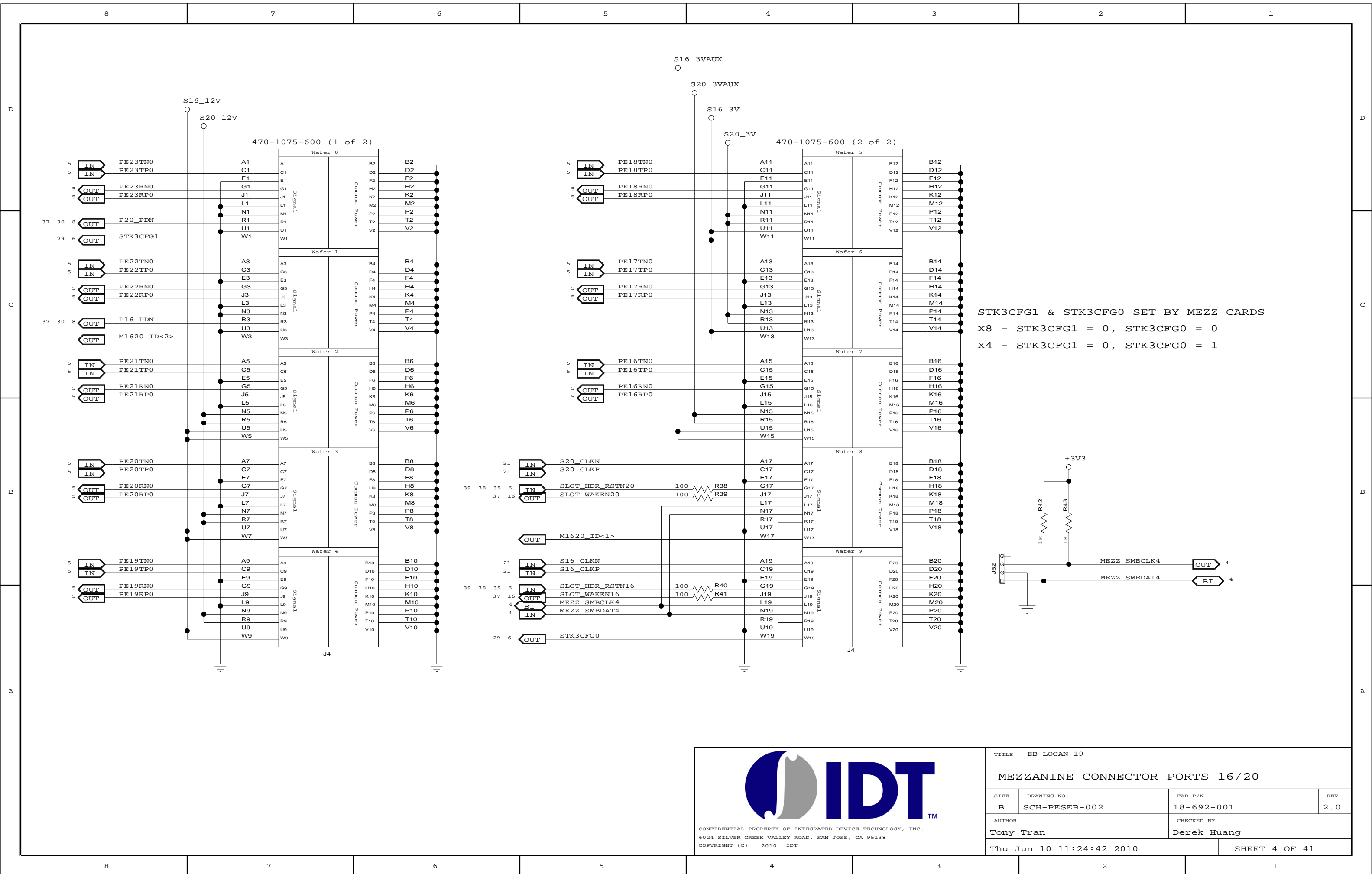


STK2CFG1 & STK2CFG0 SET BY MEZZ CARDS
 X8 - STK2CFG1 = 0, STK2CFG0 = 0
 X4 - STK2CFG1 = 0, STK2CFG0 = 1



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TITLE EB-LOGAN-19			
MEZZANINE CONNECTOR PORTS 8/12			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:42 2010			SHEET 3 OF 41

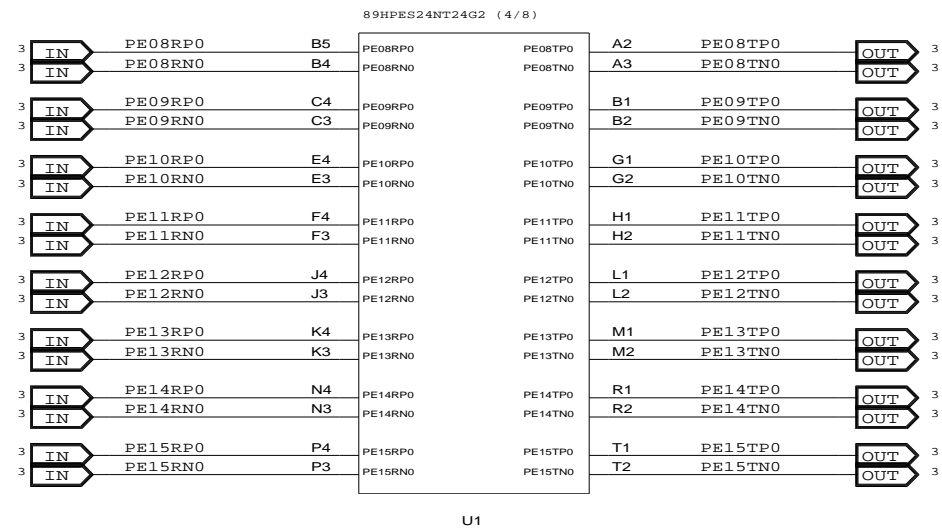
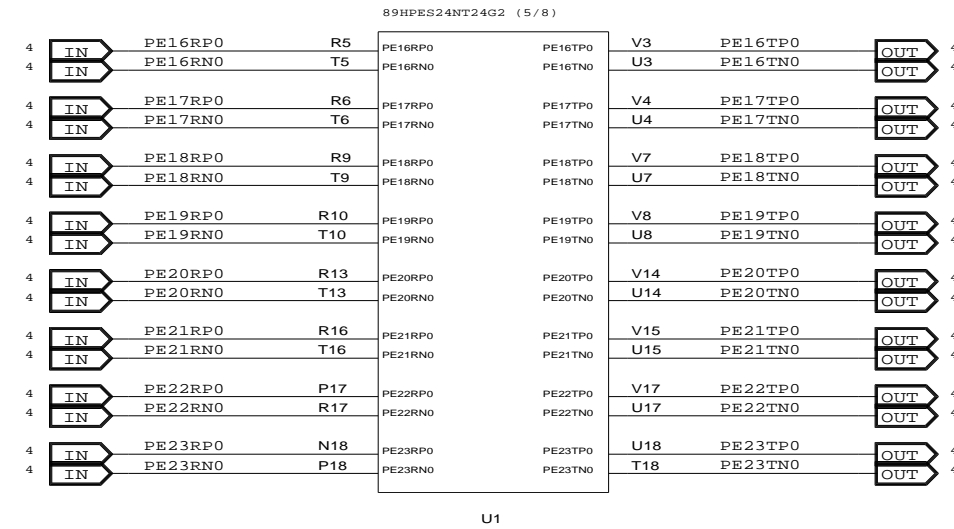
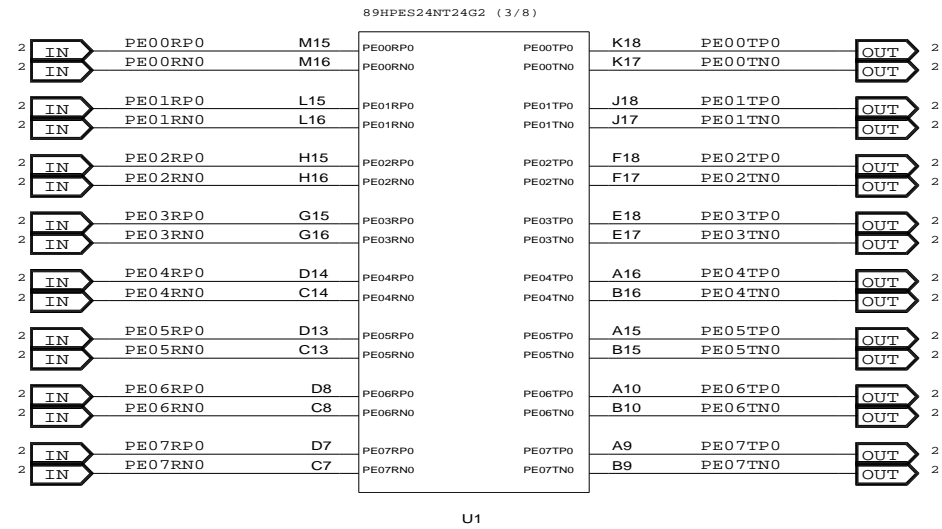



STK3CFG1 & STK3CFG0 SET BY MEZZ CARDS
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 X4 - STK3CFG1 = 0, STK3CFG0 = 1



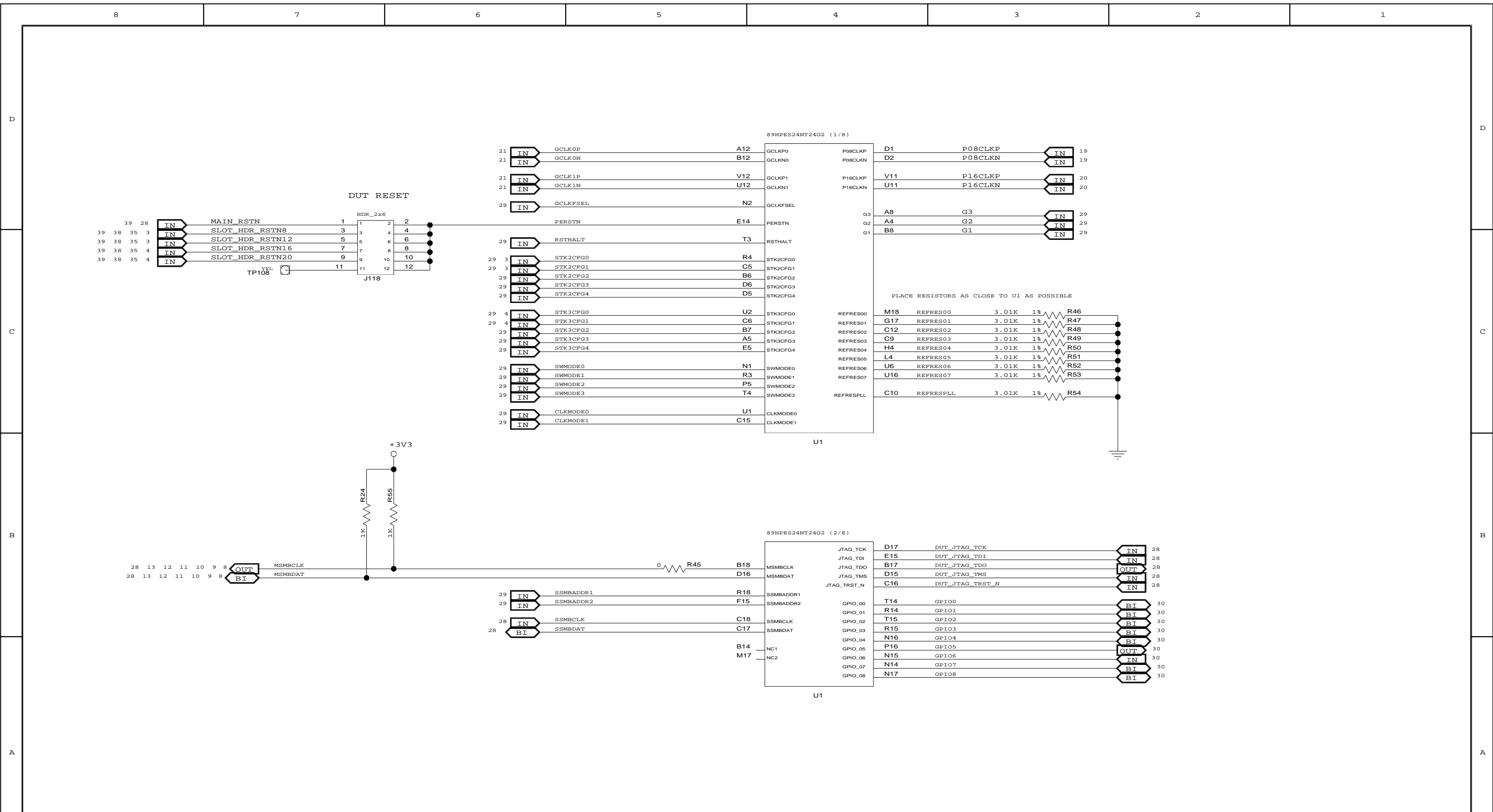
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TITLE EB-LOGAN-19			
MEZZANINE CONNECTOR PORTS 16/20			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:42 2010			SHEET 4 OF 41



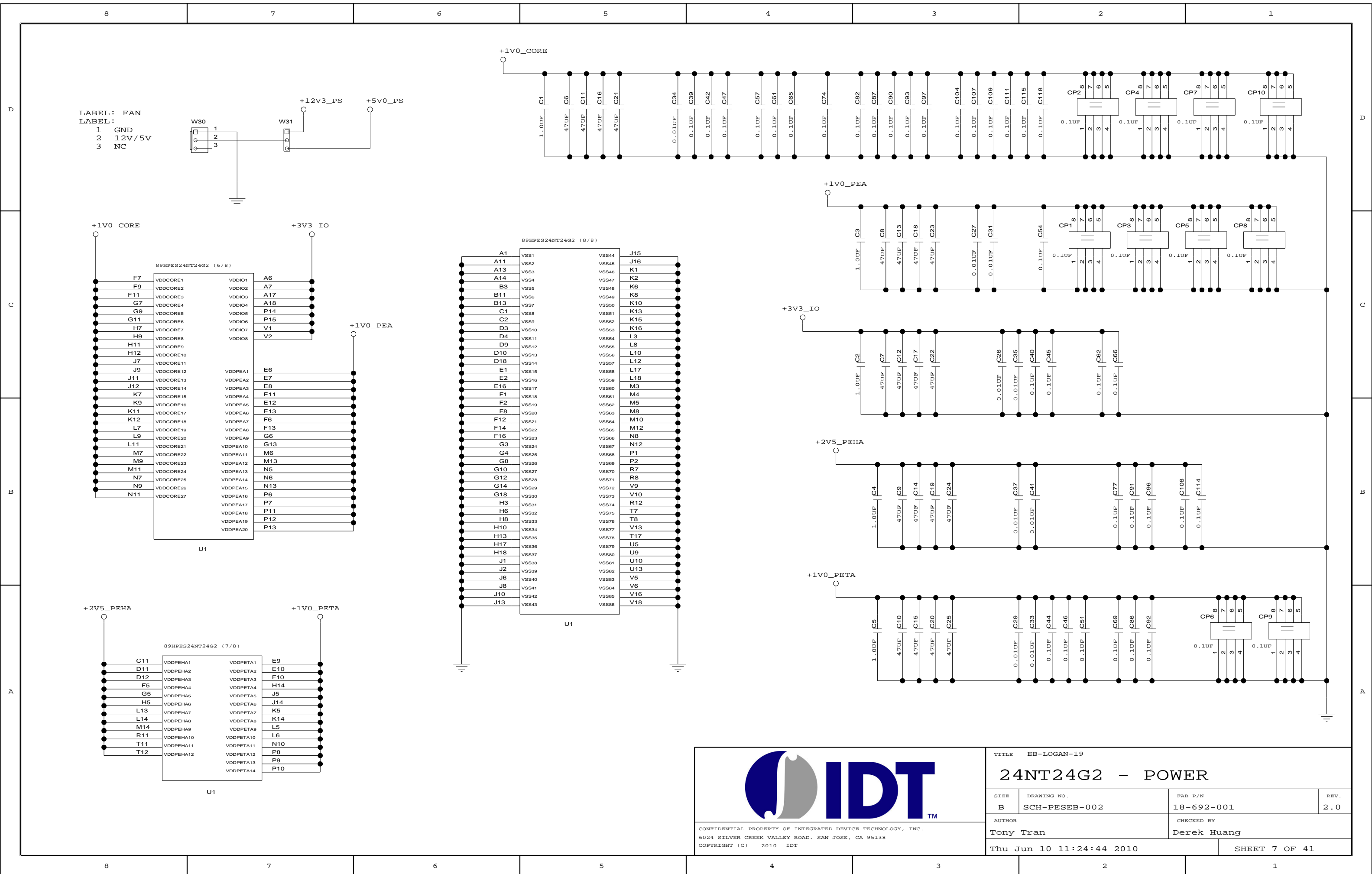
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SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
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Thu Jun 10 11:24:43 2010			SHEET 5 OF 41

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		TITLE EB-LOGAN-19		
		24NT24G2 - CLK, CONFIG, GPIO		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	SCH-PESEB-002	18-692-001	2.0	
AUTHOR		CHECKED BY		
Tony Tran		Derek Huang		
Thu Jun 10 11:24:43 2010			SHEET 6 OF 41	

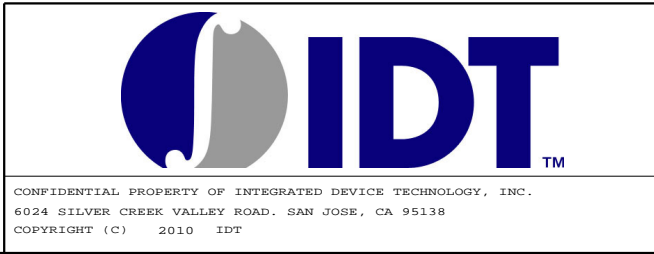
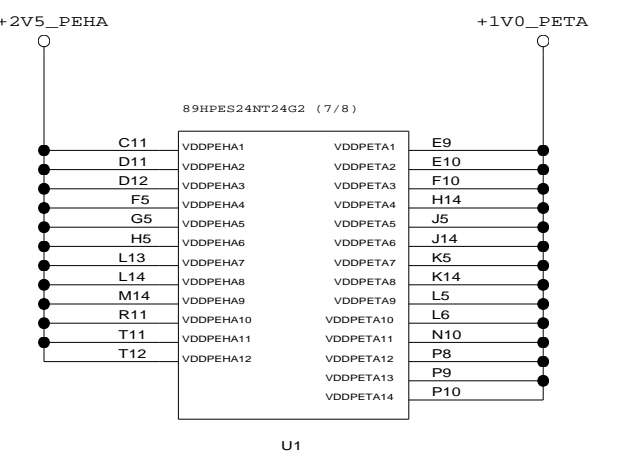
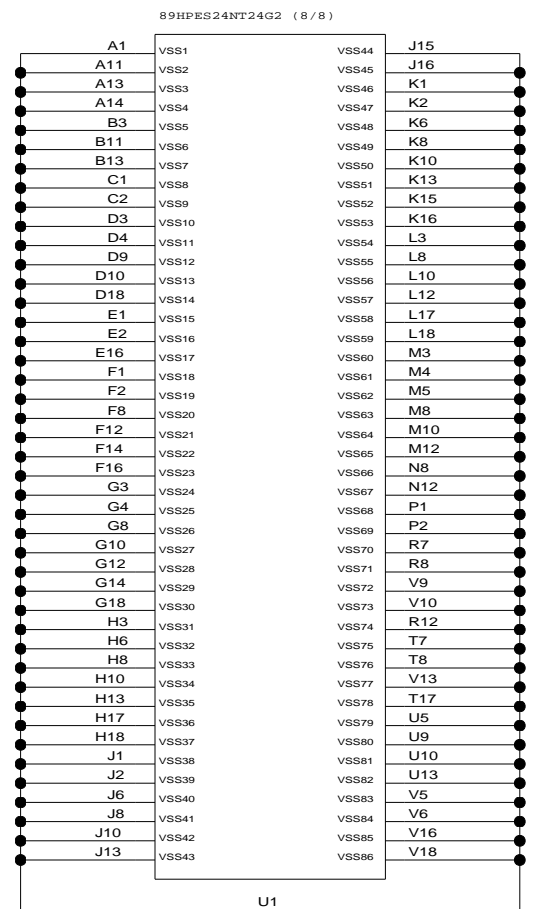
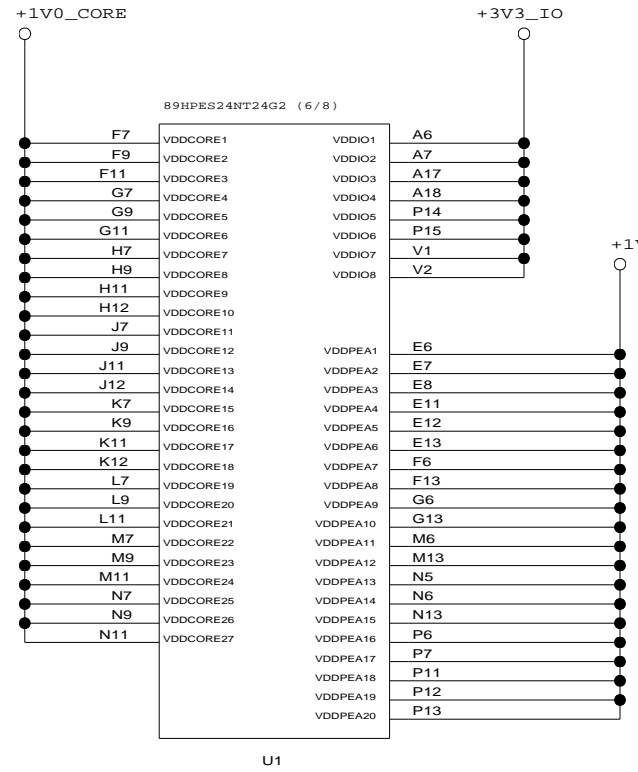
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LABEL: FAN
 LABEL:
 1 GND
 2 12V/5V
 3 NC



+12V3_PS
 +5V0_PS



TITLE EB-LOGAN-19			
24NT24G2 - POWER			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:44 2010			SHEET 7 OF 41

D

D

C

C

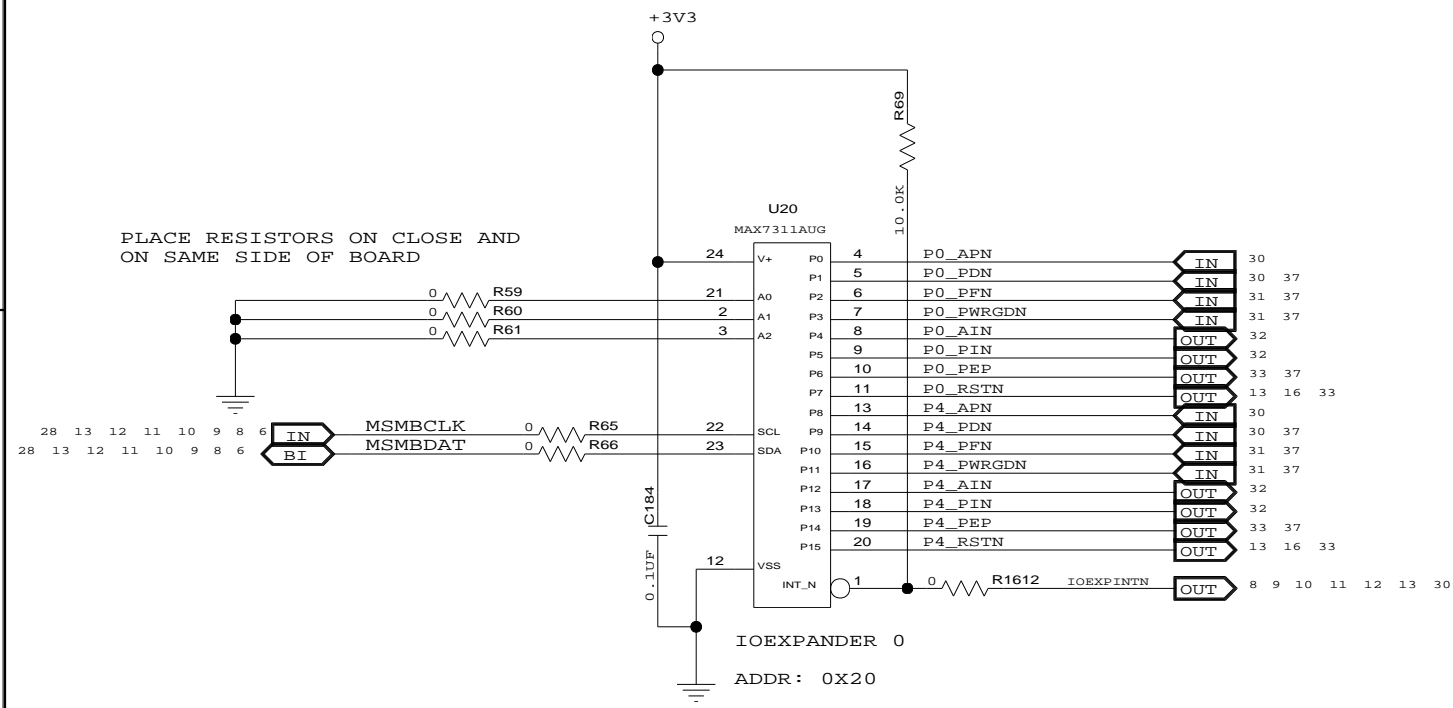
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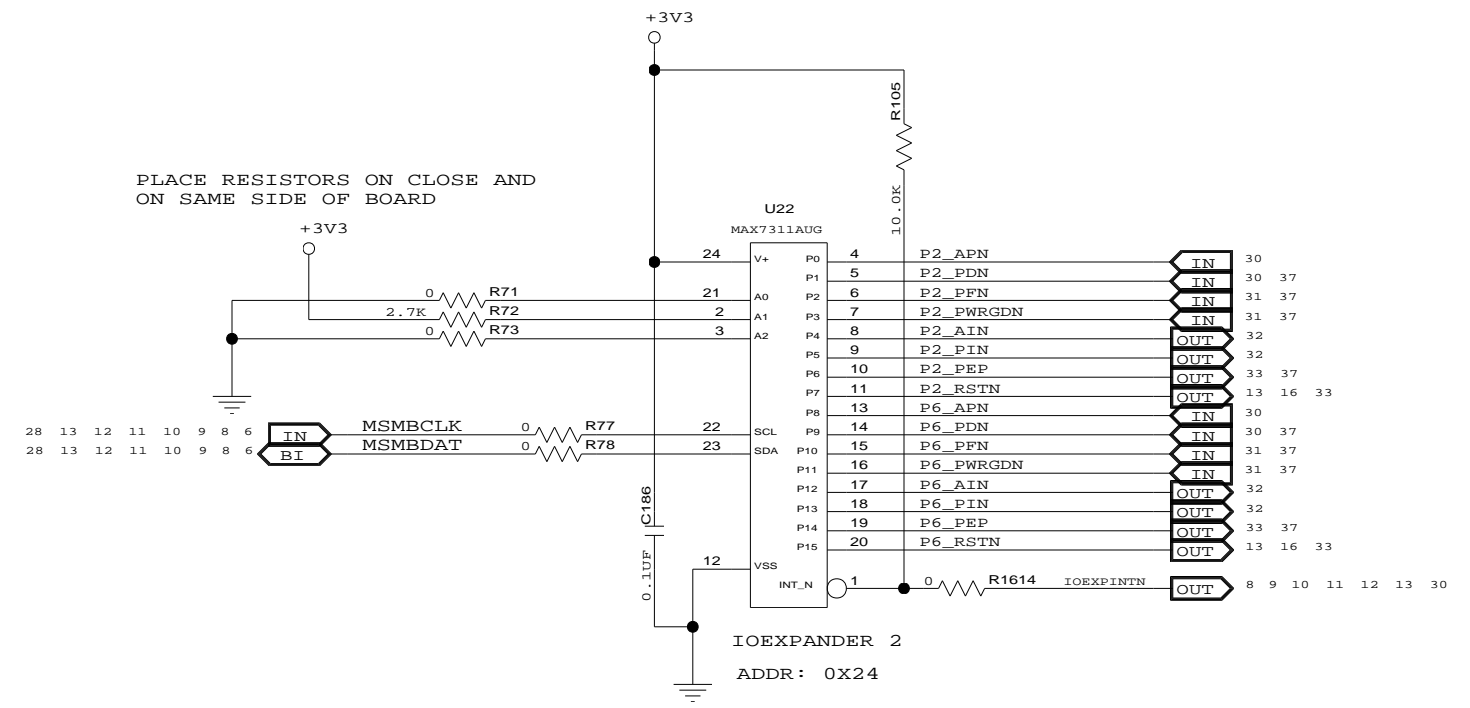
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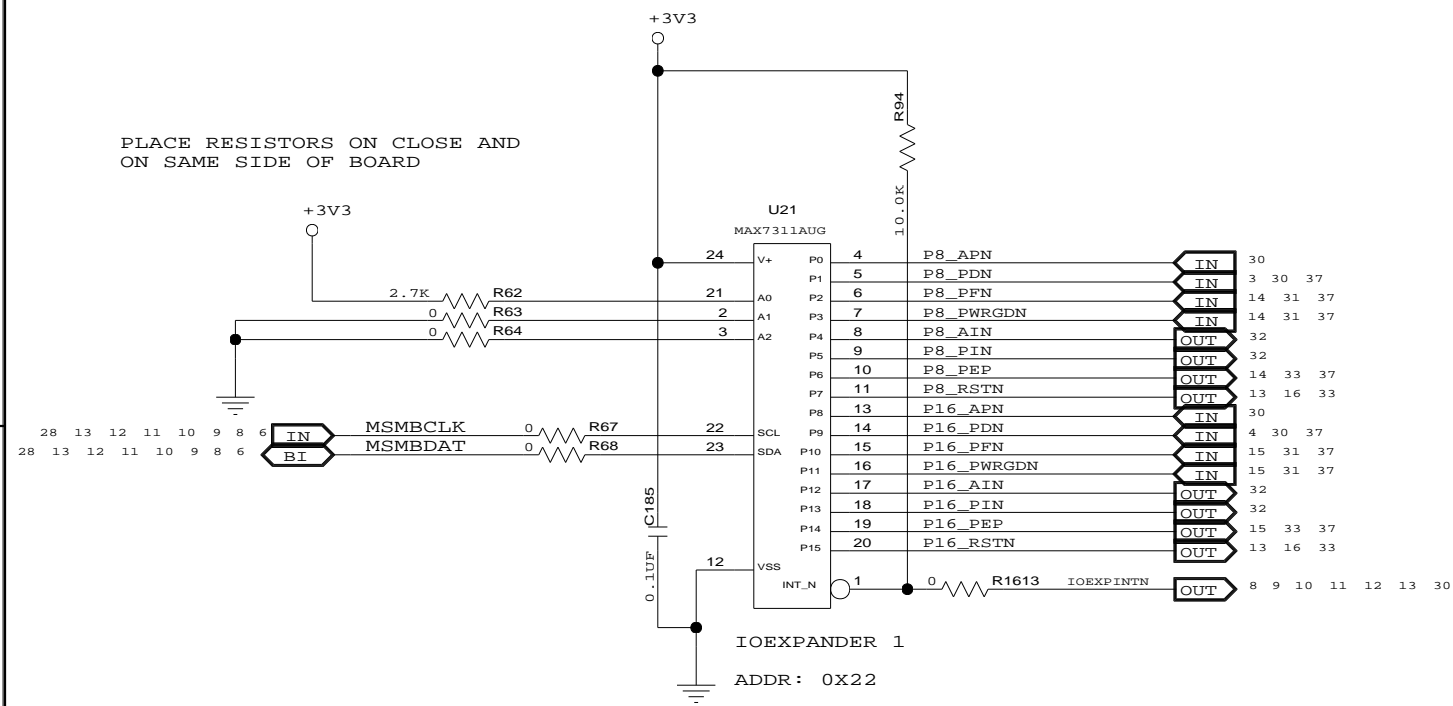
PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



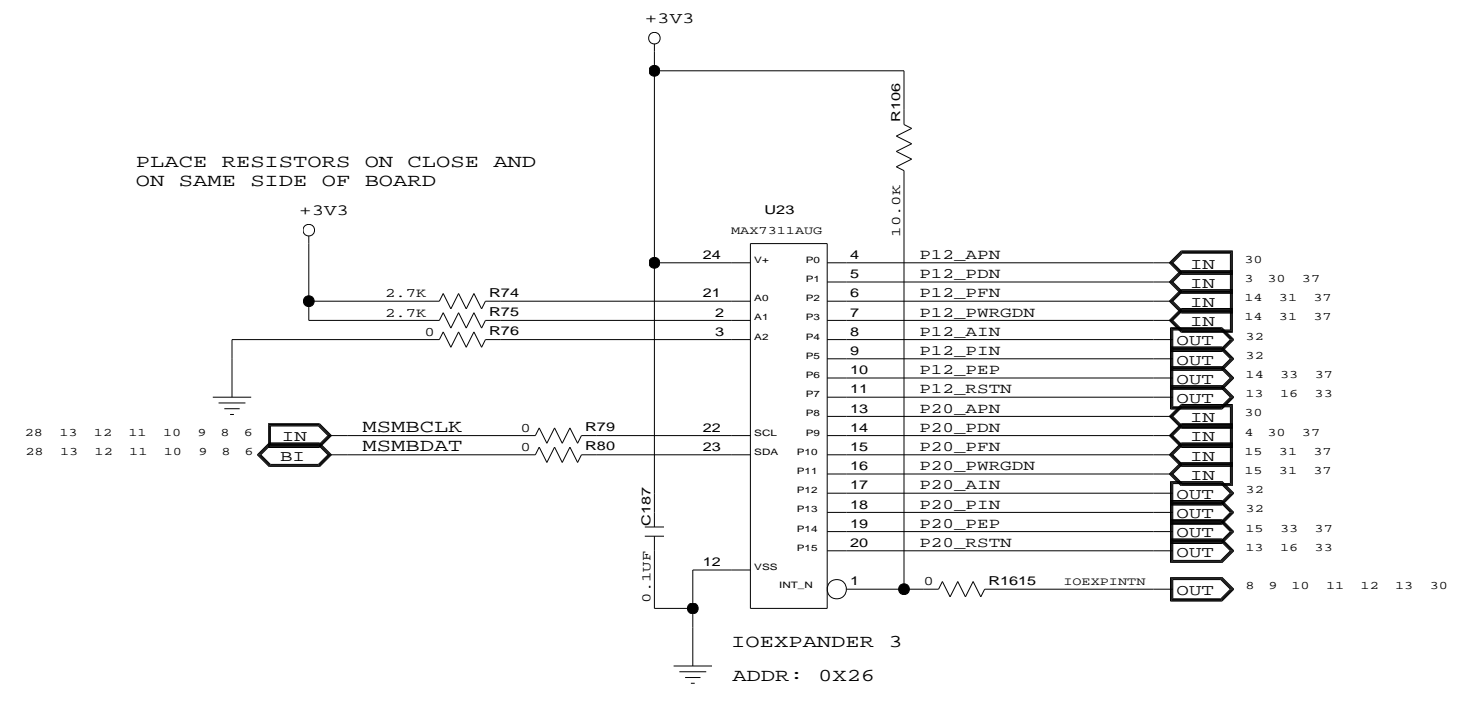
PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

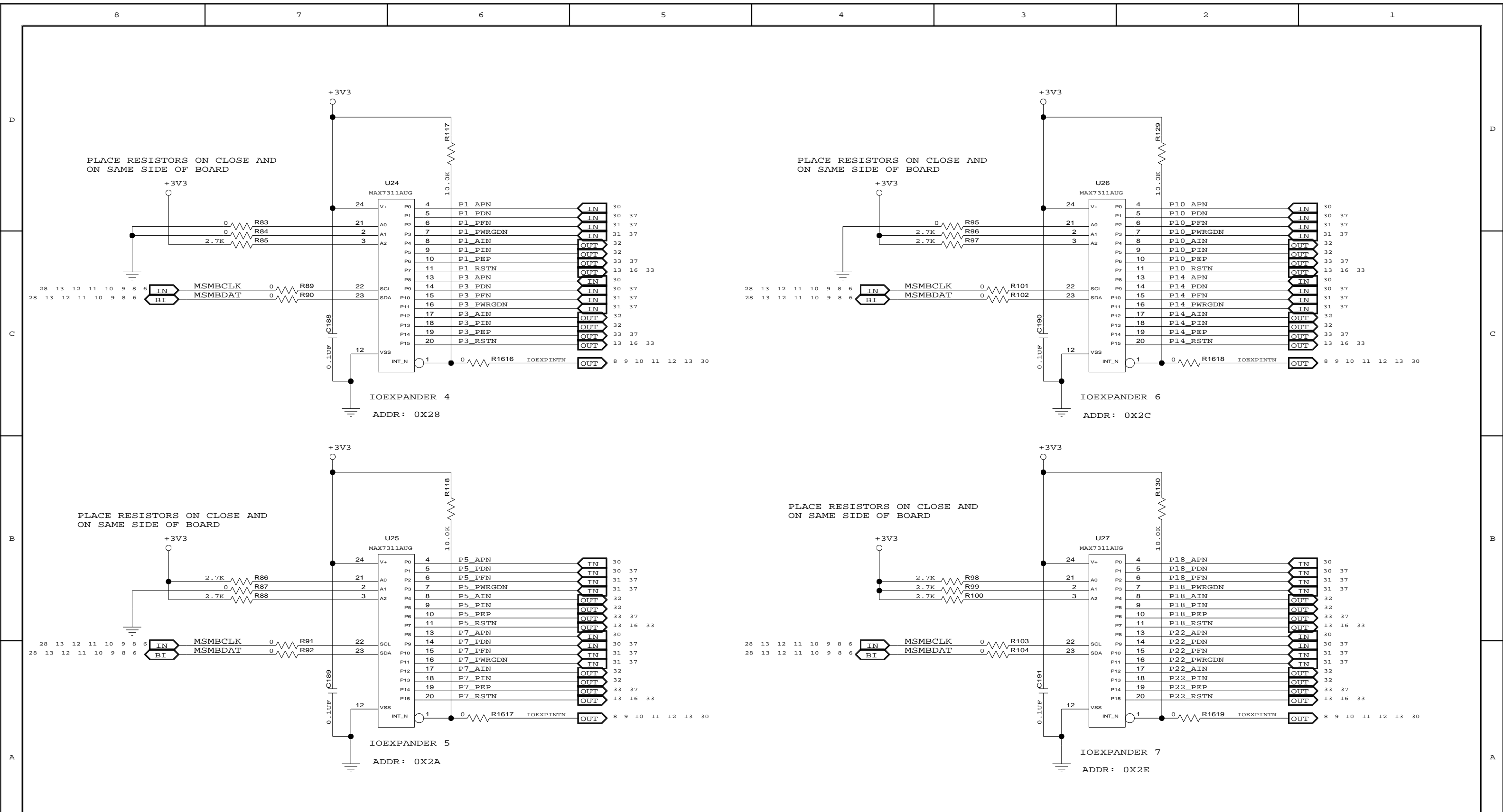



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TITLE EB-LOGAN-19

IOEXPANDER 0-3

SIZE	DRAWING NO.	FAB P/N	REV.
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TITLE EB-LOGAN-19

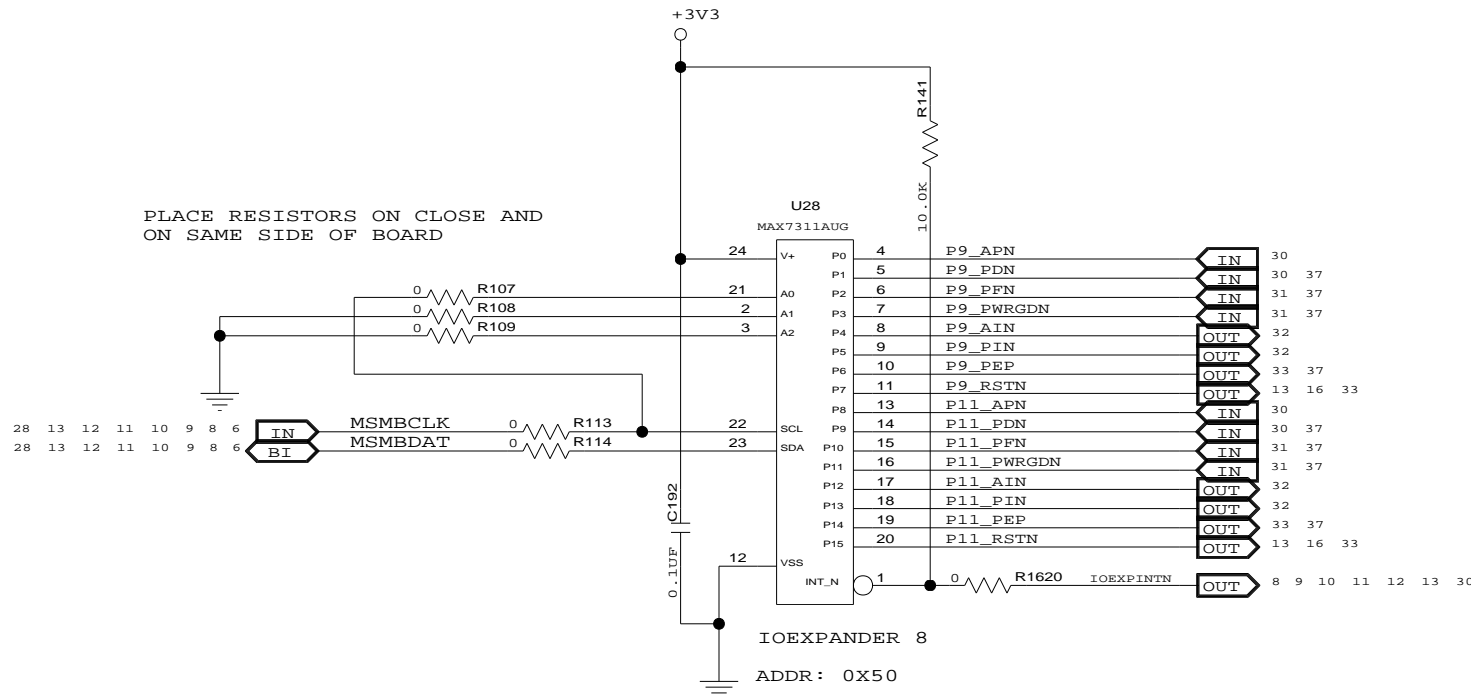
IOEXPANDER 4-7

SIZE	DRAWING NO.	FAB P/N	REV.
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AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:45 2010			SHEET 9 OF 41

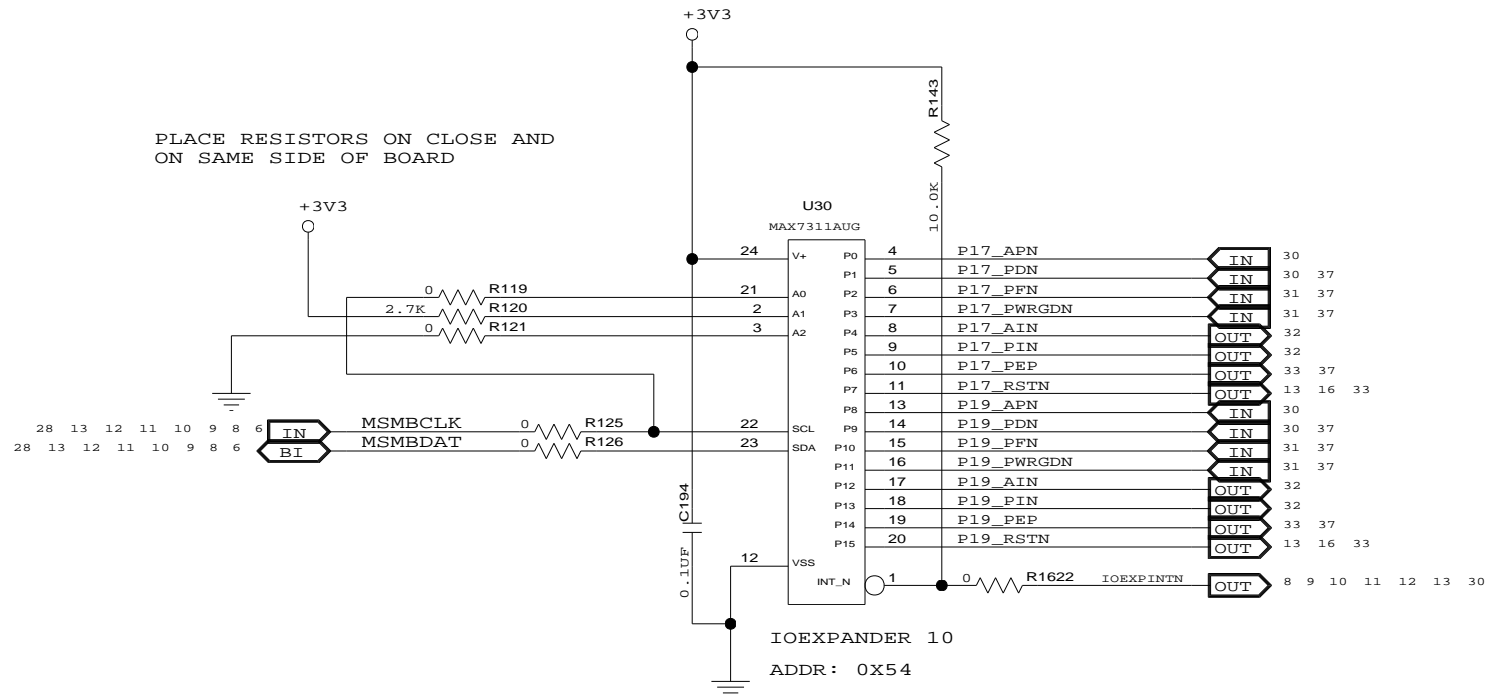
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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



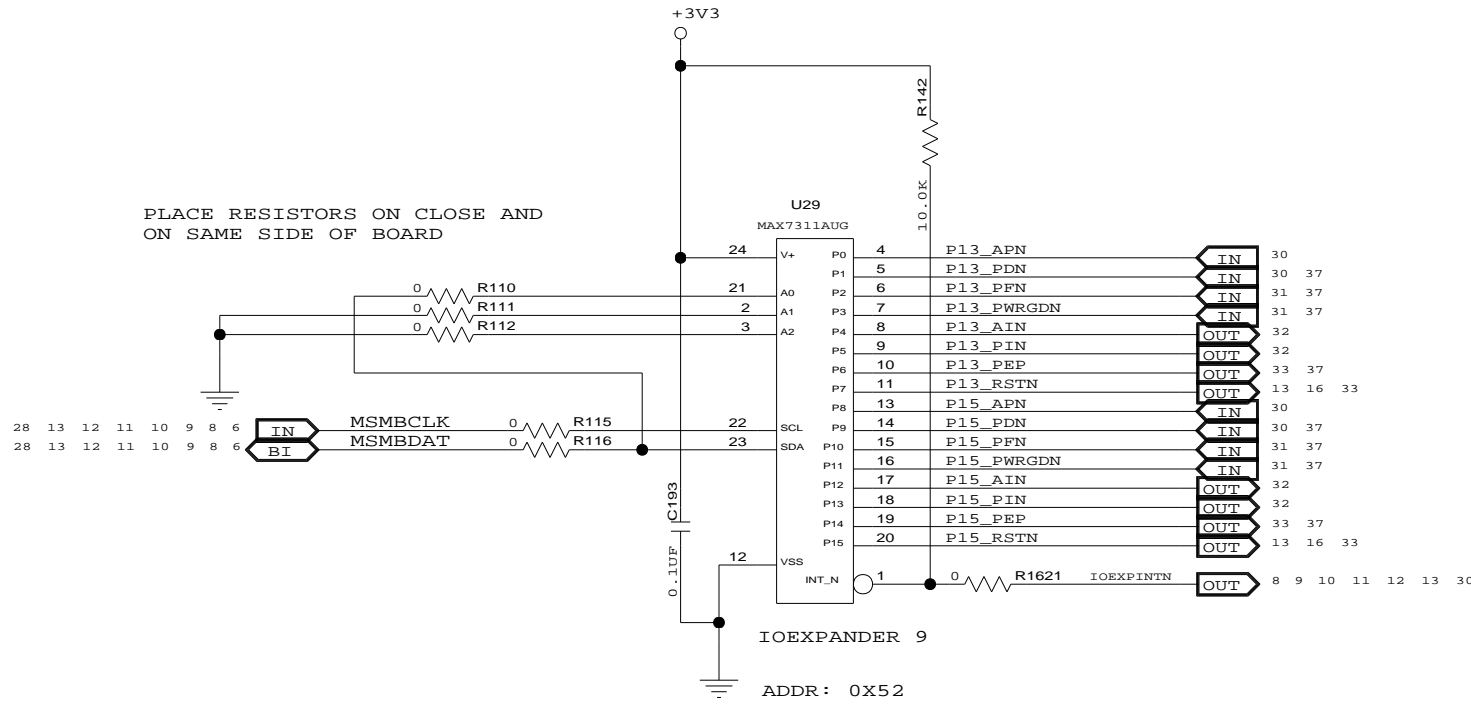
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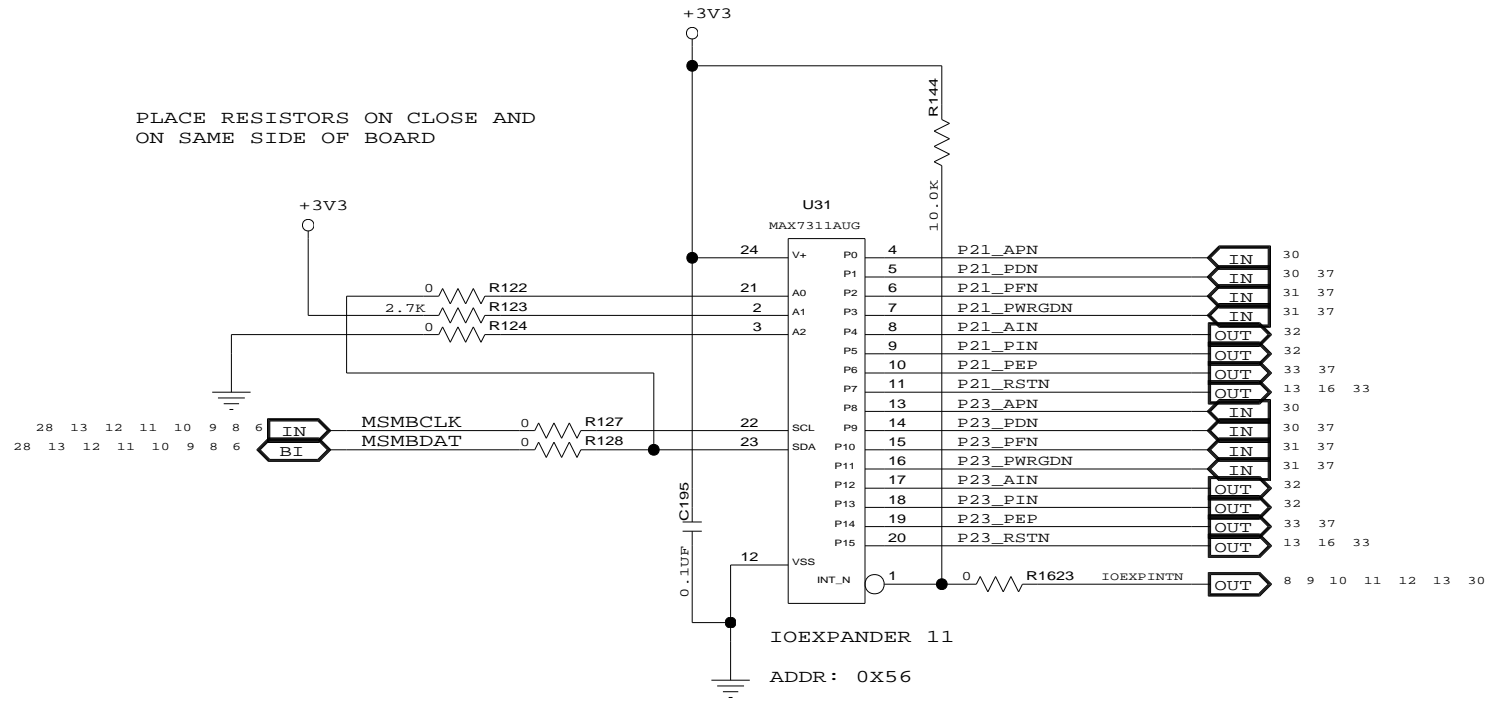
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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

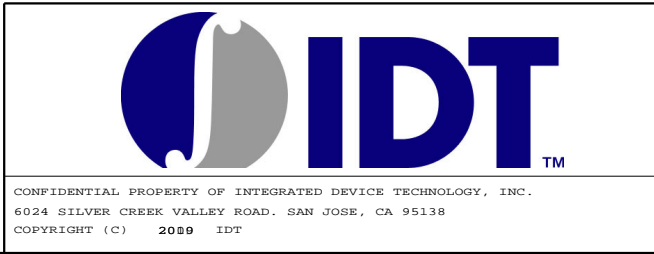


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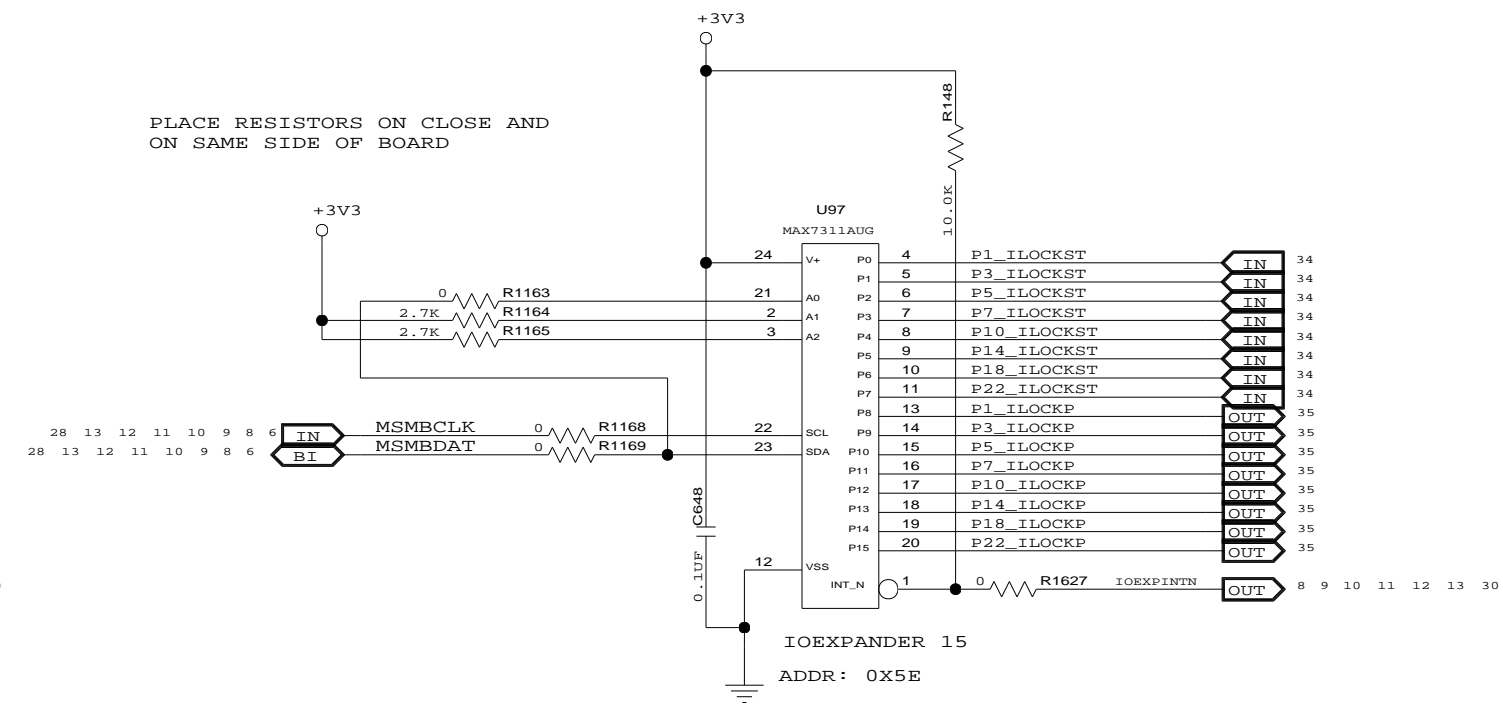
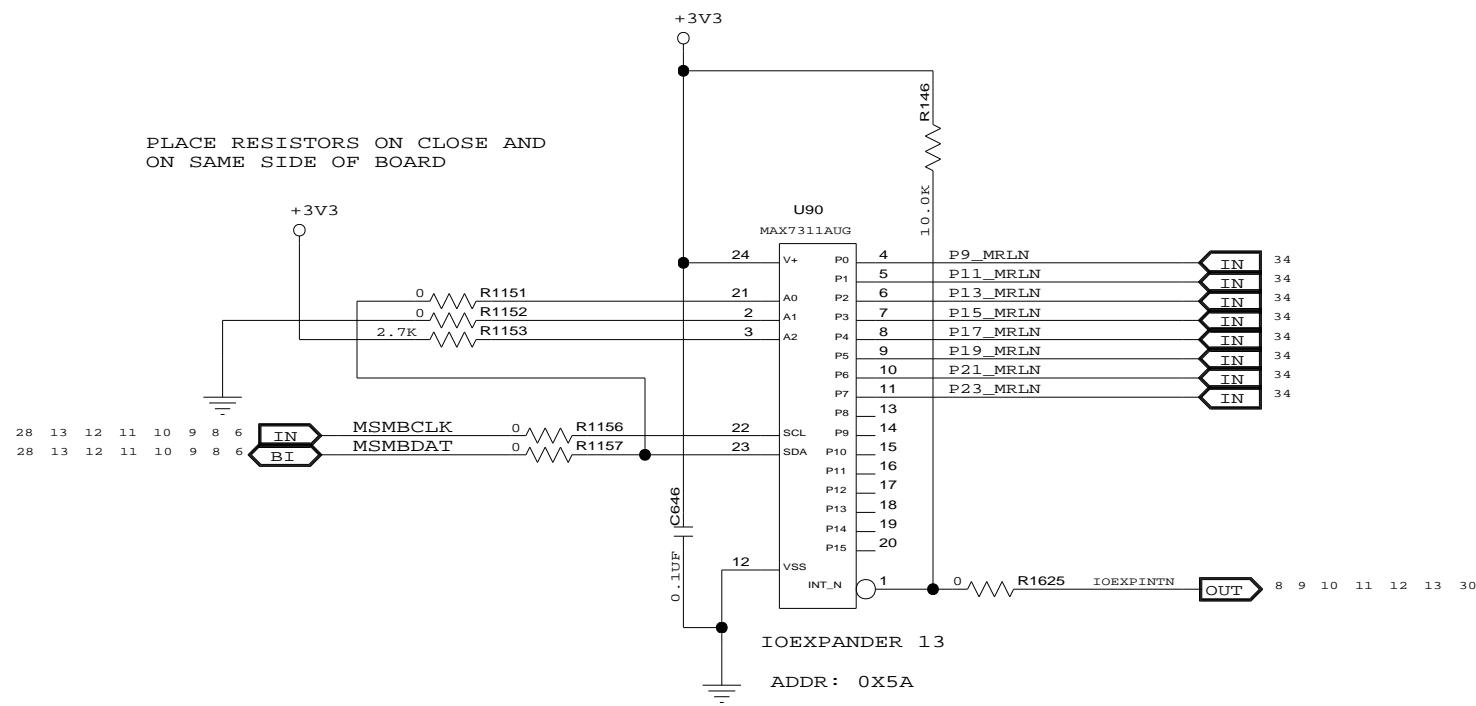
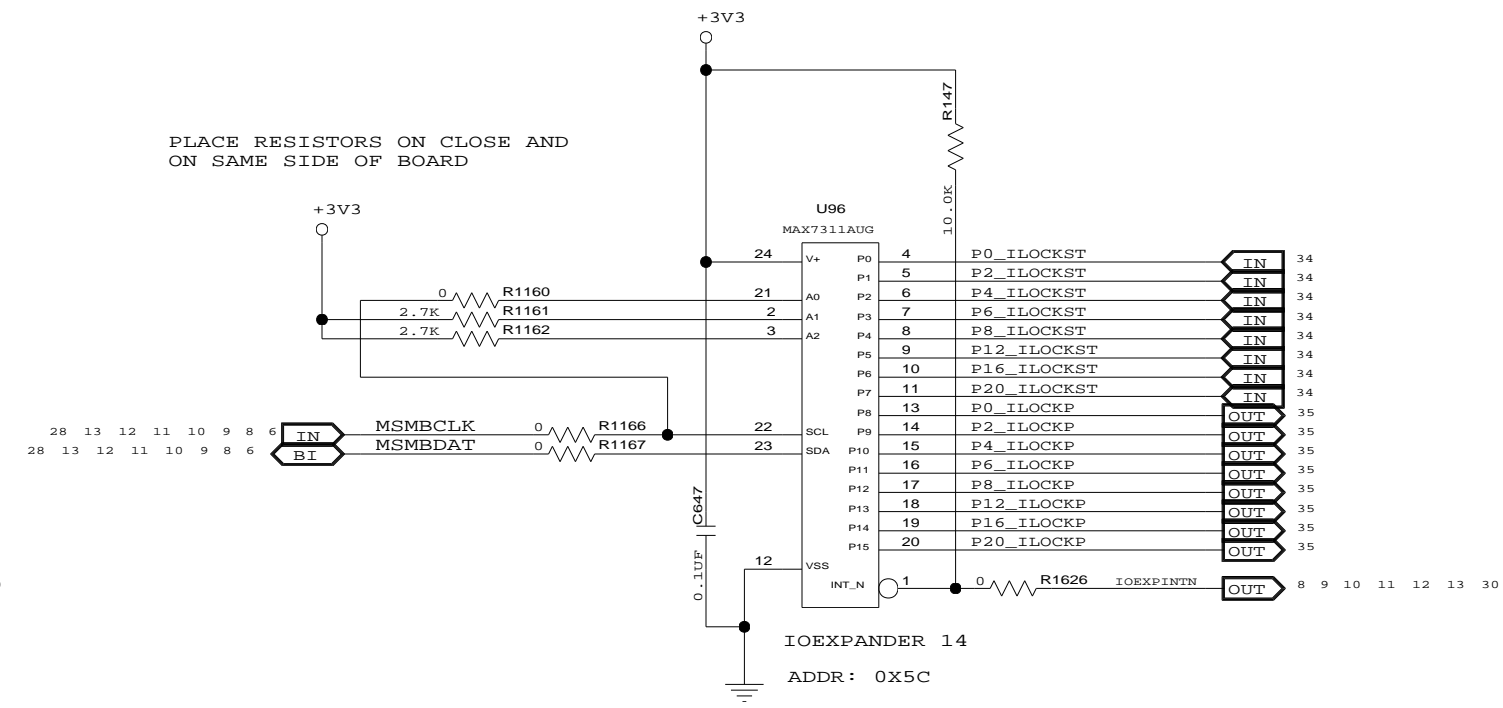
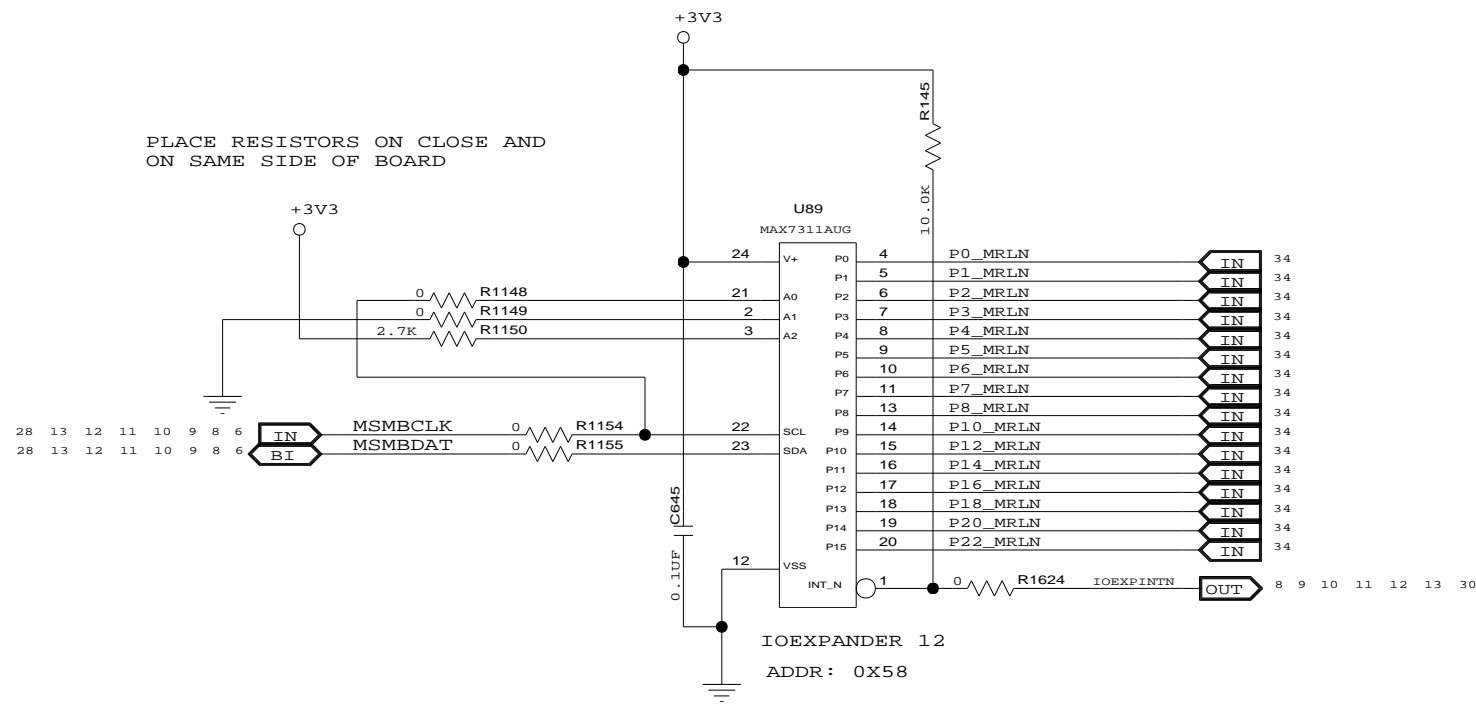
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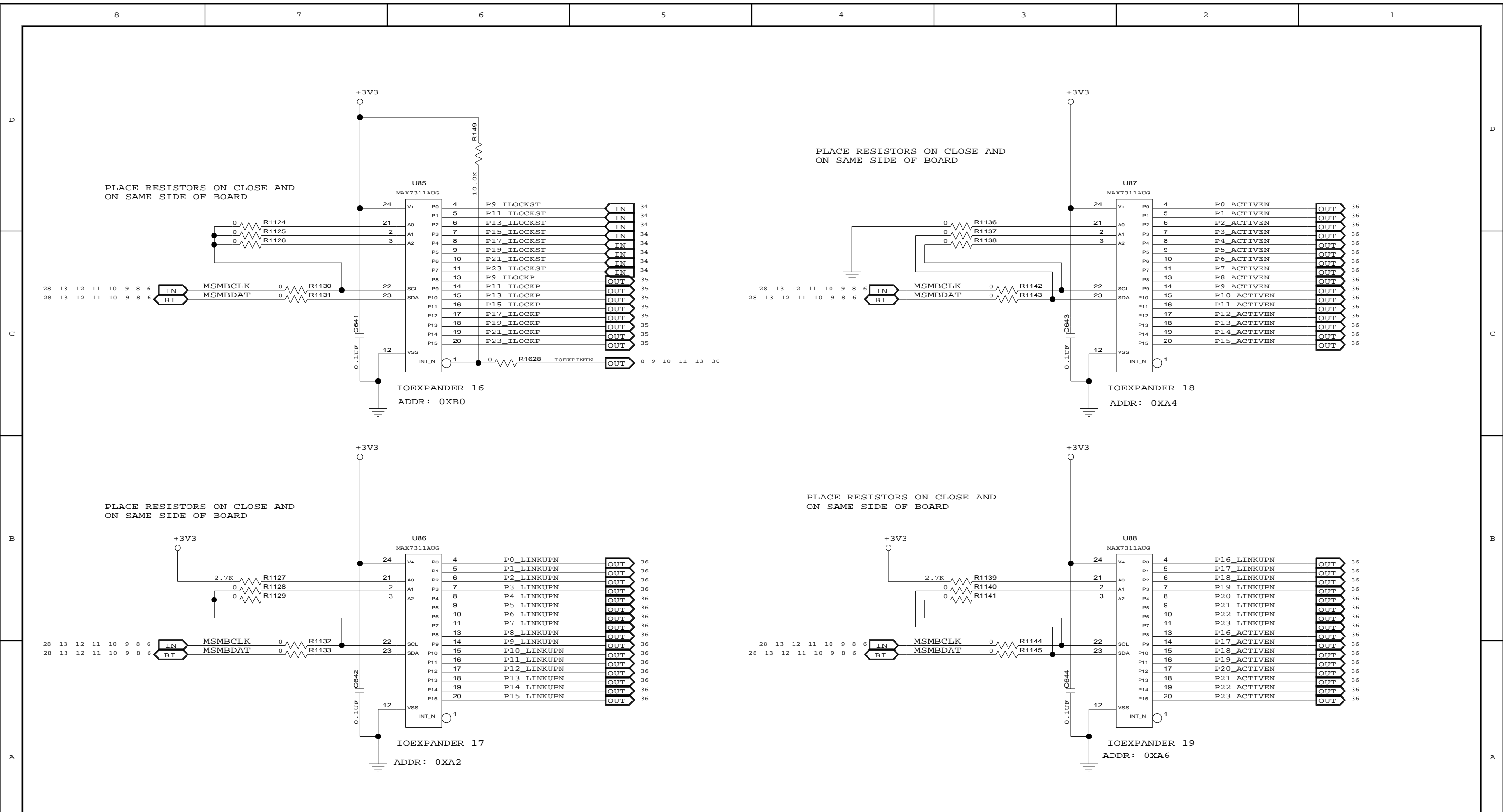


TITLE EB-LOGAN-19			
IOEXPANDER 8-11			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
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TITLE EB-LOGAN-19			
IOEXPANDER 12-15			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:45 2010			SHEET 11 OF 41



PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

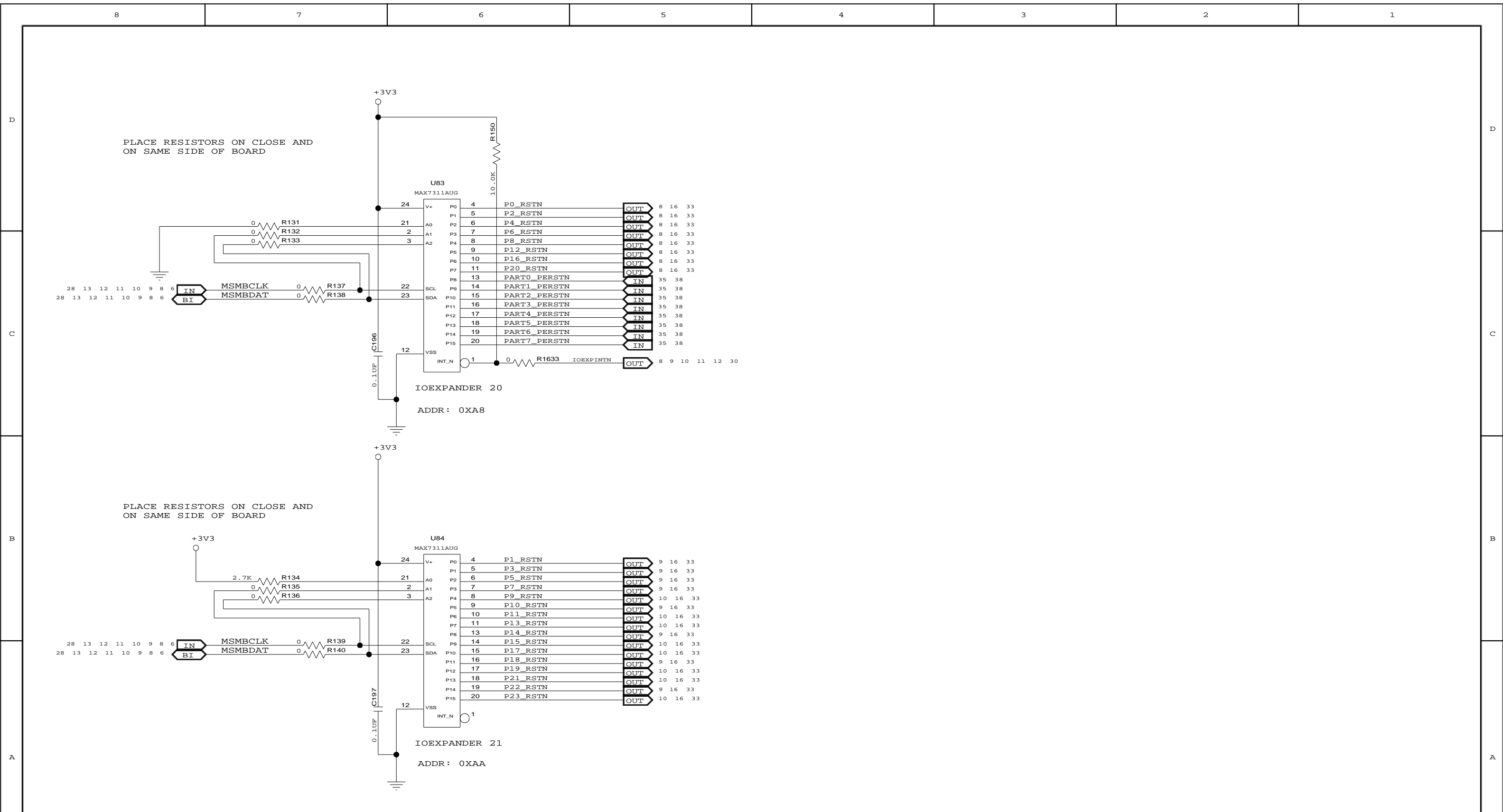
PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

TITLE EB-LOGAN-19

IOEXPANDER 16-19

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
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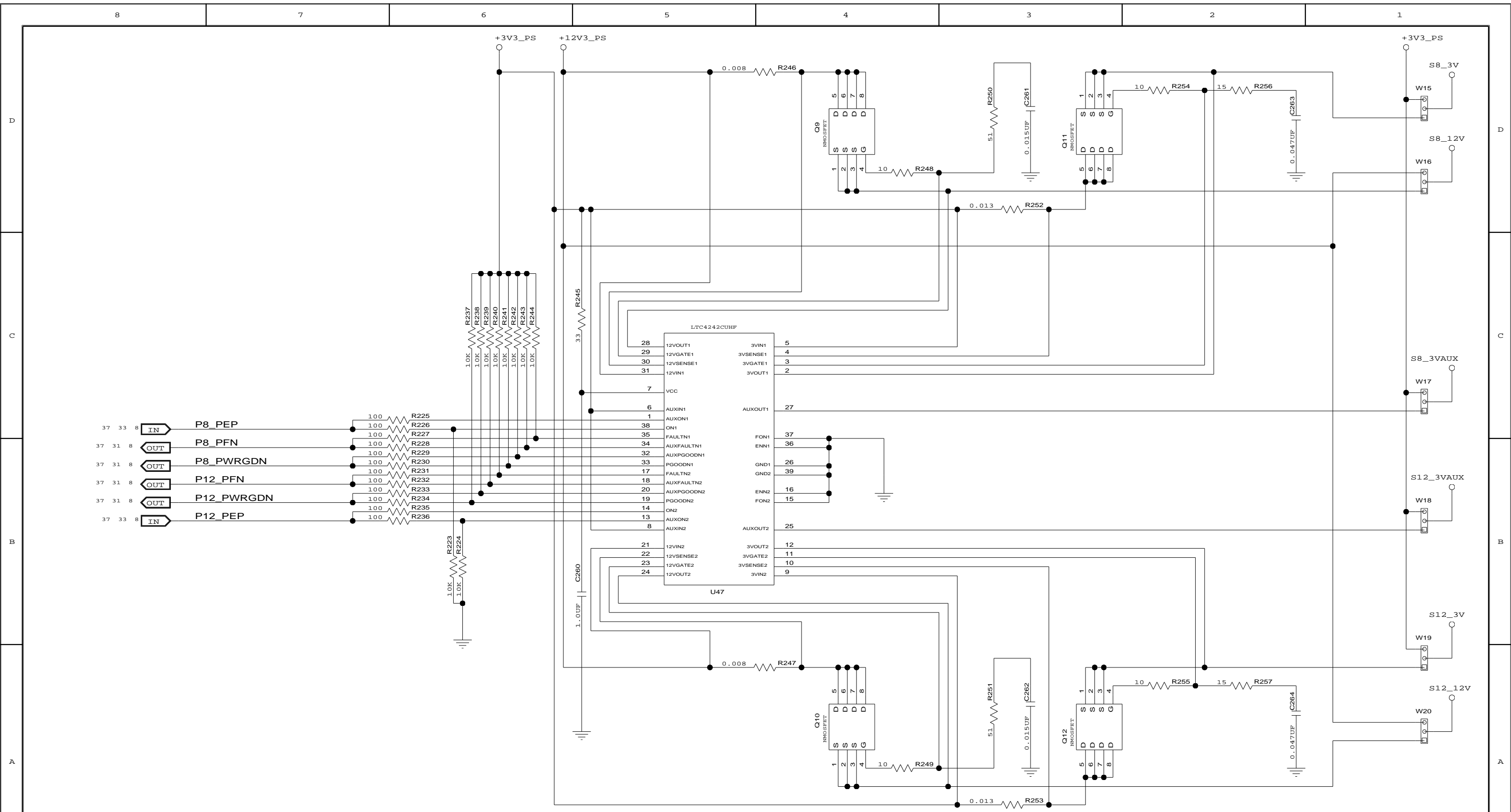



TITLE EB-LOGAN-19

IOEXPANDER 20-21

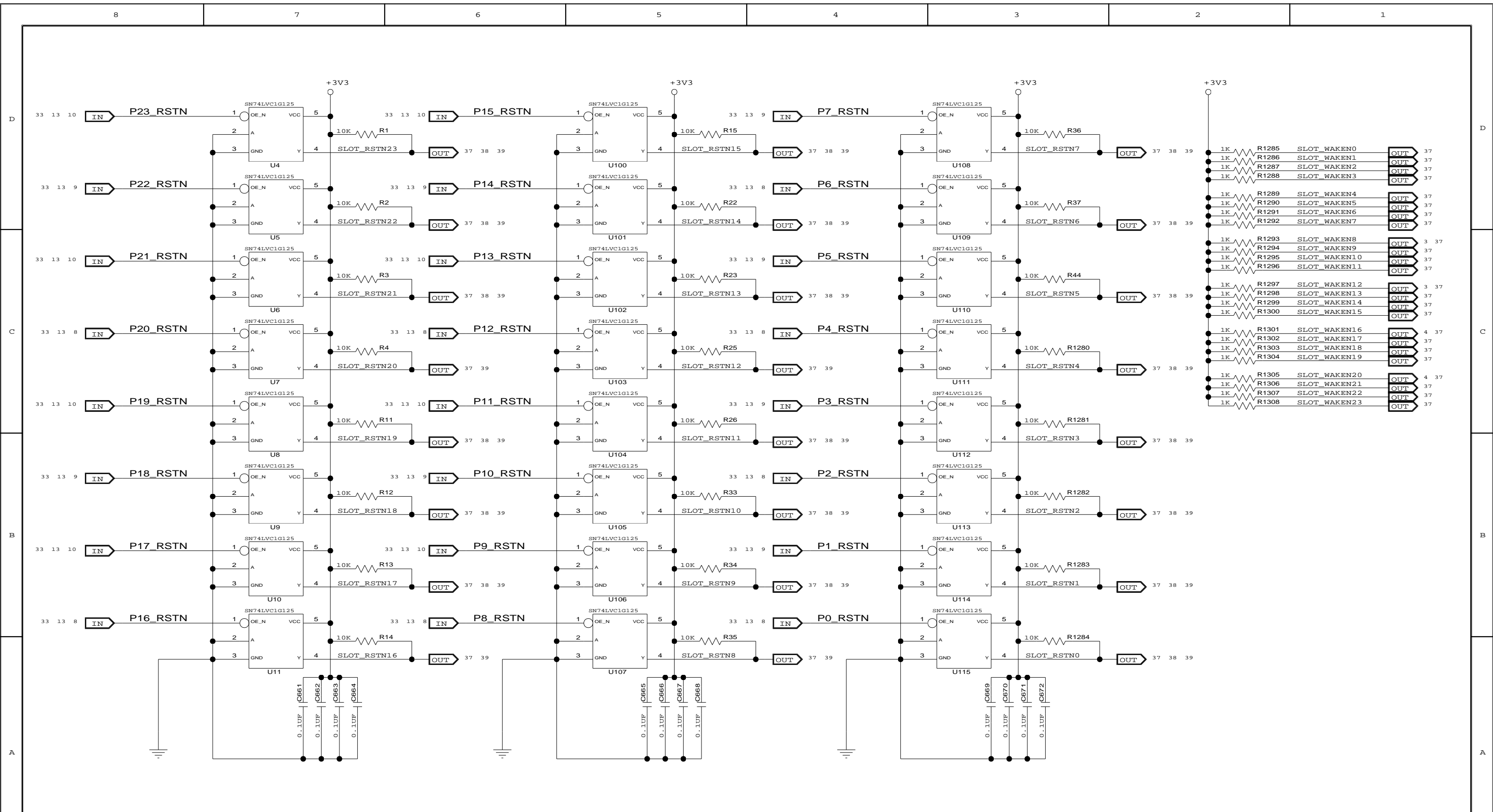
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B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
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TITLE EB-LOGAN-19			
HOT PLUG CONTROL PORTS 8-12			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:46 2010			SHEET 14 OF 41



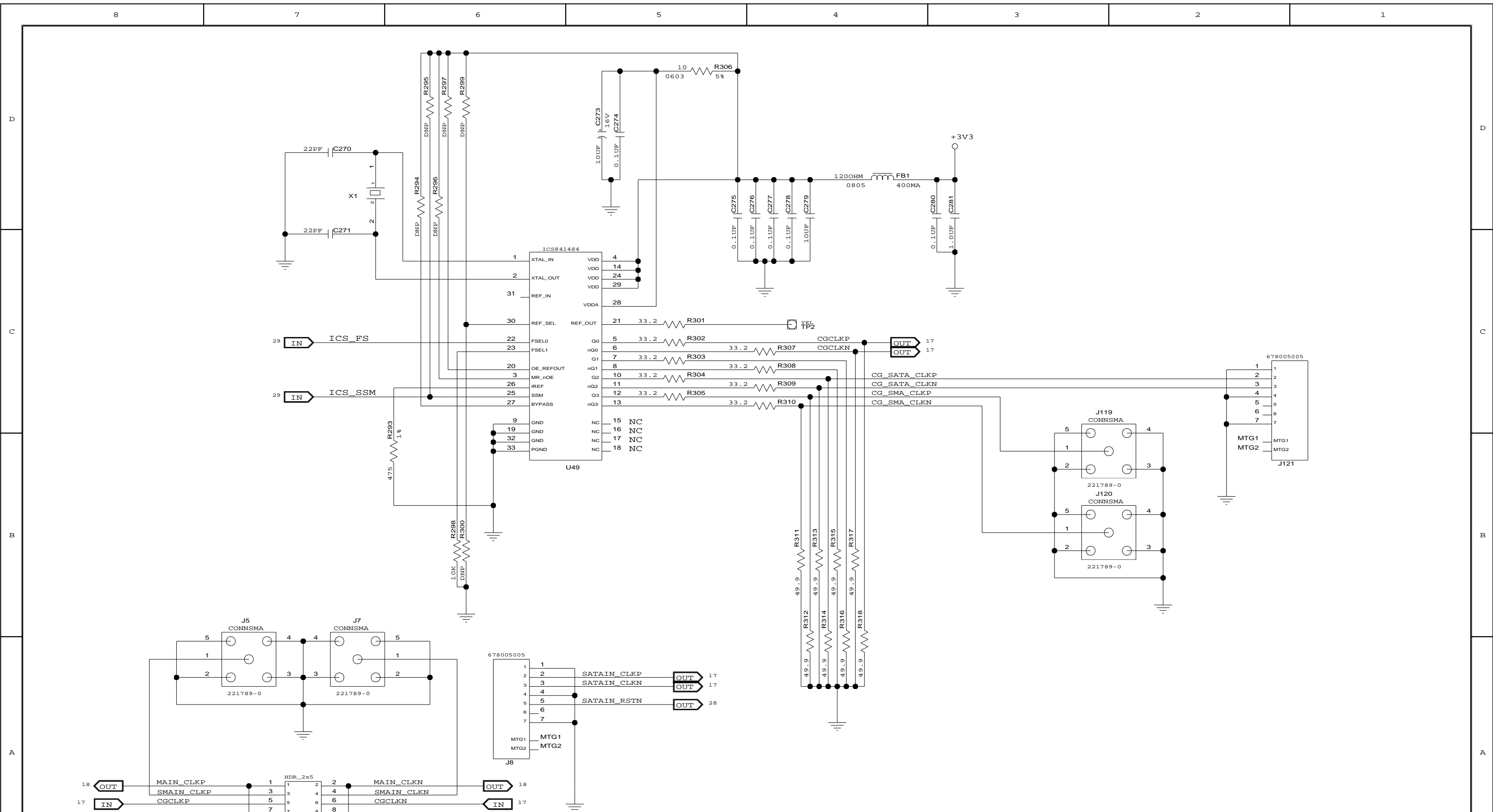



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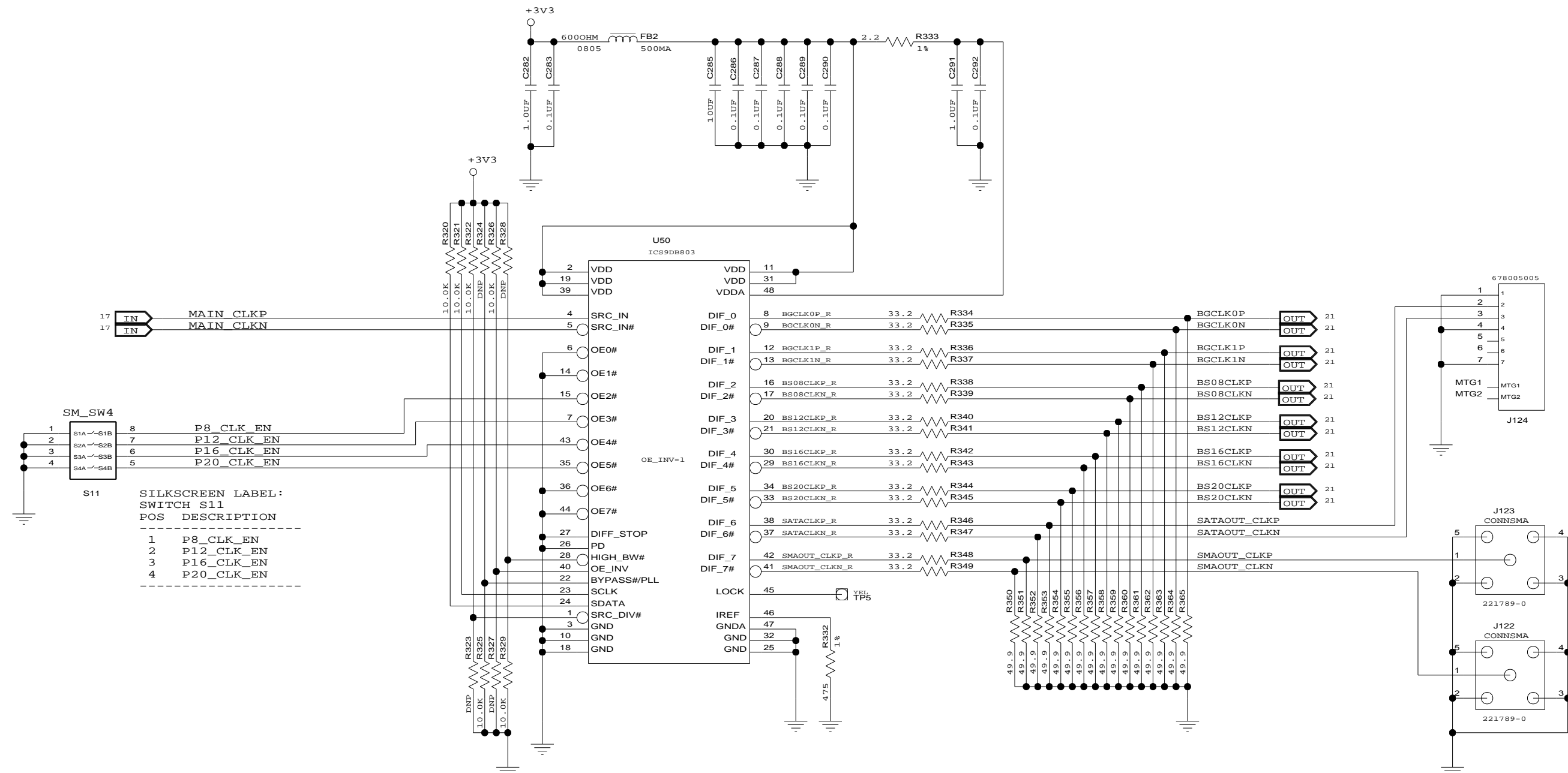
TITLE EB-LOGAN-19

SLOT RESETS AND WAKE PULL-UPS

SIZE	DRAWING NO.	FAB P/N	REV.
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AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:47 2010			SHEET 16 OF 41




		TITLE EB-LOGAN-19	
		CLOCK	
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
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		SHEET 17 OF 41	



SILKSCREEN LABEL:
SWITCH S11
POS DESCRIPTION

POS	DESCRIPTION
1	P8_CLK_EN
2	P12_CLK_EN
3	P16_CLK_EN
4	P20_CLK_EN



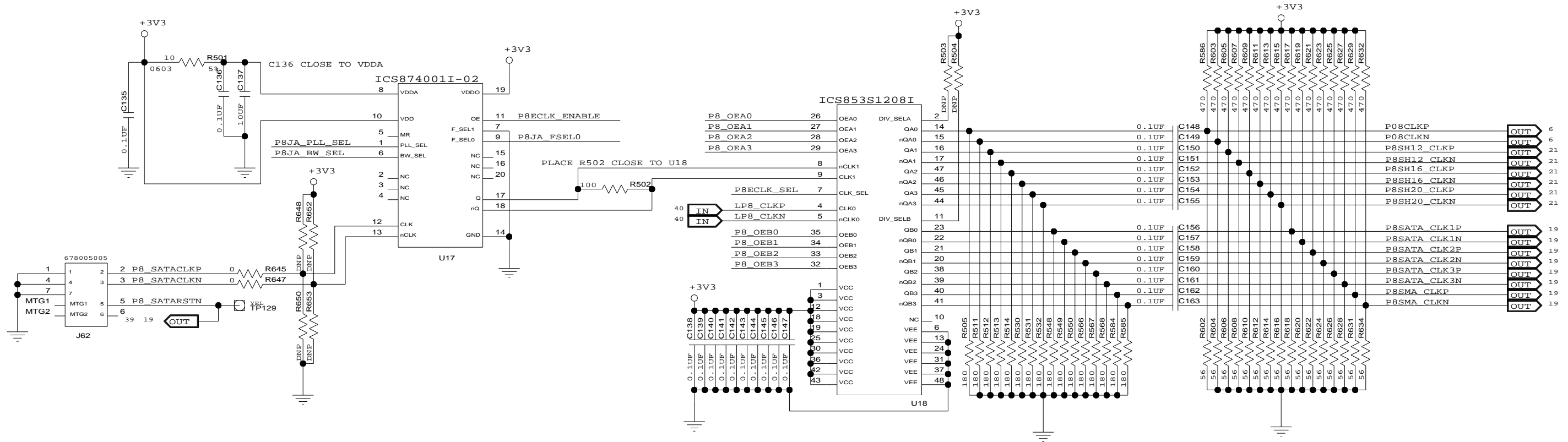
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TITLE EB-LOGAN-19

CLOCK BUFFER

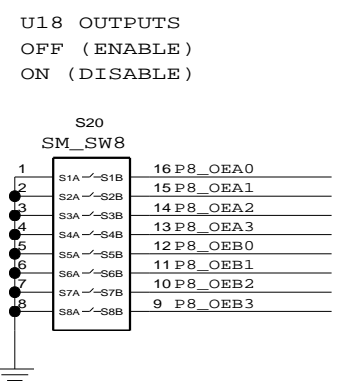
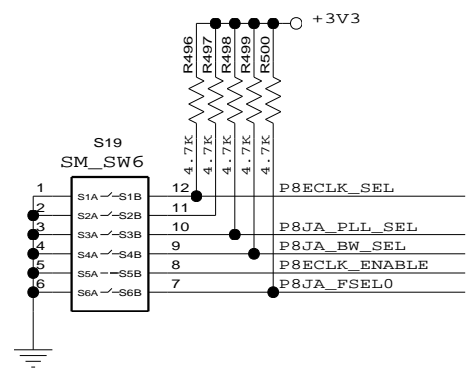
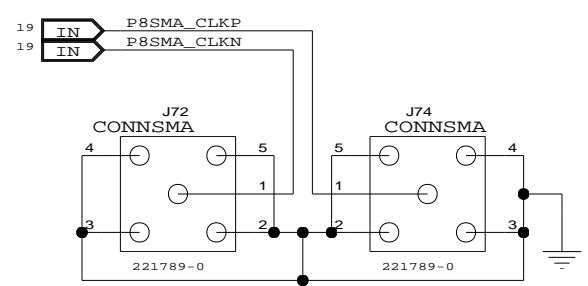
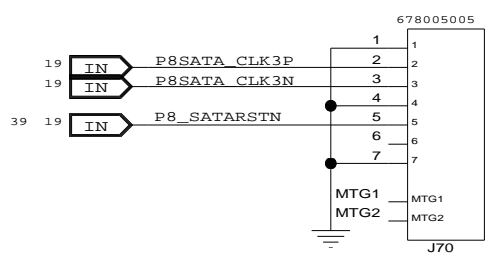
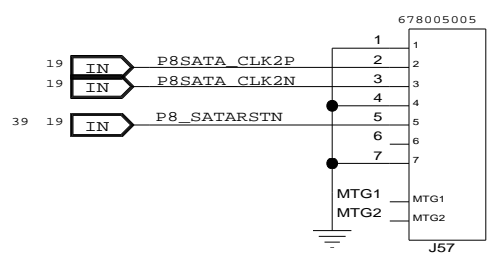
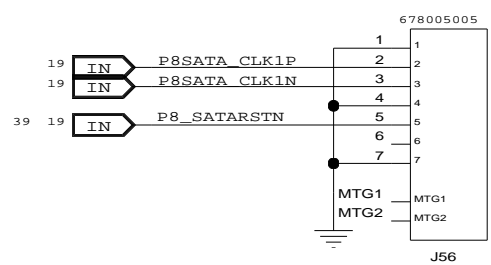
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:48 2010			SHEET 18 OF 41

P8CLK - DUT PORT 8 CLK
 LP8CLK - LOCAL CLOCK GEN. PORT 8 CLK
 P8SHXCLK - TO SLOT CLK HEADERS



DEFAULT DIPSW SETTING

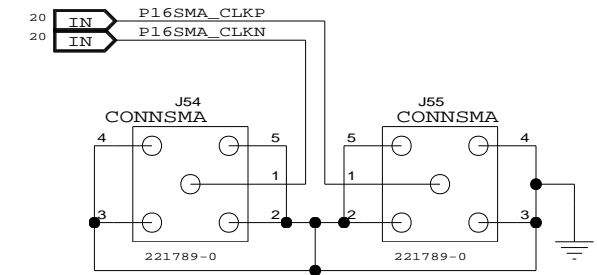
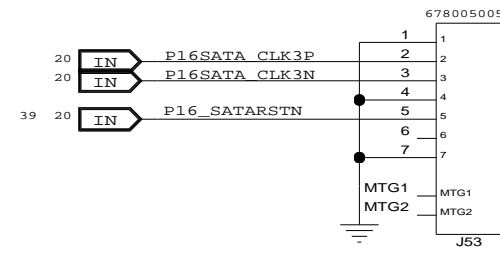
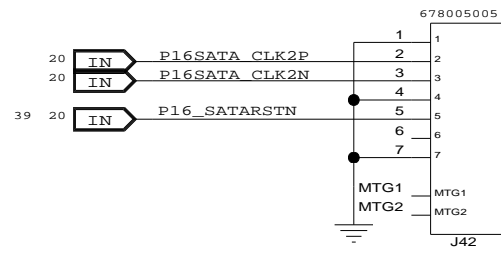
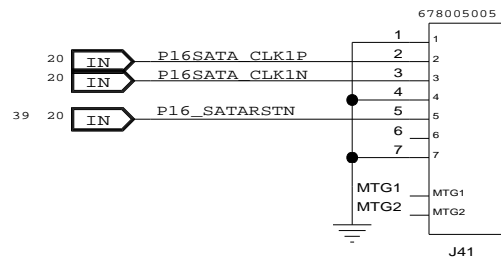
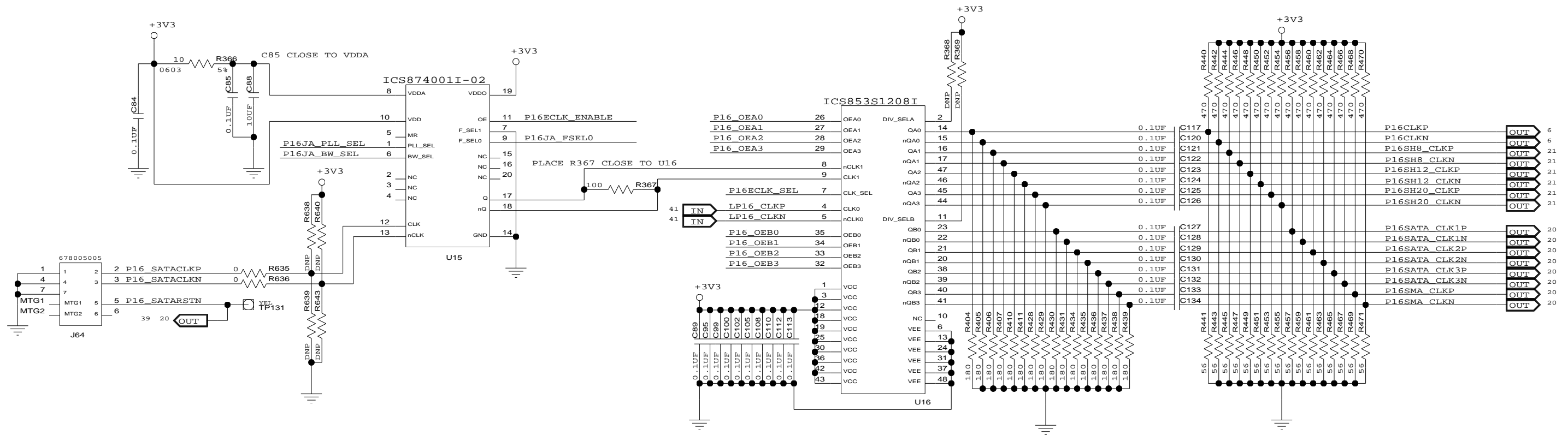
- S19:1 OFF (SATACLK)
- S19:3 OFF (PLL)
- S19:4 OFF (2.2MHZ)
- S19:5 OFF (U15 OUT ON)
- S19:6 ON (100MHZ)



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TITLE EB-LOGAN-19			
CLOCK SELECTOR DUT PCLK 8			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:28:22 2010			SHEET 19 OF 41

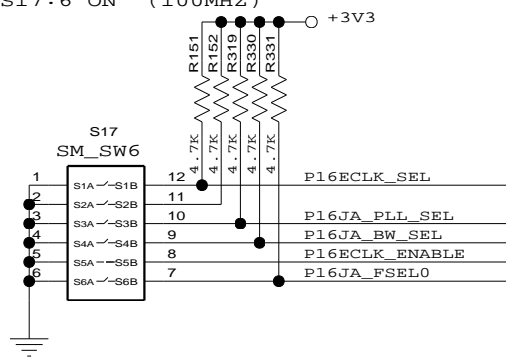
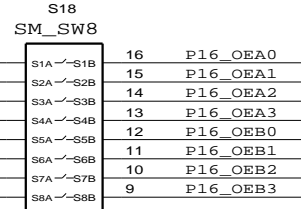
P16CLK - DUT PORT 16 CLK
 LP16CLK - LOCAL CLOCK GEN. PORT 16 CLK
 P16SHXCLK - TO SLOT CLK HEADERS



DEFAULT DIPSW SETTING

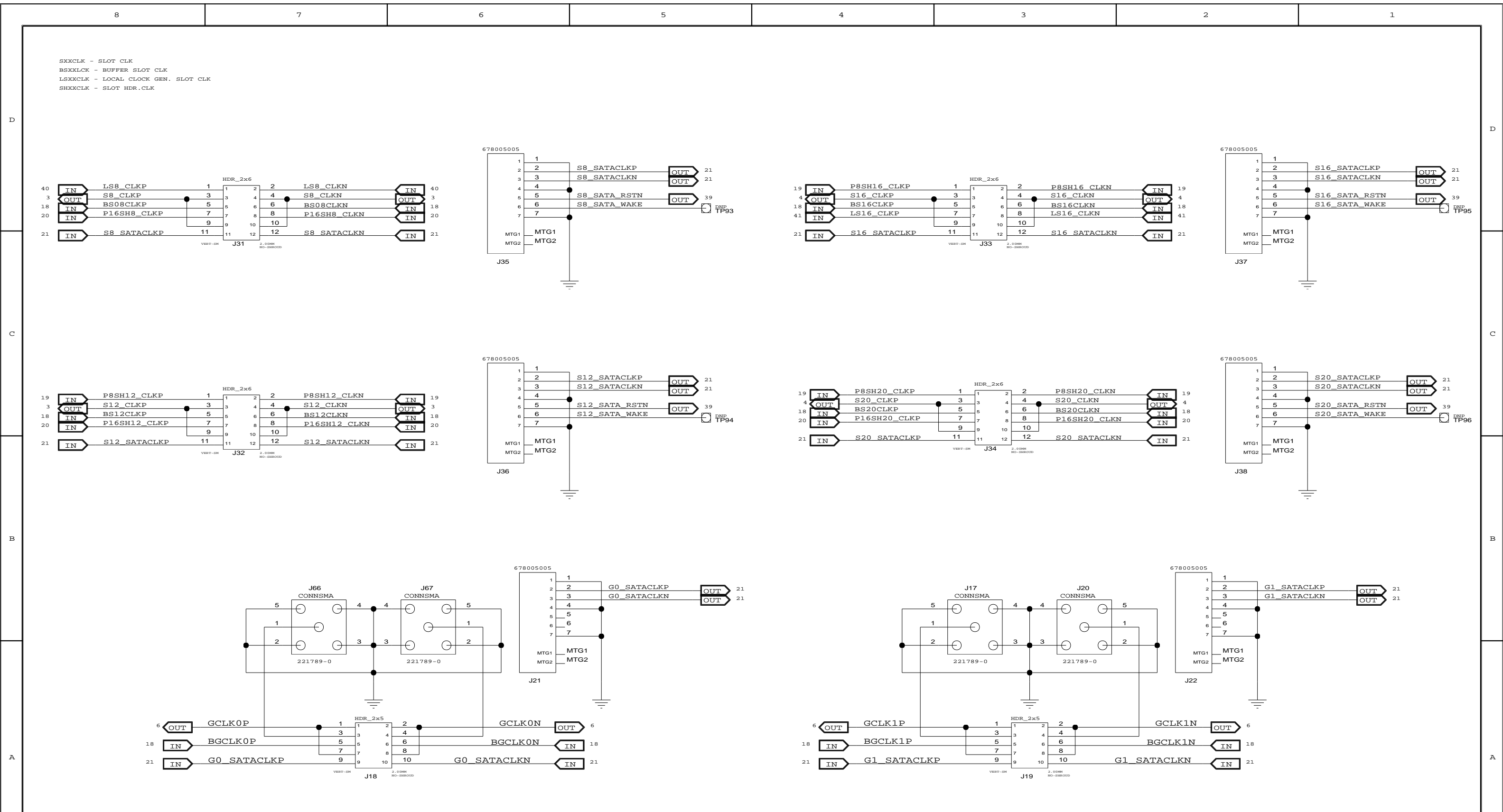
- S17:1 OFF (SATACLK)
- S17:3 OFF (PLL)
- S17:4 OFF (2.2MHZ)
- S17:5 OFF (U15 OUT ON)
- S17:6 ON (100MHZ)

U16 OUTPUTS
 OFF (ENABLE)
 ON (DISABLE)

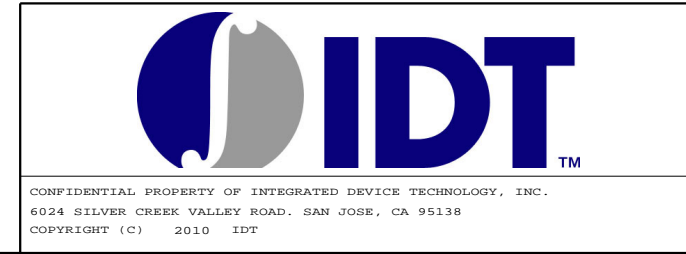


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TITLE EB-LOGAN-19			
CLOCK SELECTOR DUT PCLK 16			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:28:19 2010			SHEET 20 OF 41

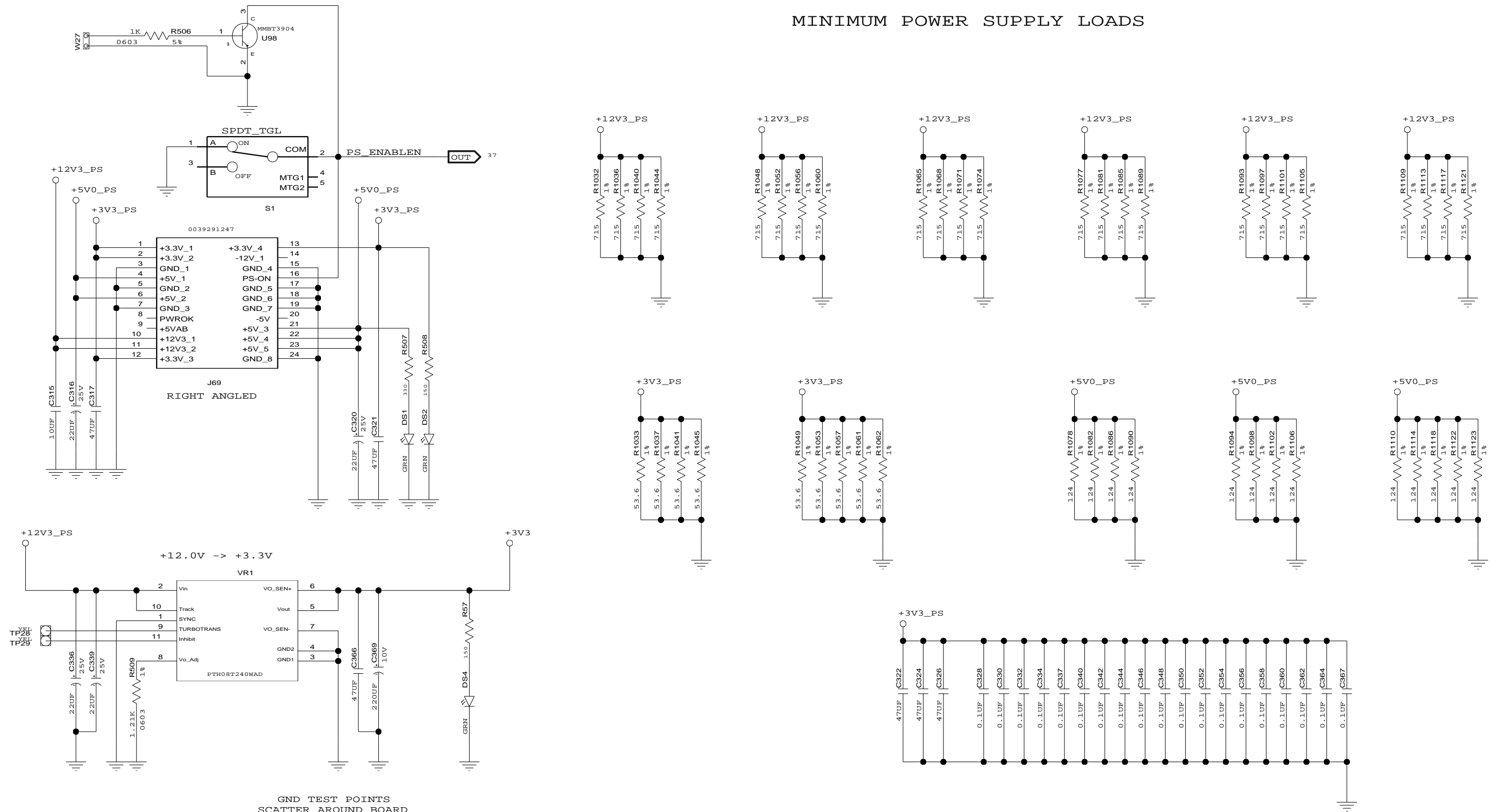


SXXCLK - SLOT CLK
 BSXXCLK - BUFFER SLOT CLK
 LSXXCLK - LOCAL CLOCK GEN. SLOT CLK
 SHXXCLK - SLOT HDR.CLK

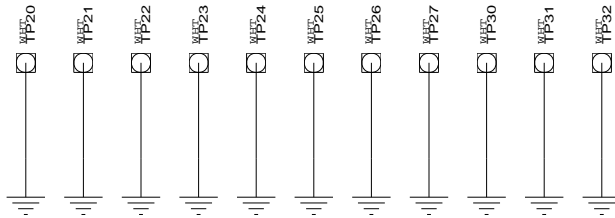
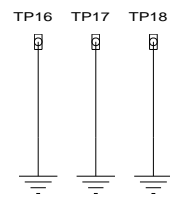


TITLE EB-LOGAN-19			
CLOCK SELECTOR SLOTS 8-20, GCLK			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:49 2010			SHEET 21 OF 41

MINIMUM POWER SUPPLY LOADS

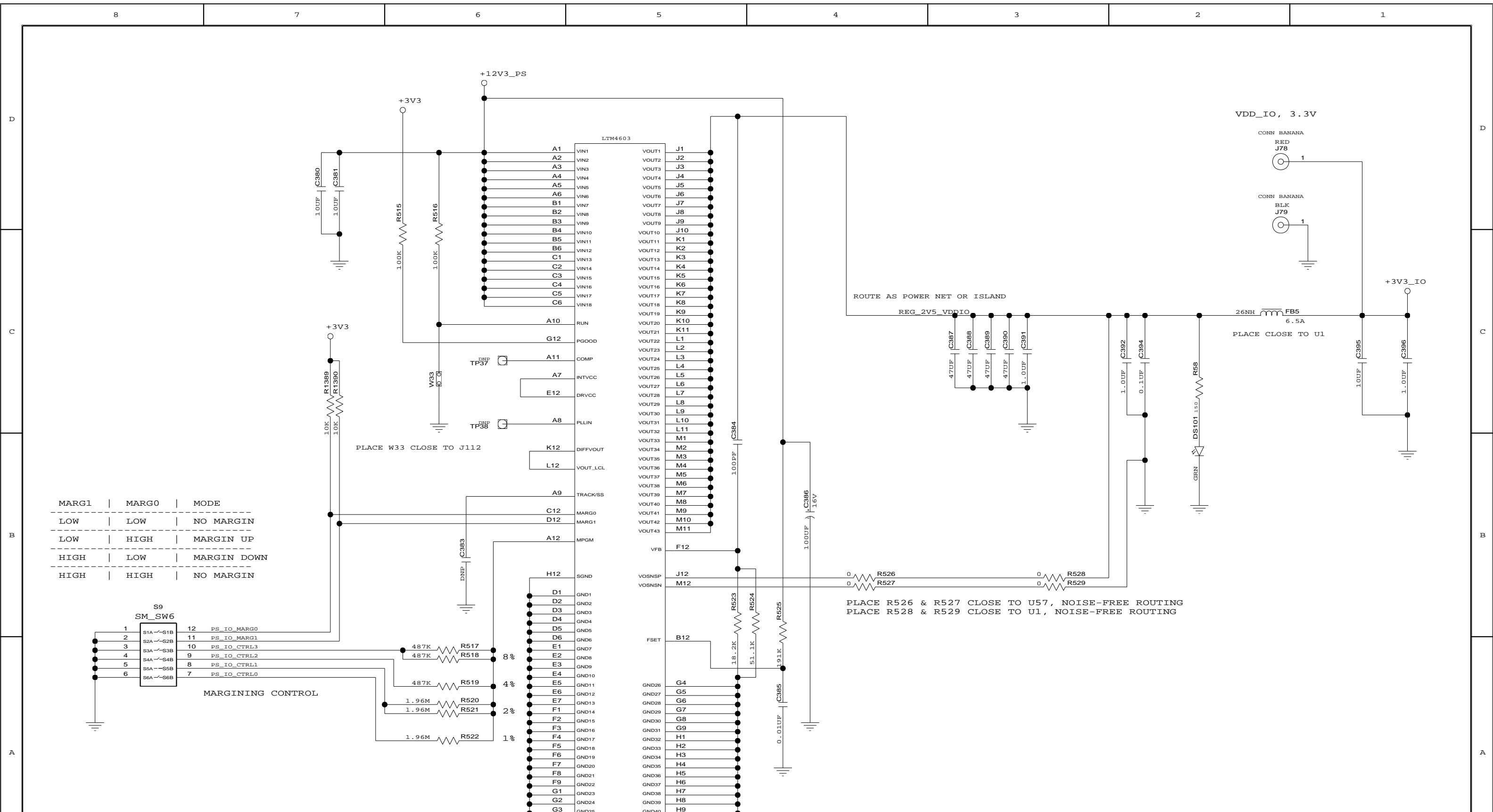


GND TEST POINTS
SCATTER AROUND BOARD



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TITLE EB-LOGAN-19			
POWER CONNECTORS, MIN LOAD RESISTORS			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:50 2010			SHEET 22 OF 41



MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

MARGINING CONTROL

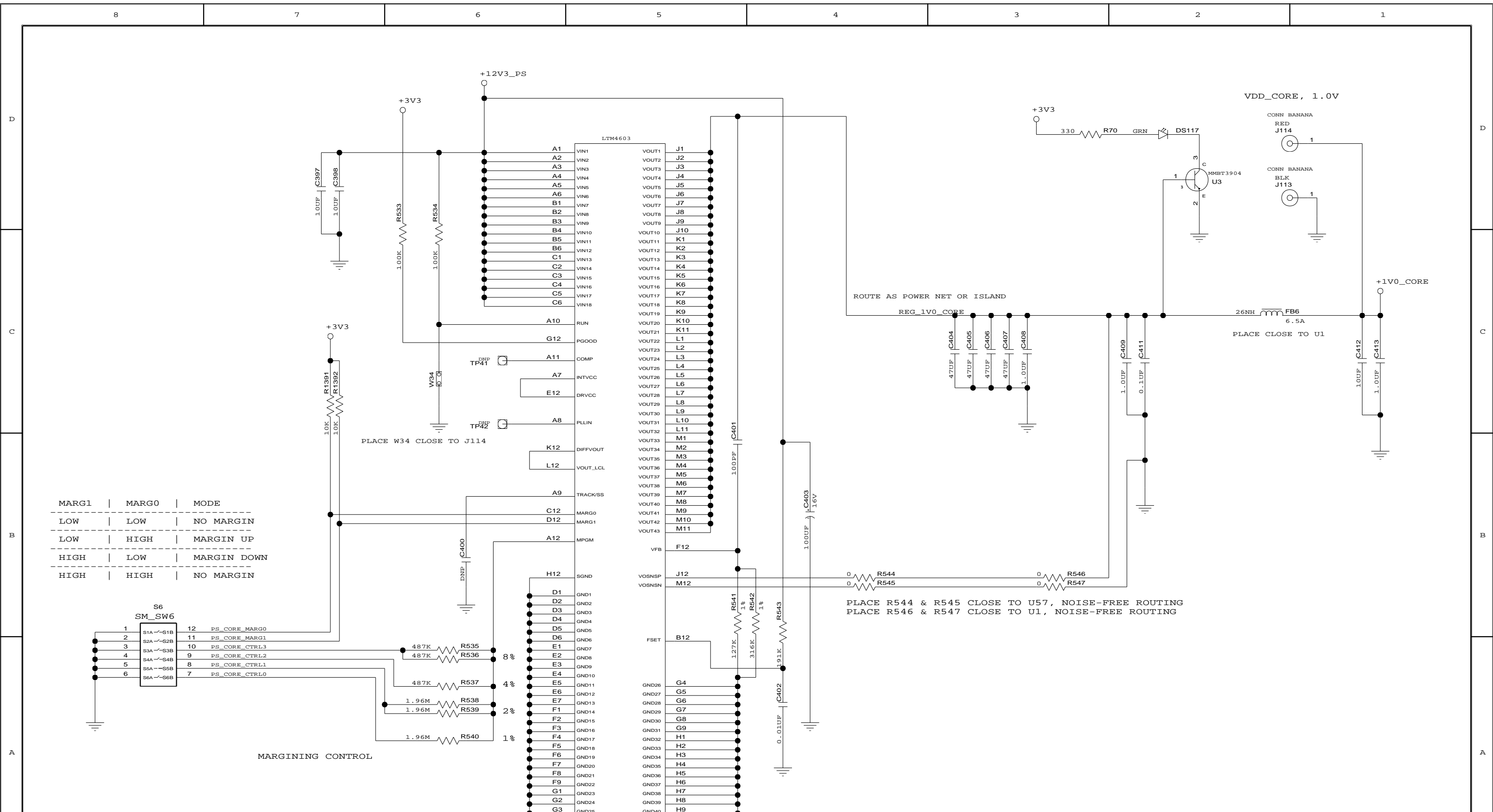
PLACE R526 & R527 CLOSE TO U57, NOISE-FREE ROUTING
 PLACE R528 & R529 CLOSE TO U1, NOISE-FREE ROUTING


TITLE EB-LOGAN-19

POWER REGULATOR - VDDIO

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:50 2010			SHEET 23 OF 41

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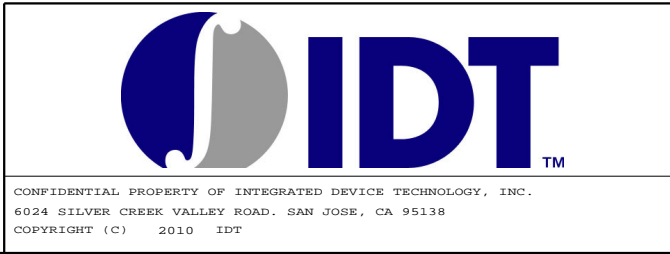
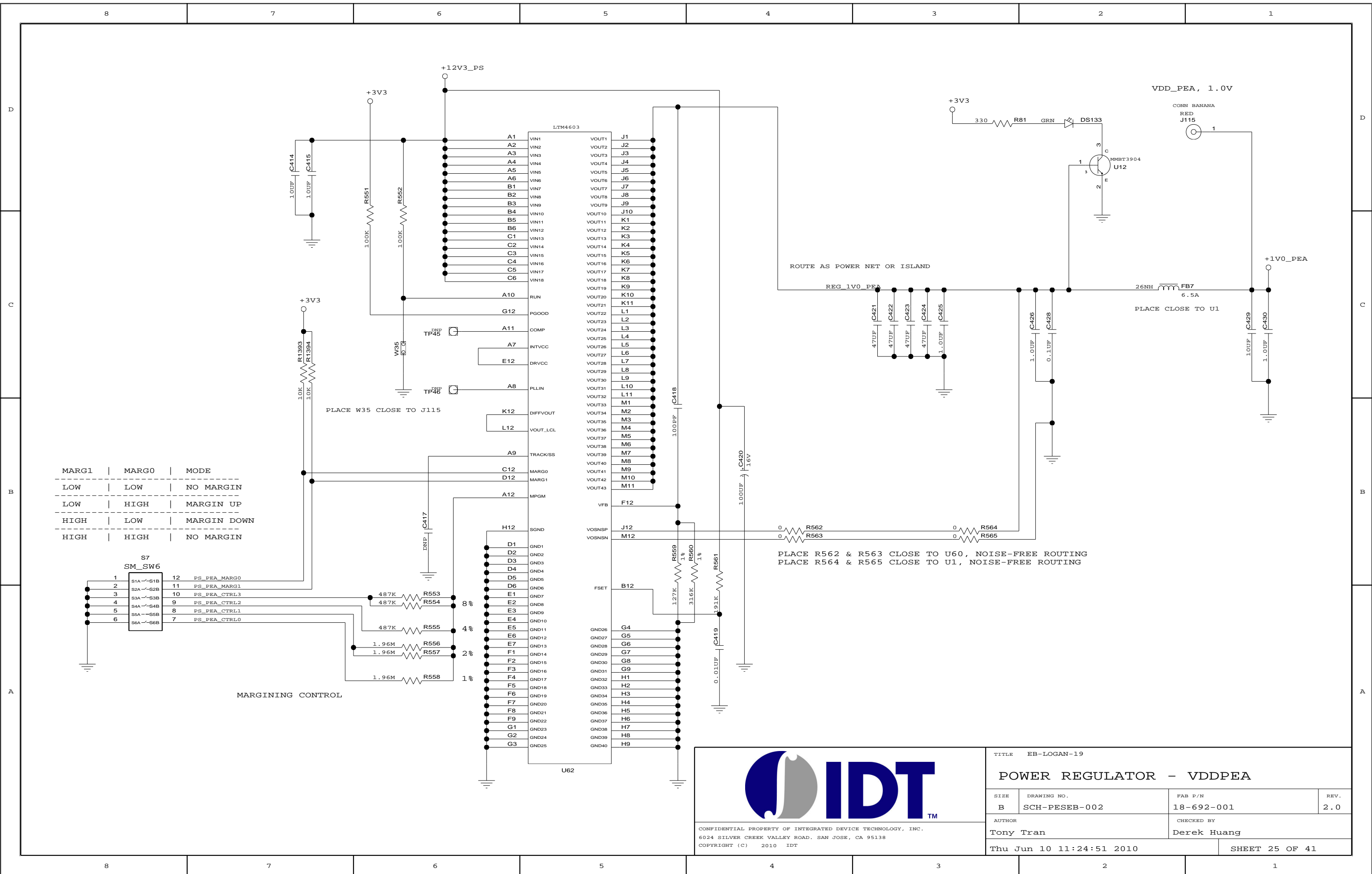


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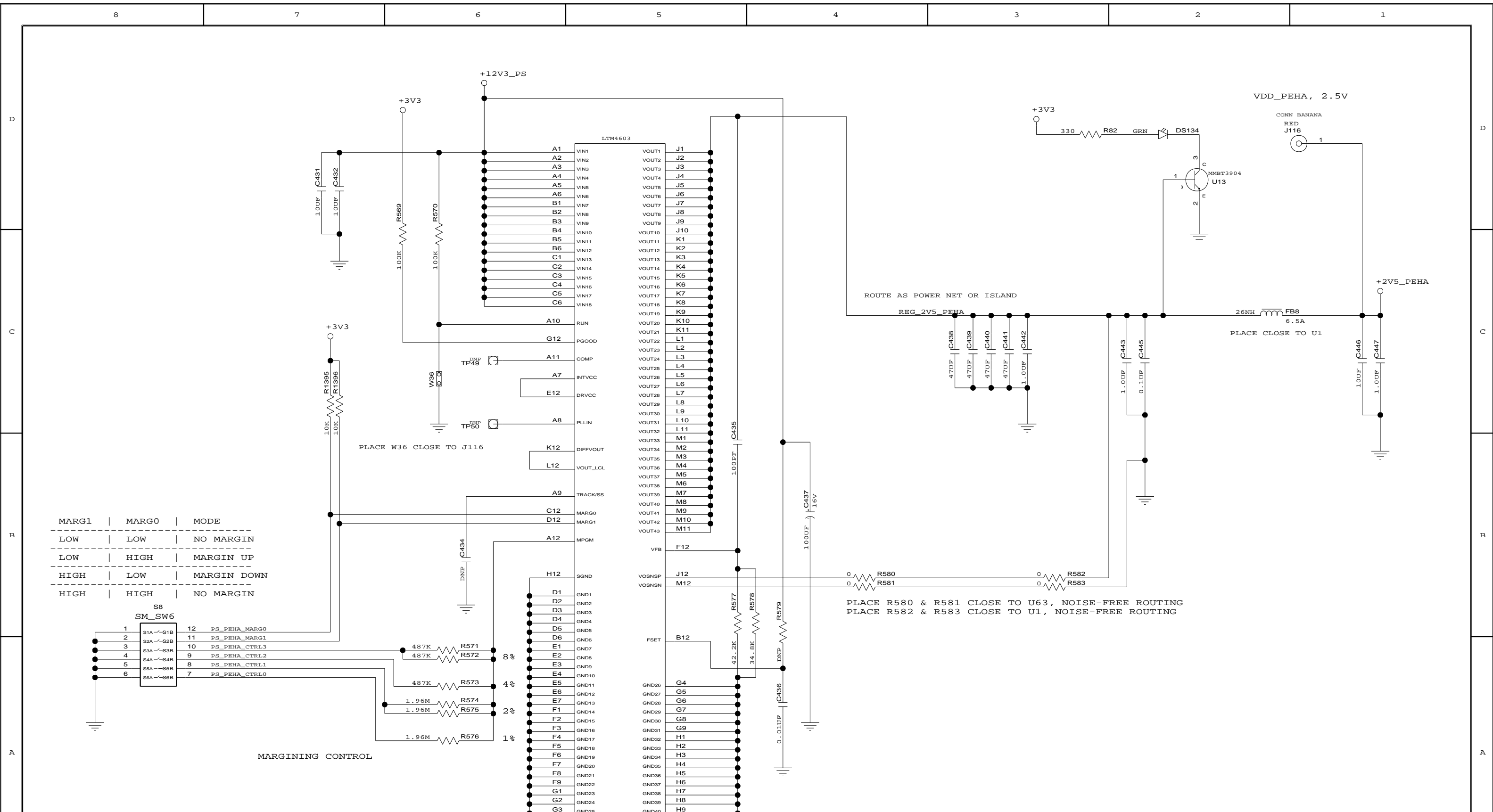
TITLE EB-LOGAN-19

POWER REGULATOR - VDDCORE

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:51 2010			SHEET 24 OF 41

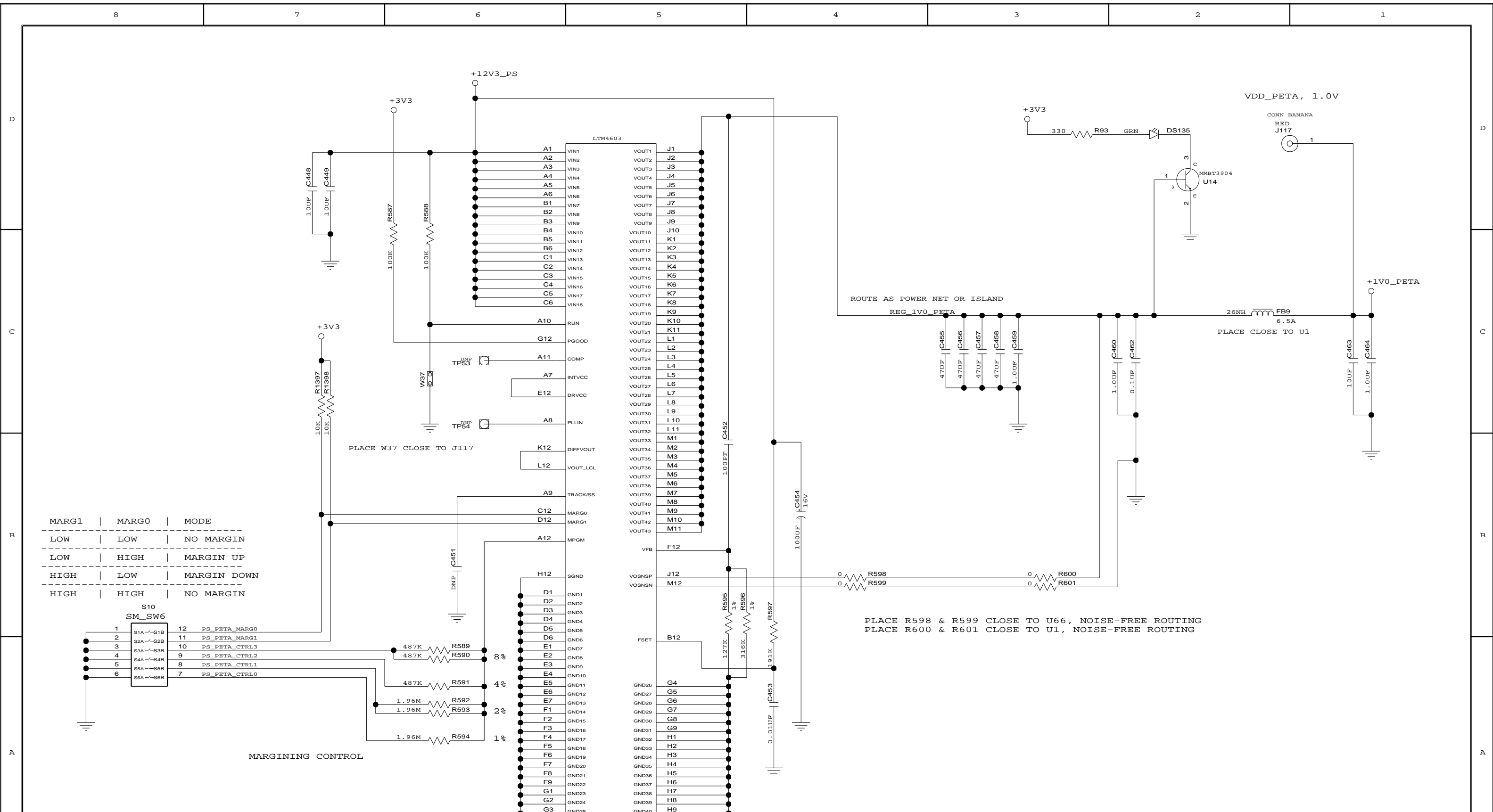


TITLE EB-LOGAN-19			
POWER REGULATOR - VDDPEA			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:51 2010			SHEET 25 OF 41




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TITLE EB-LOGAN-19			
POWER REGULATOR - VDDPEHA			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:51 2010			SHEET 26 OF 41



MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

MARGINING CONTROL

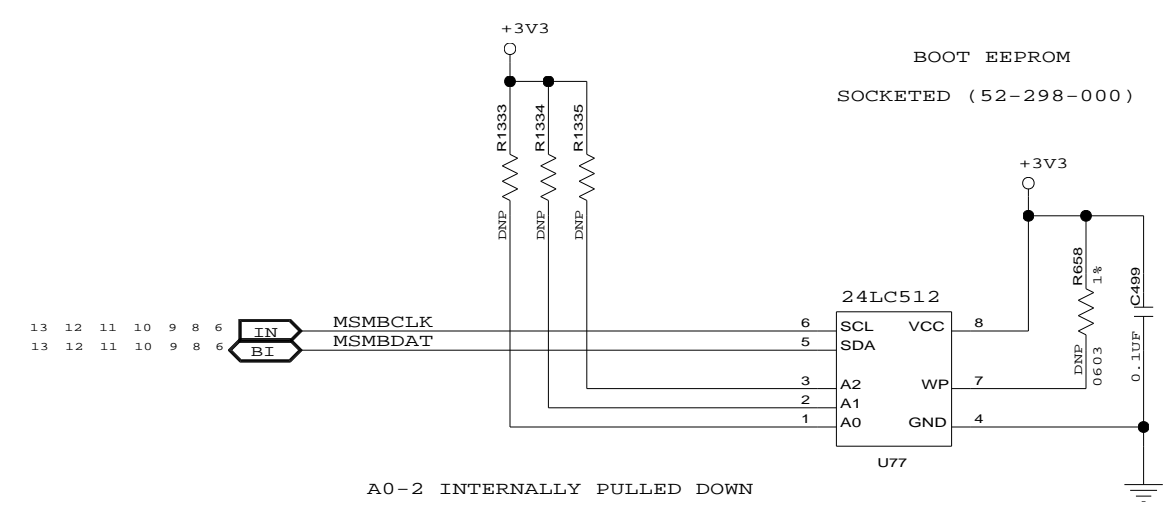
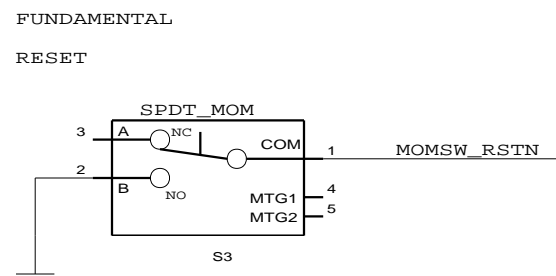
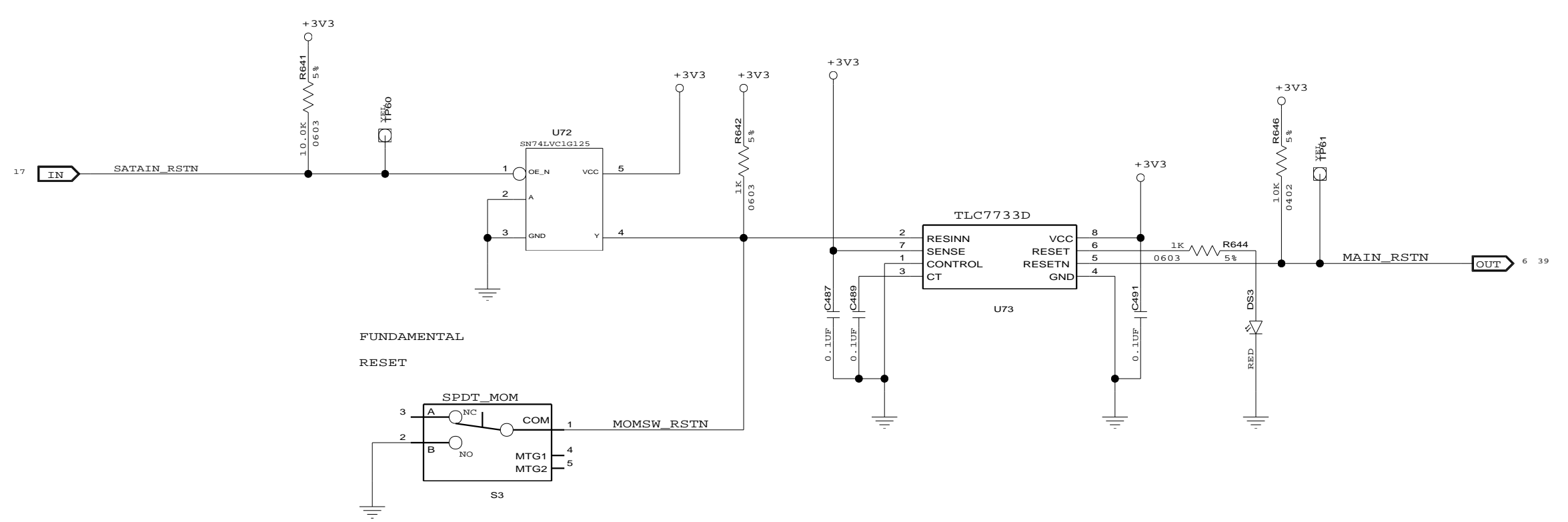


TITLE EB-LOGAN-19

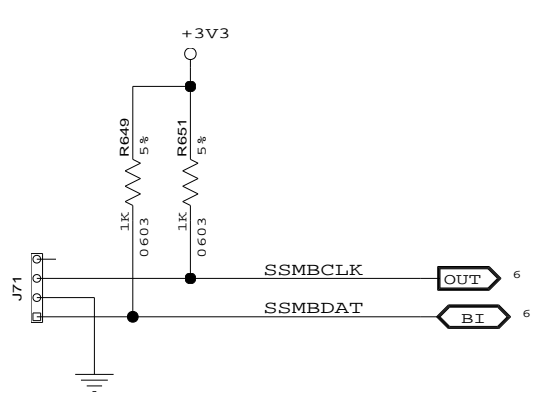
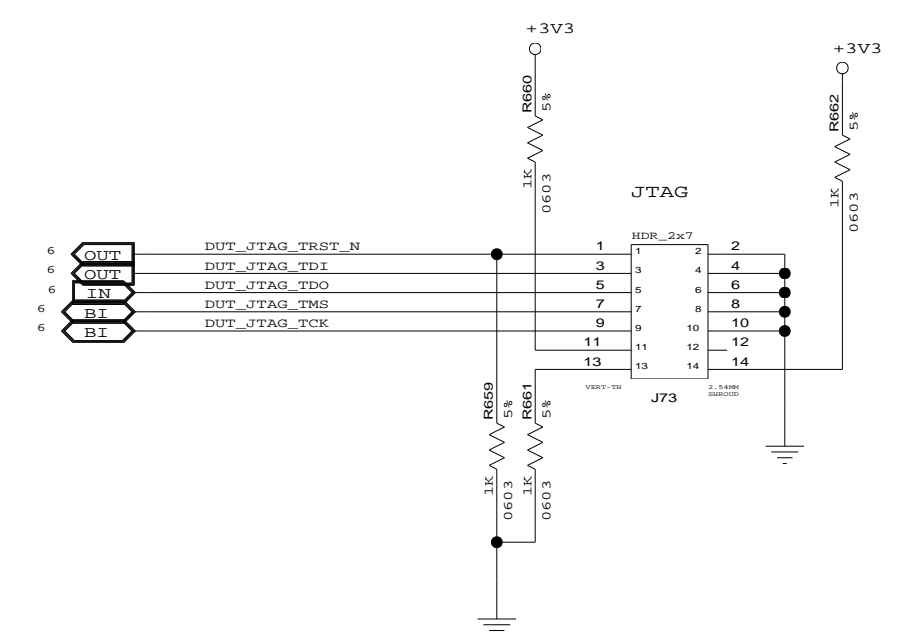
POWER REGULATOR - VDDPETA

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:52 2010			SHEET 27 OF 41

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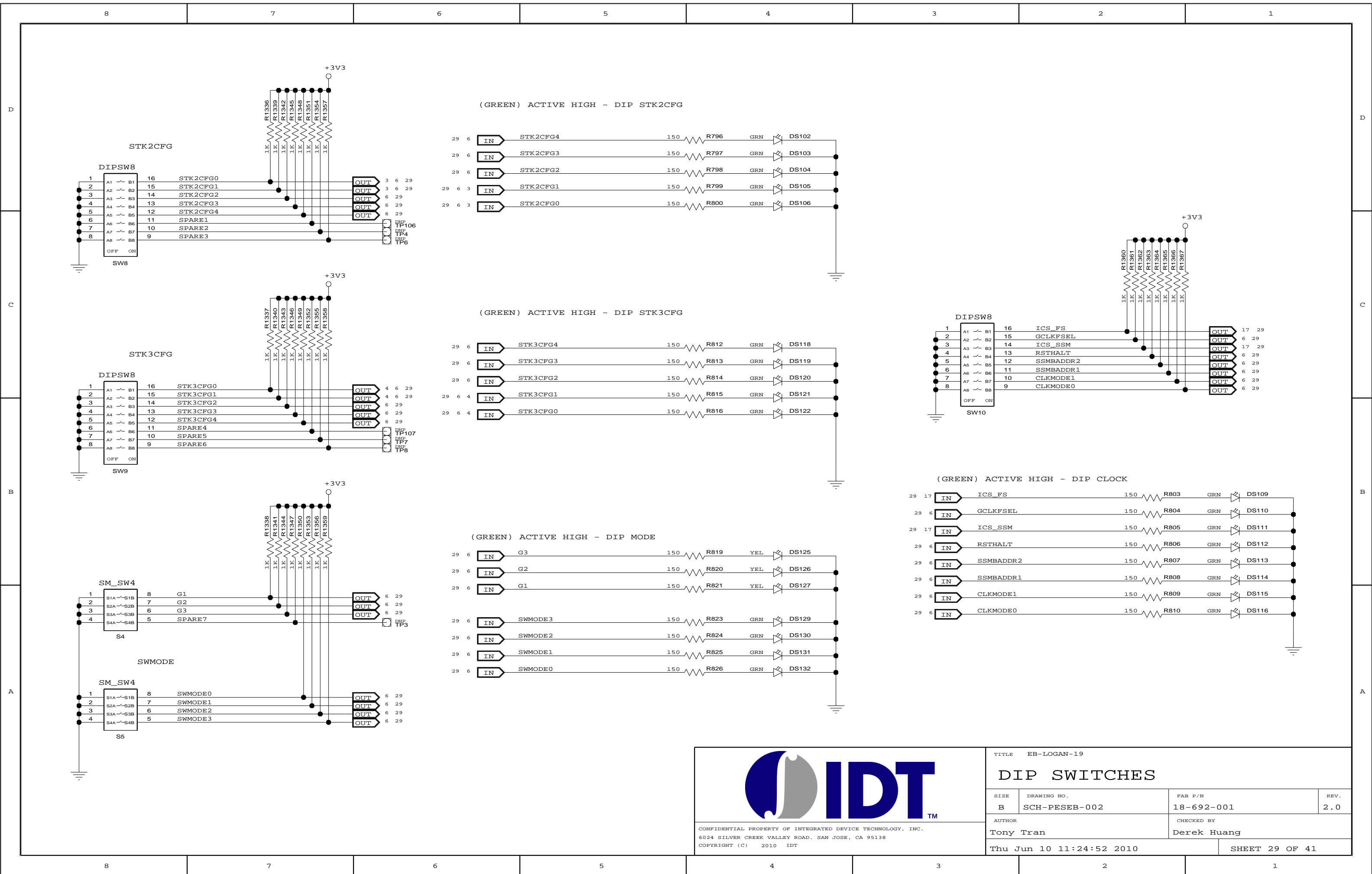



A0-2 INTERNALLY PULLED DOWN



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TITLE EB-LOGAN-19			
RESET, SMBUS, EEPROM, JTAG			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:52 2010			SHEET 28 OF 41



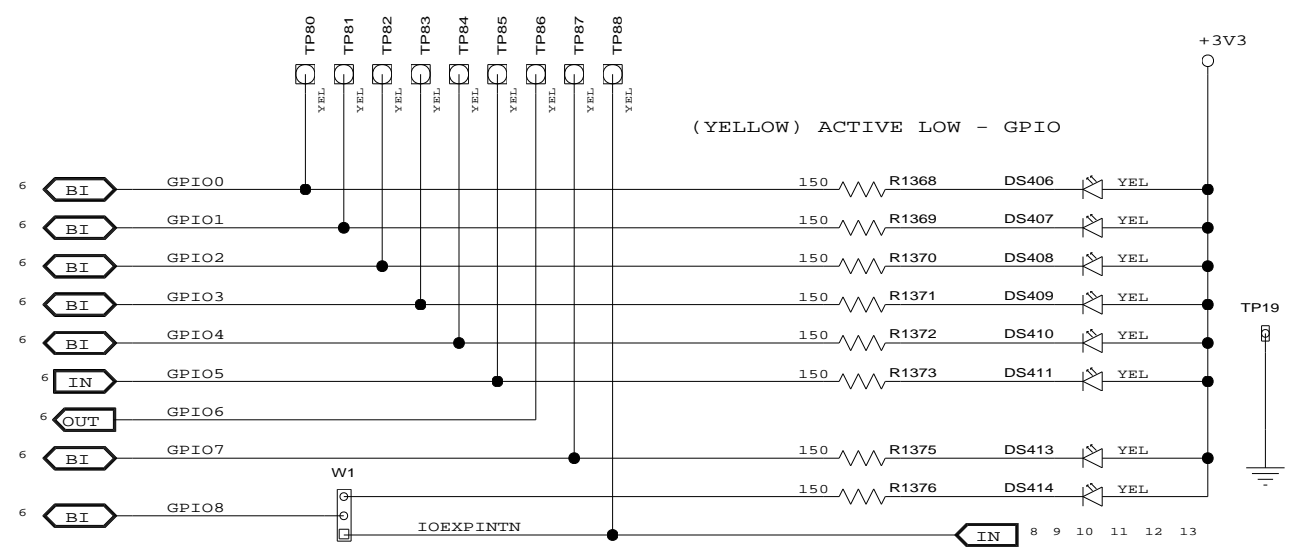


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TITLE EB-LOGAN-19

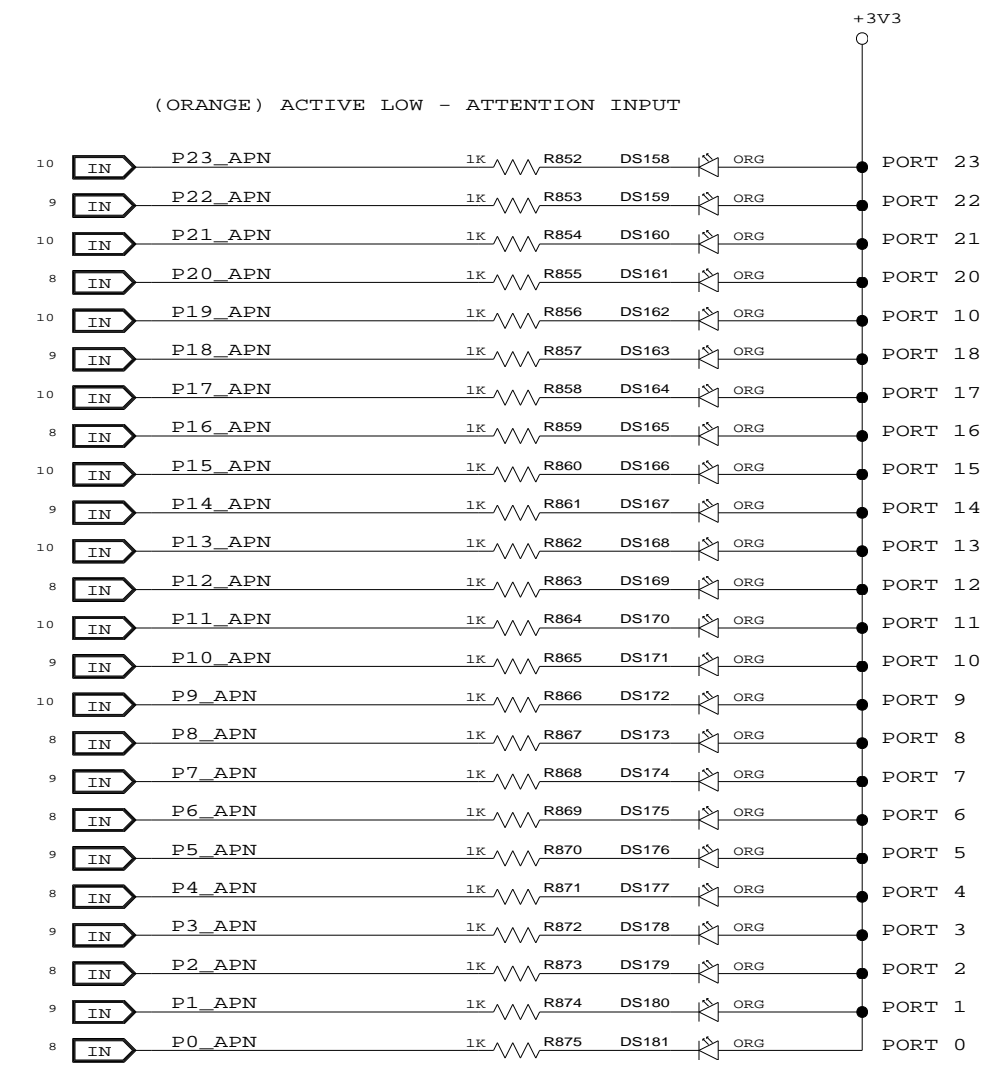
DIP SWITCHES

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:52 2010			SHEET 29 OF 41

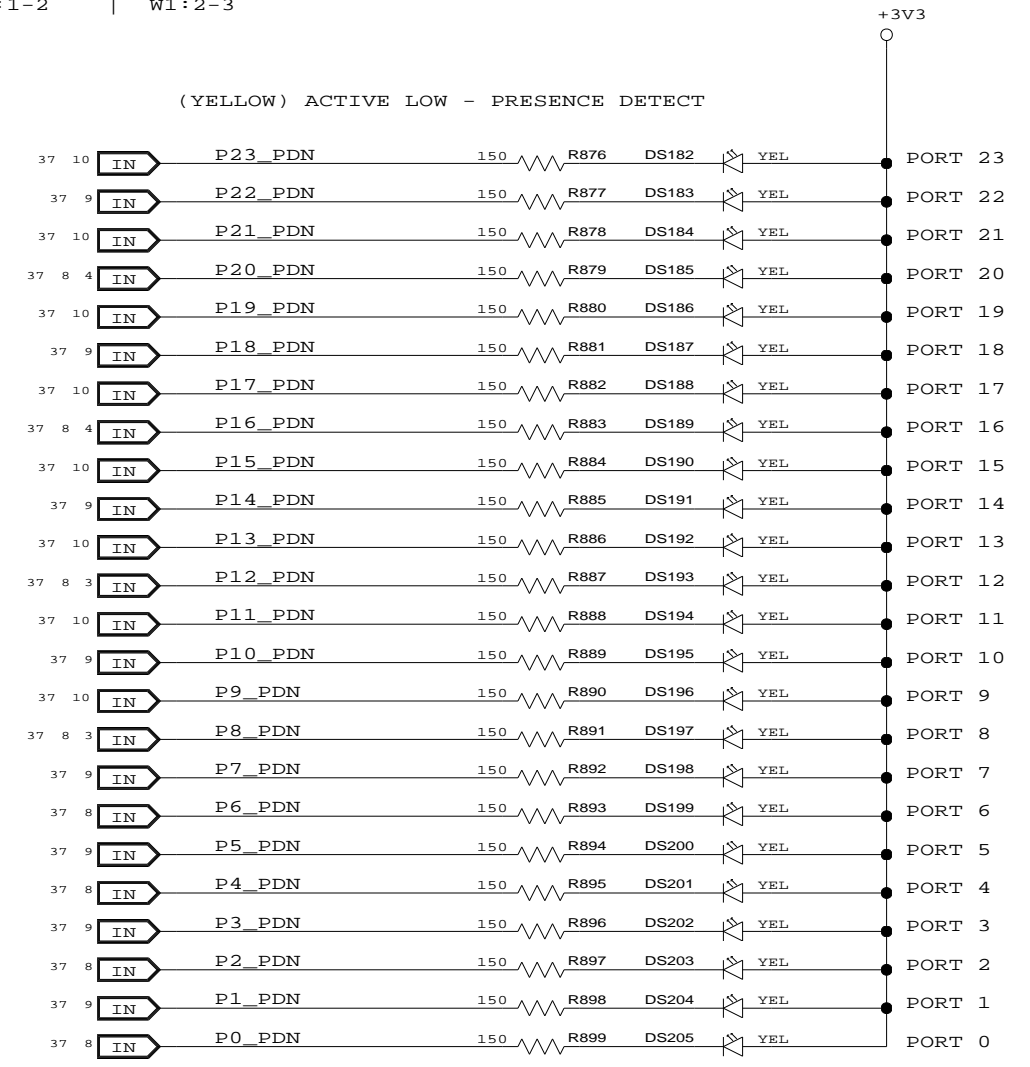


GPIO	ALT0	ALT1
0	PART0PERSTN	P16LINKUPN
1	PART1PERSTN	P16ACTIVEN
2	PART2PERSTN	P4LINKUPN
3	PART3PERSTN	P4ACTIVEN
4	FAILOVER0	P0LINKUPN
5	GPEN	P0ACTIVEN
6	FAILOVER1	FAILOVER3
7	FAILOVER2	P8LINKUPN
8	IOEXPINTN W1:1-2	P8ACTIVEN W1:2-3

(ORANGE) ACTIVE LOW - ATTENTION INPUT



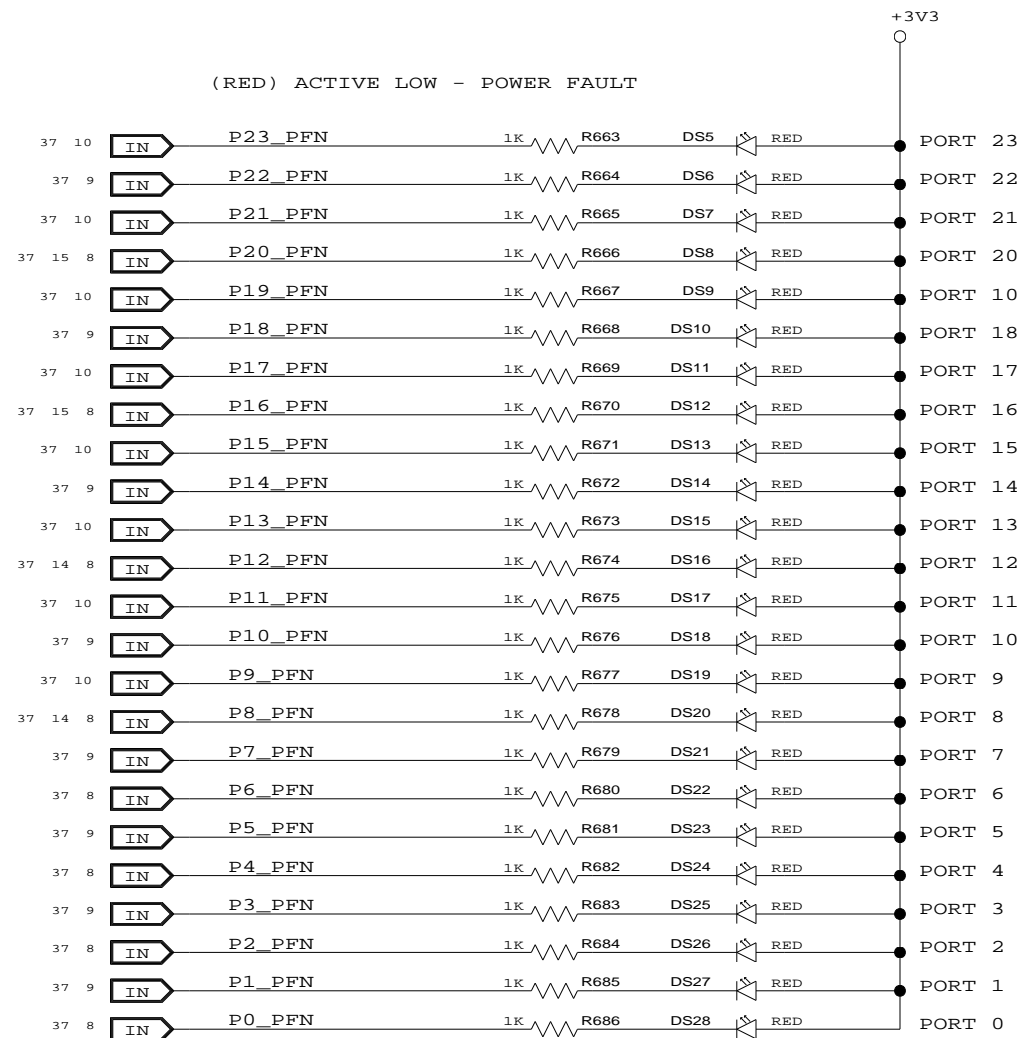
(YELLOW) ACTIVE LOW - PRESENCE DETECT



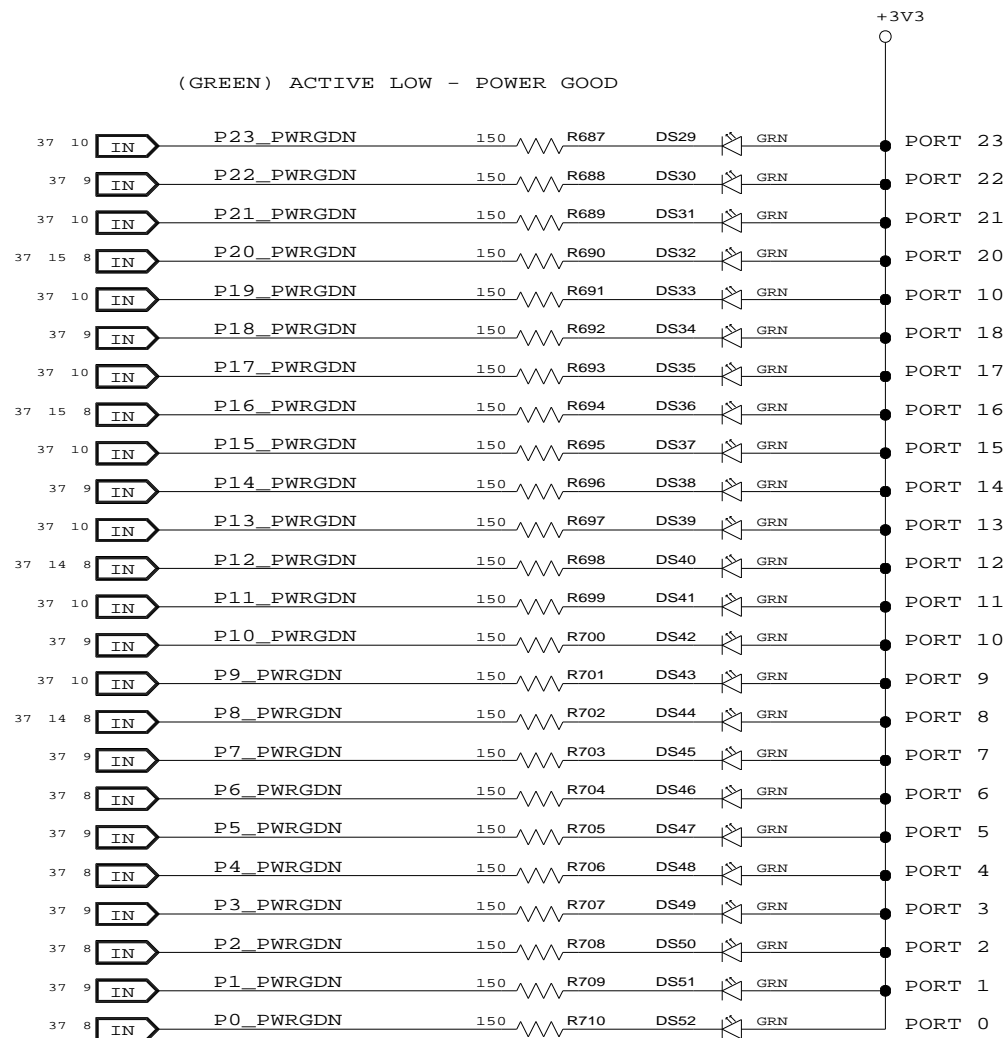
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TITLE EB-LOGAN-19			
LED - PORT STATUS (1 OF 7)			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:53 2010			SHEET 30 OF 41

(RED) ACTIVE LOW - POWER FAULT



(GREEN) ACTIVE LOW - POWER GOOD

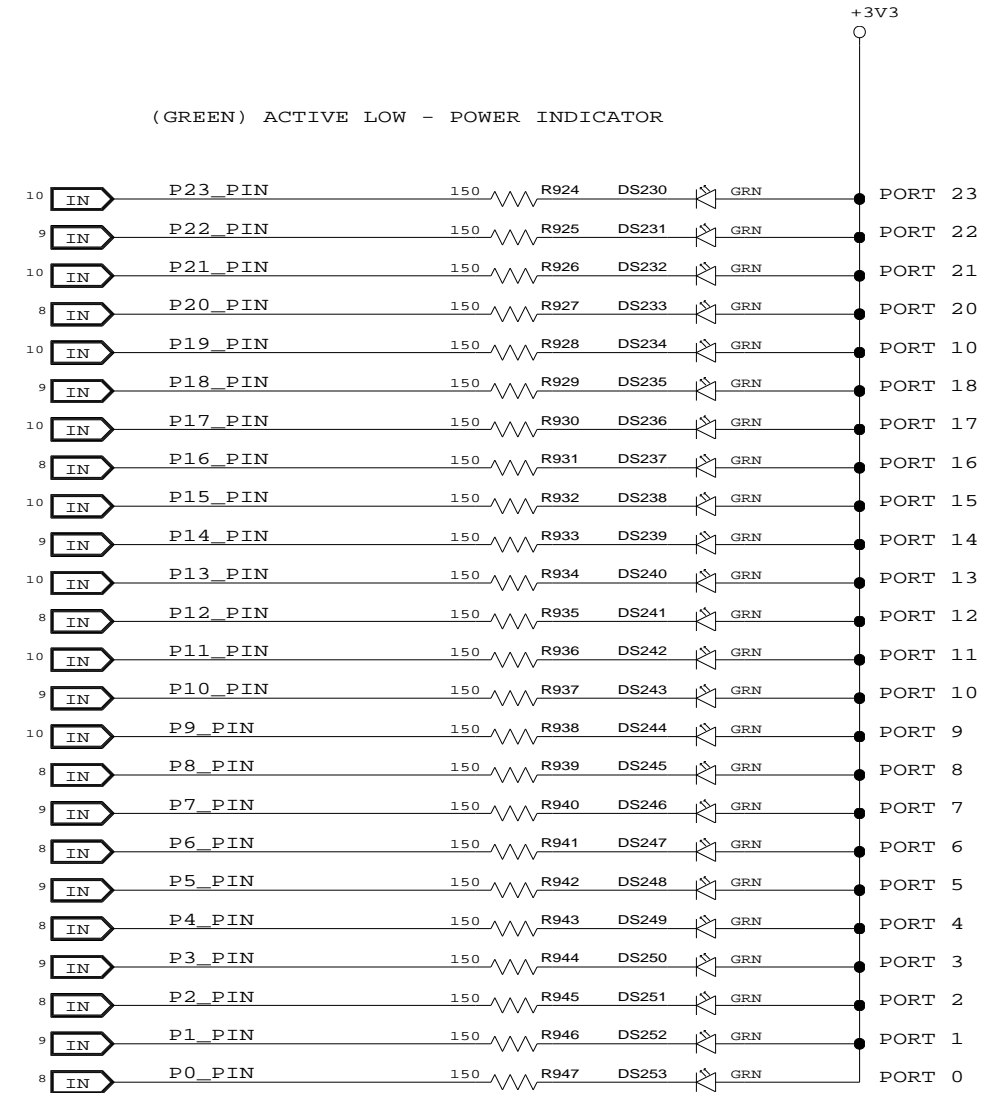
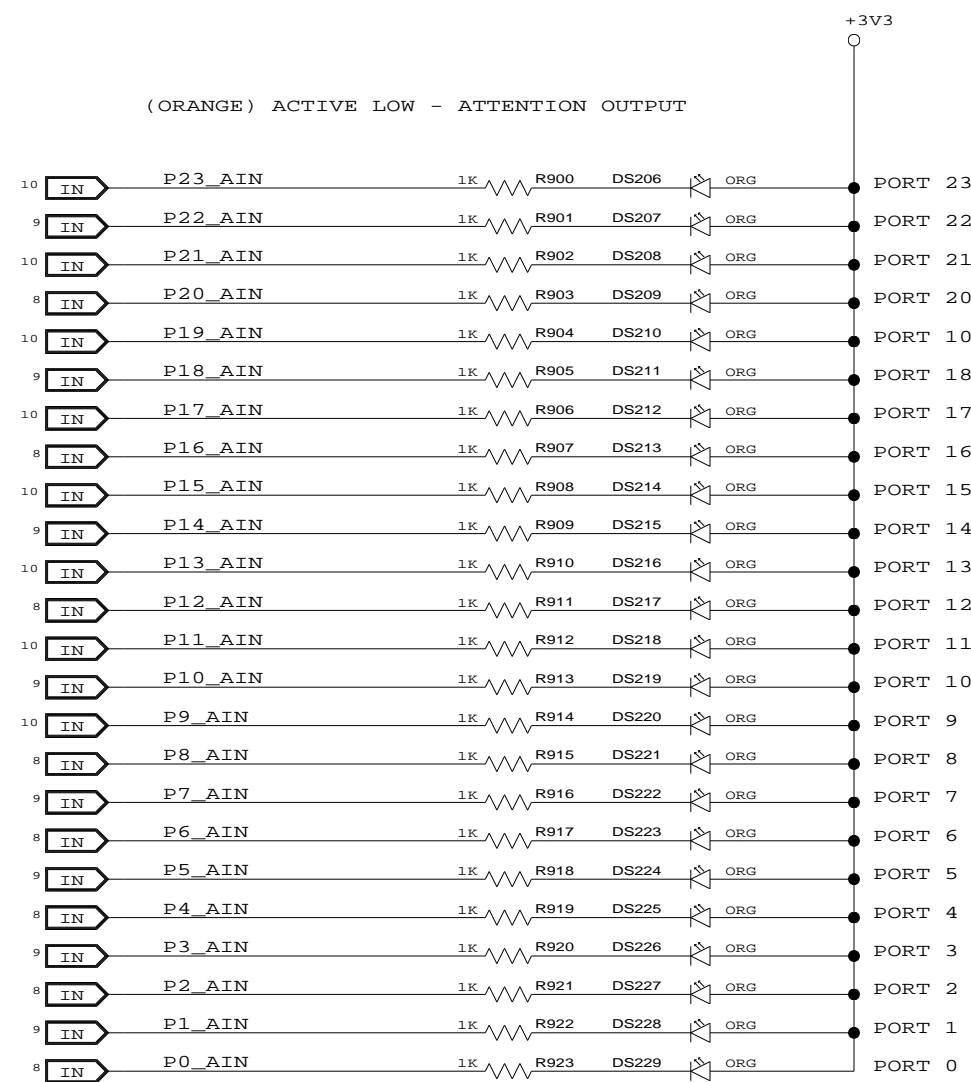


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TITLE EB-LOGAN-19

LED - PORT STATUS (2 OF 7)

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:53 2010			SHEET 31 OF 41



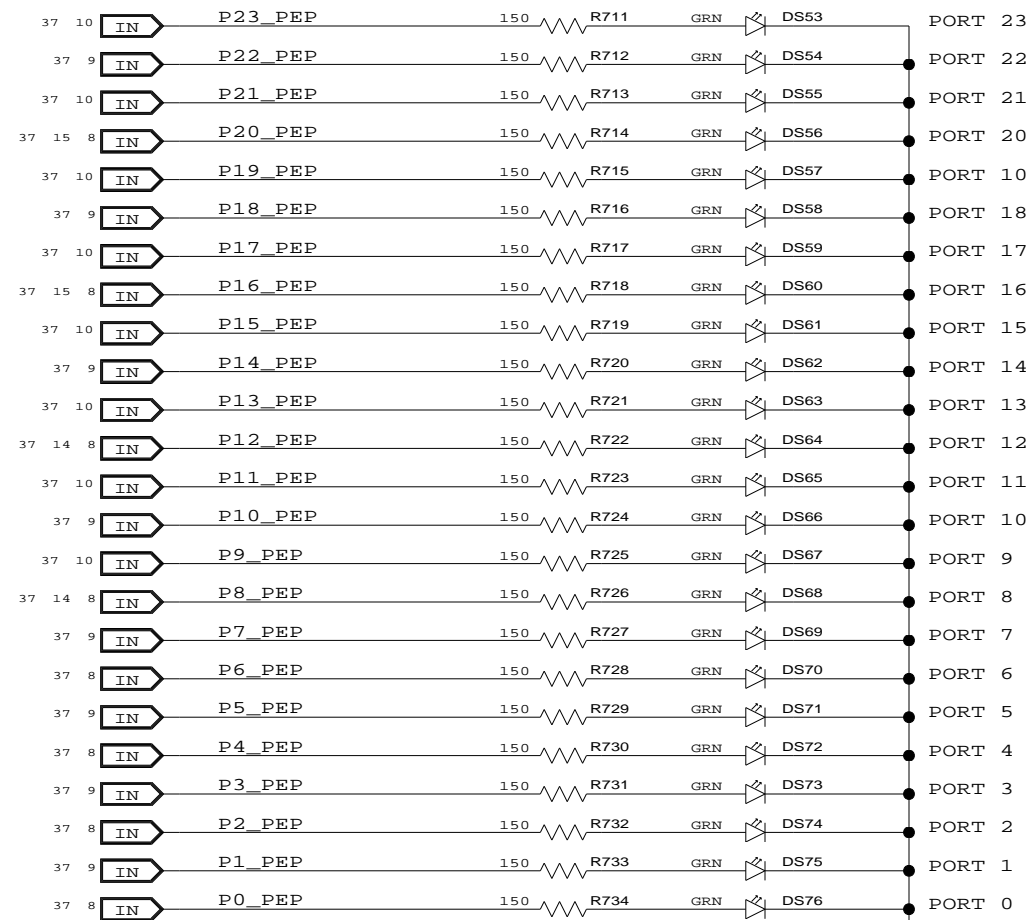
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TITLE EB-LOGAN-19

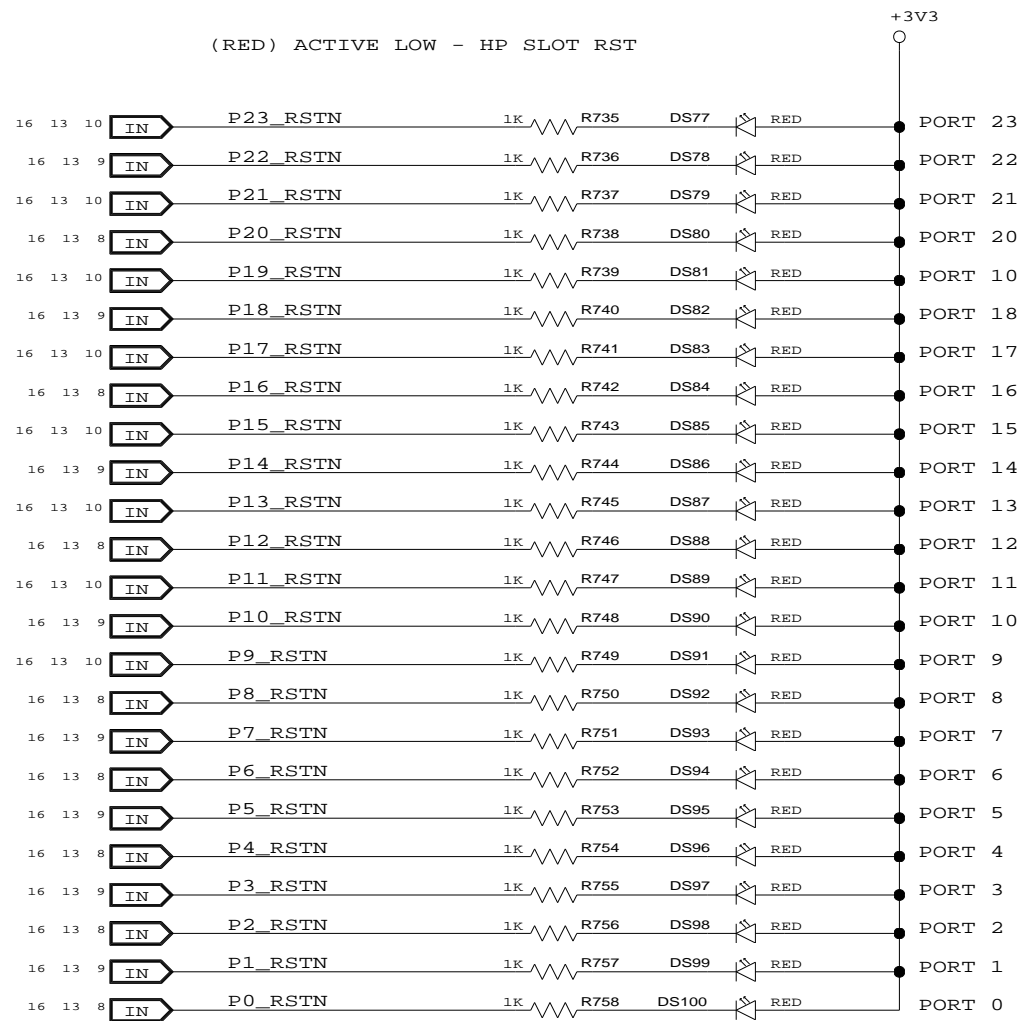
LED - PORT STATUS (3 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:53 2010			SHEET 32 OF 41

(GREEN) ACTIVE HIGH - POWER ENABLE



(RED) ACTIVE LOW - HP SLOT RST



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TITLE EB-LOGAN-19

LED - PORT STATUS (4 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:54 2010			SHEET 33 OF 41

8

7

6

5

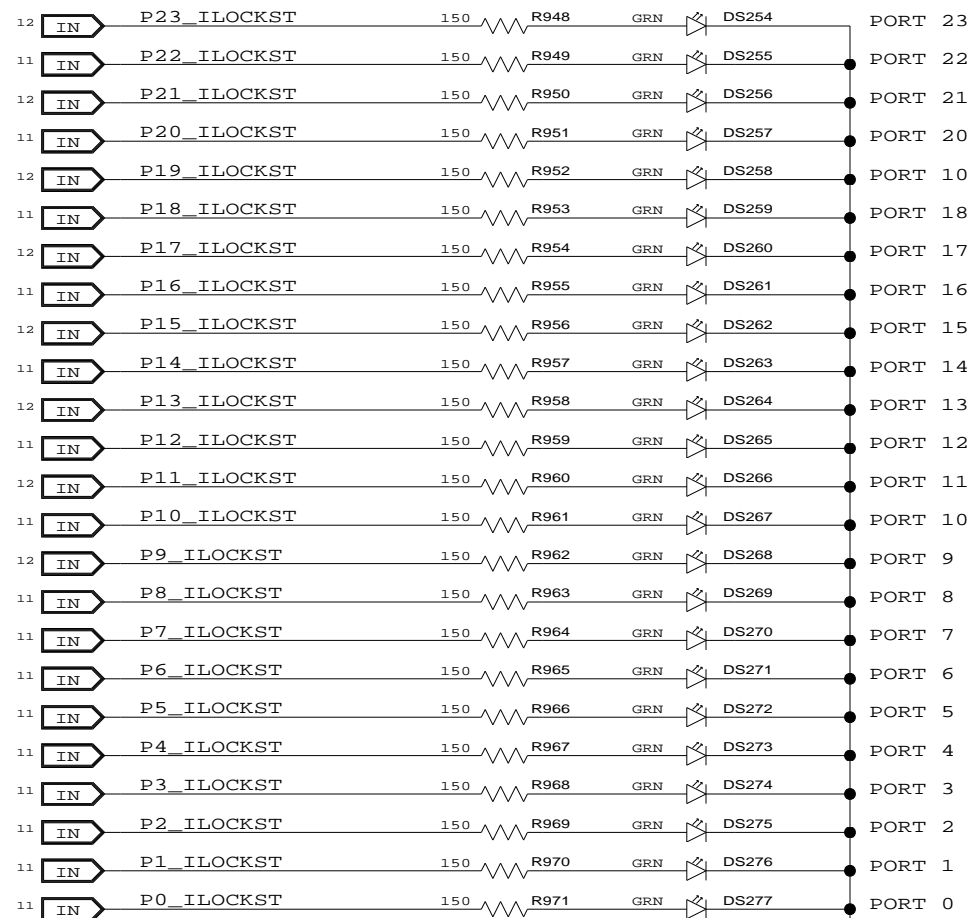
4

3

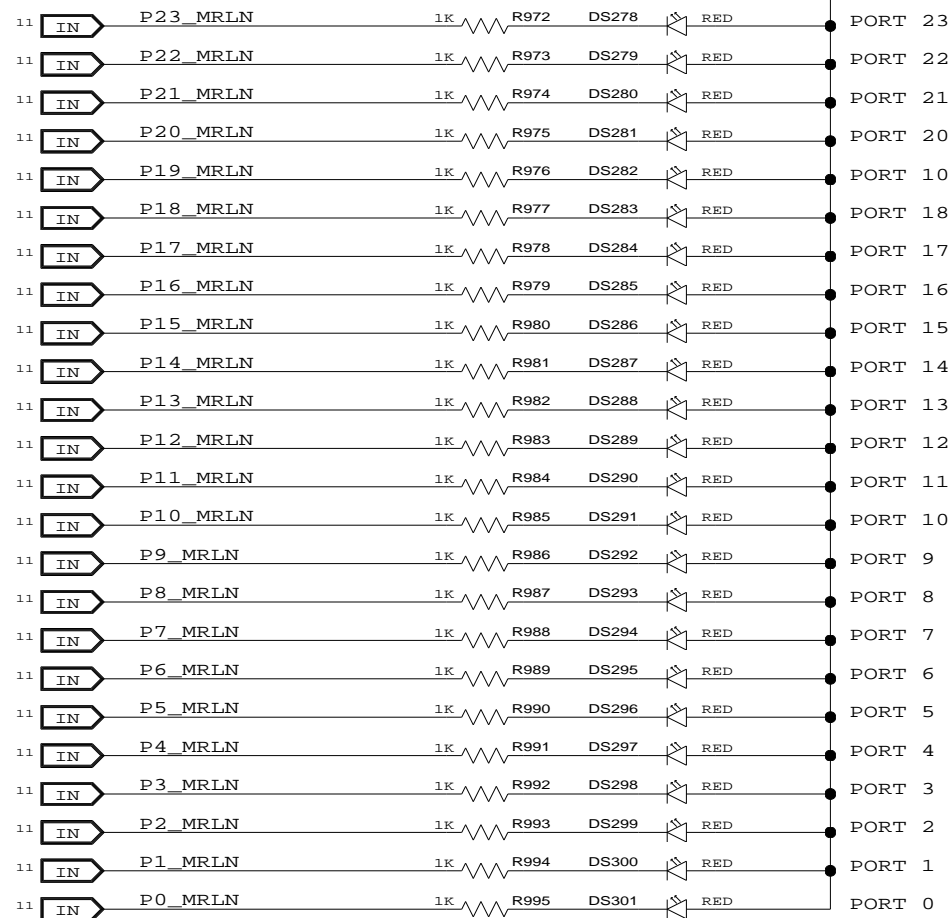
2

1

(GREEN) ACTIVE HIGH - INTERLOCK INPUT



(RED) ACTIVE LOW - MRL



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TITLE EB-LOGAN-19

LED - PORT STATUS (5 OF 7)

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
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AUTHOR Tony Tran	CHECKED BY Derek Huang
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Thu Jun 10 11:24:54 2010

SHEET 34 OF 41

8

7

6

5

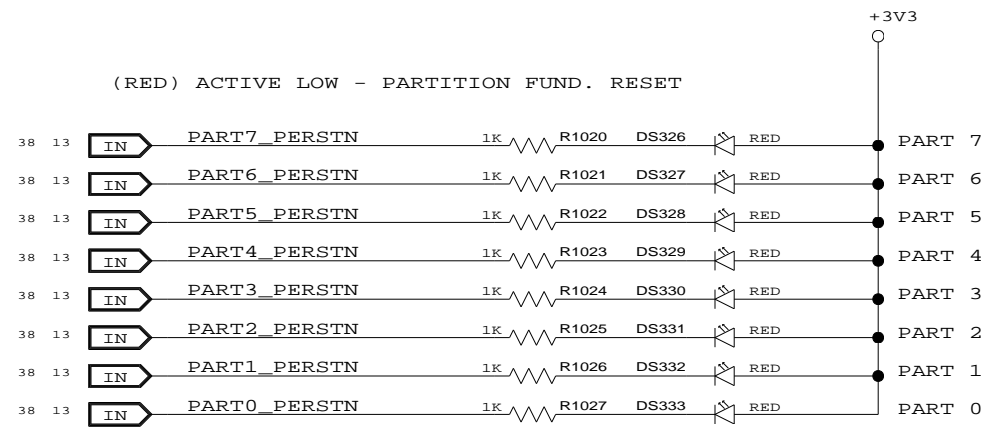
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3

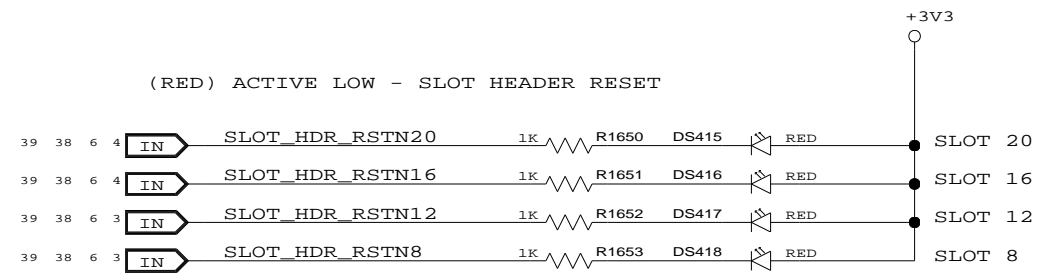
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1

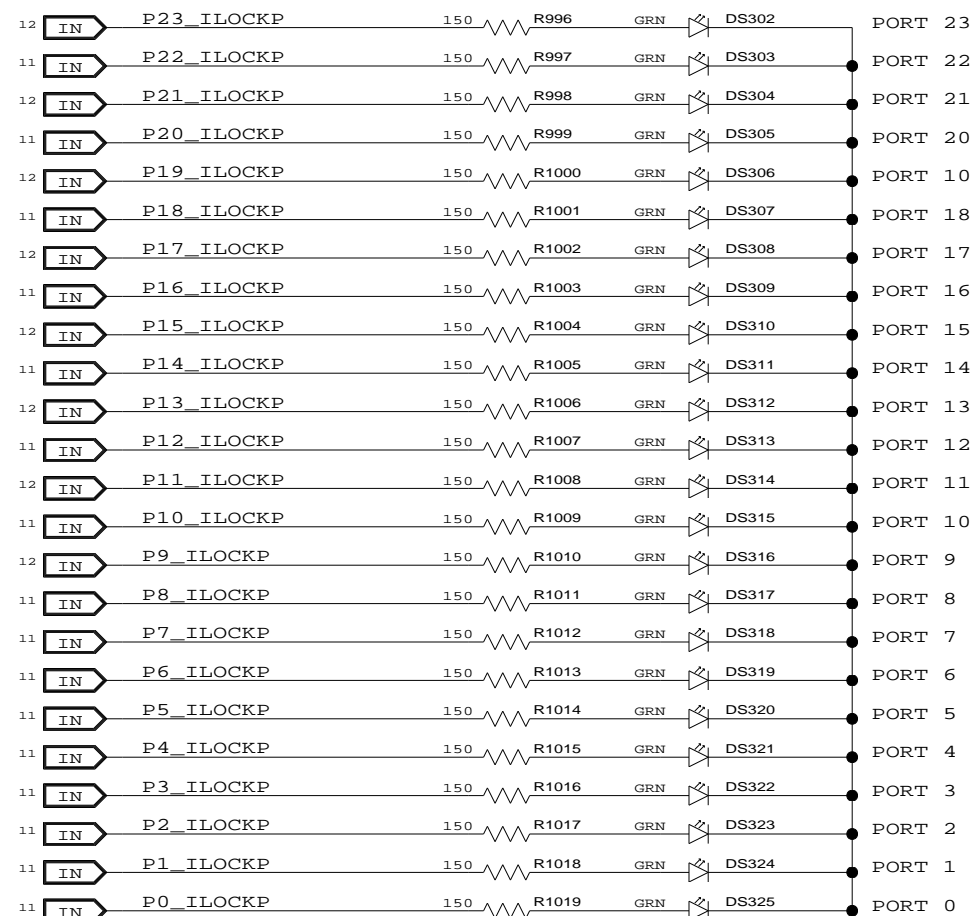
(RED) ACTIVE LOW - PARTITION FUND. RESET



(RED) ACTIVE LOW - SLOT HEADER RESET



(GREEN) ACTIVE HIGH - INTERLOCK OUTPUT



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TITLE EB-LOGAN-19

LED - PORT STATUS (6 OF 7)

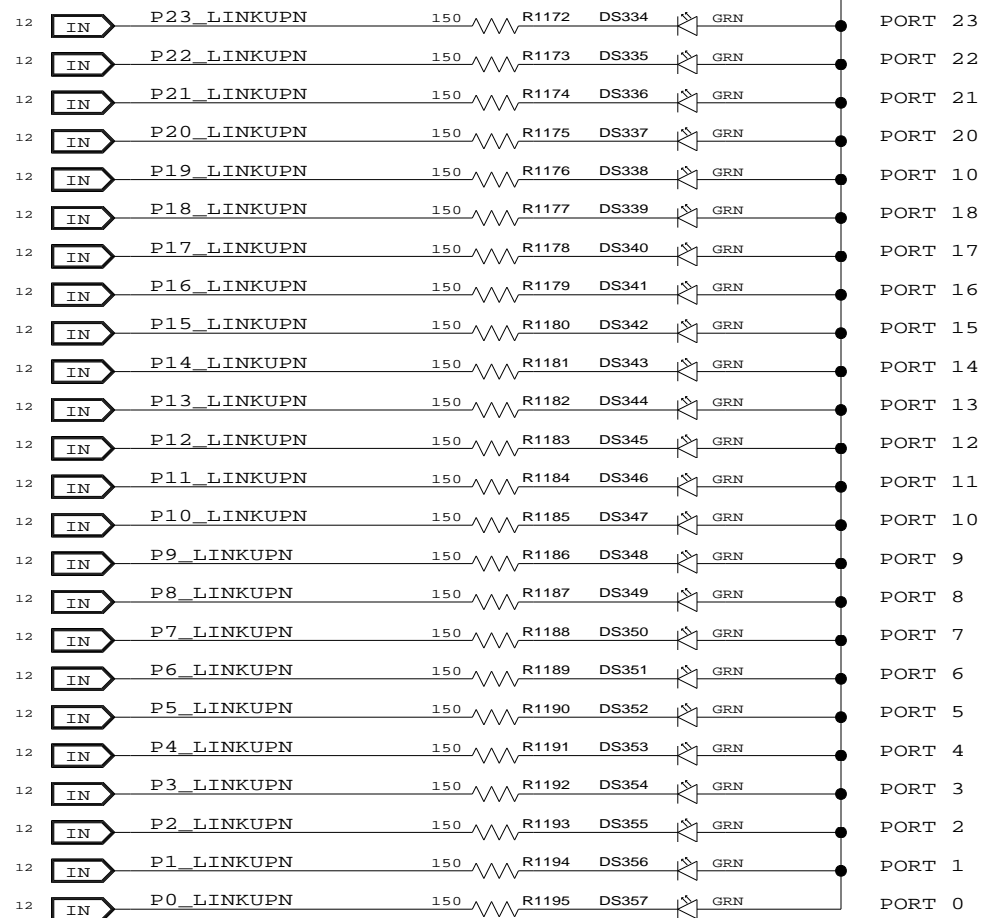
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

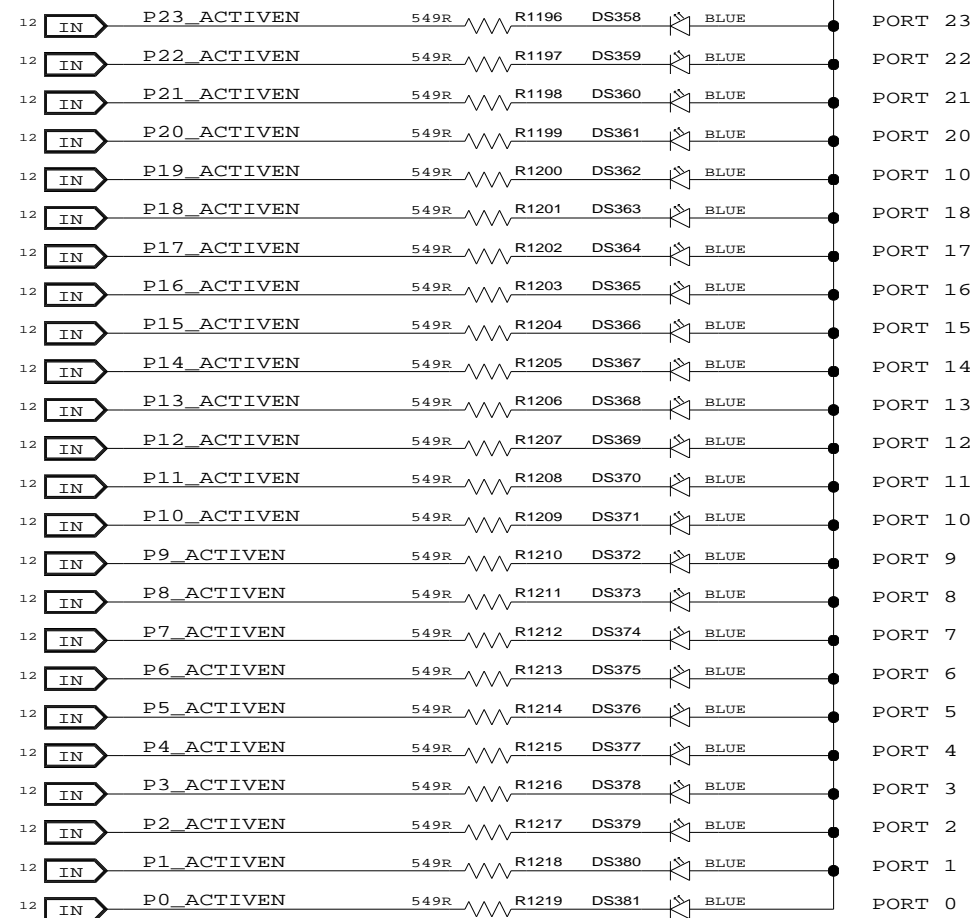
Thu Jun 10 11:24:54 2010

SHEET 35 OF 41

(GREEN) ACTIVE LOW - LINK UP



(BLUE) ACTIVE LOW - LINK ACTIVITY



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TITLE EB-LOGAN-19

LED - PORT STATUS (7 OF 7)

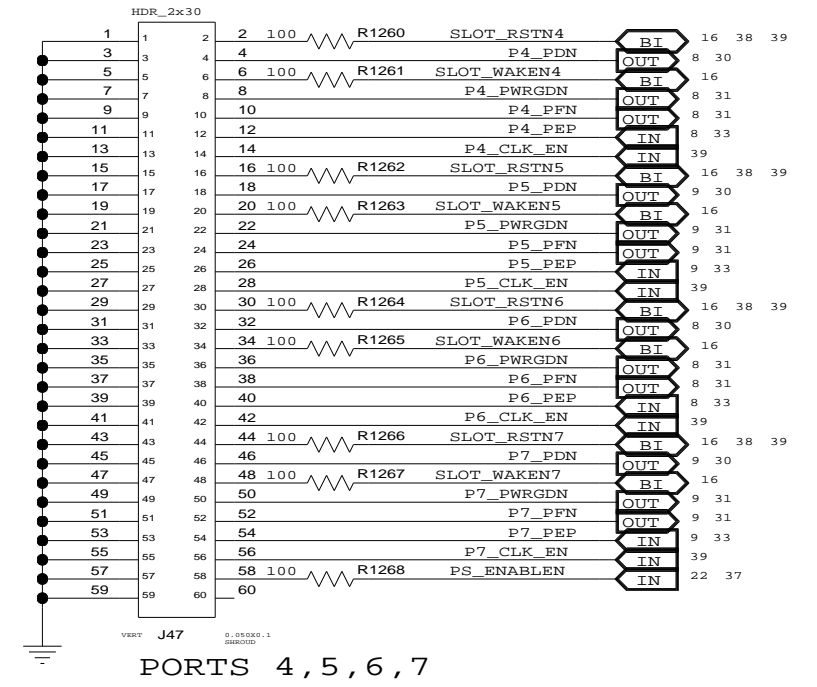
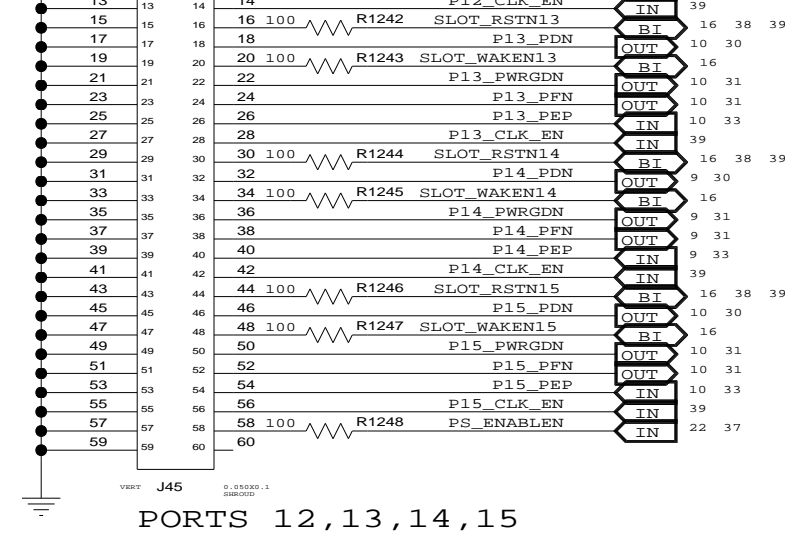
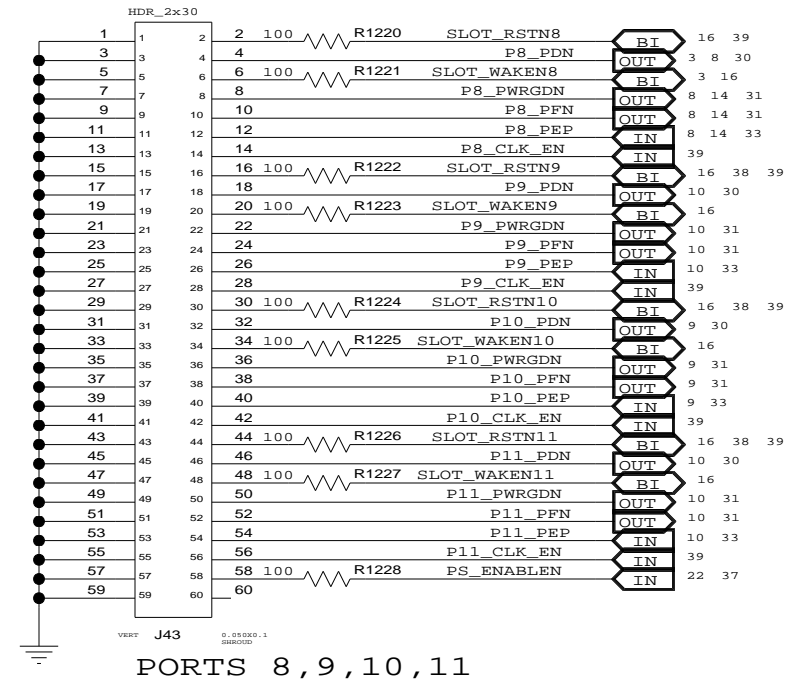
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
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AUTHOR Tony Tran	CHECKED BY Derek Huang
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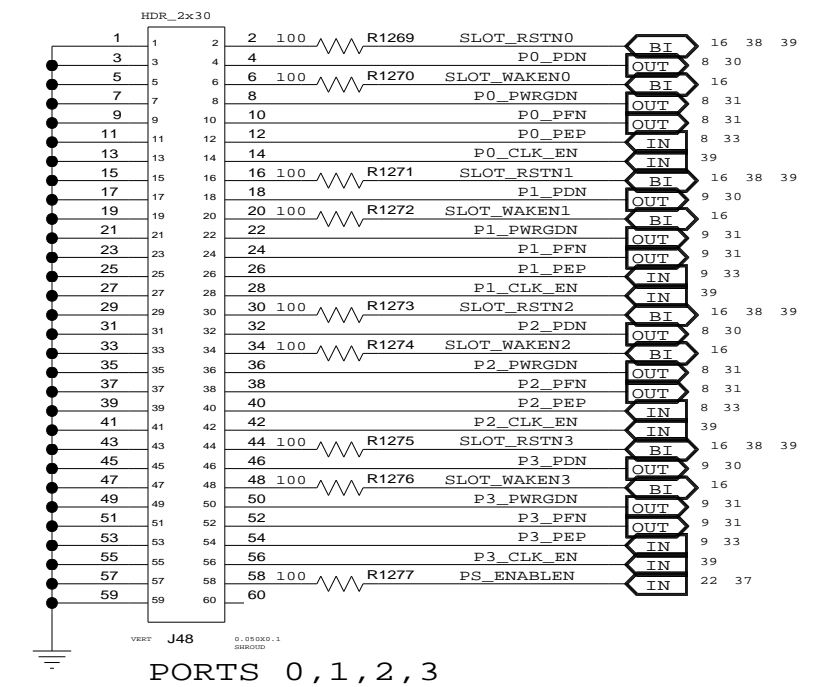
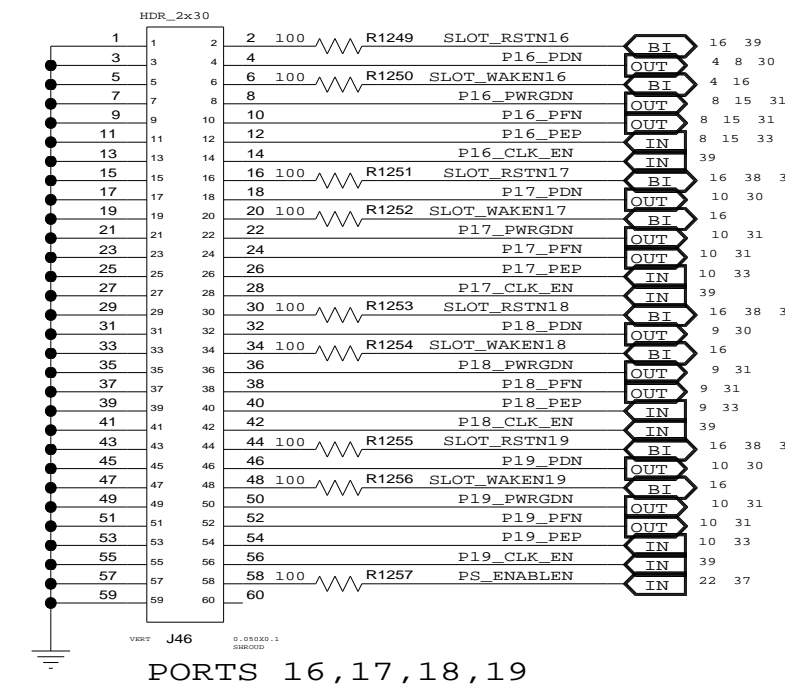
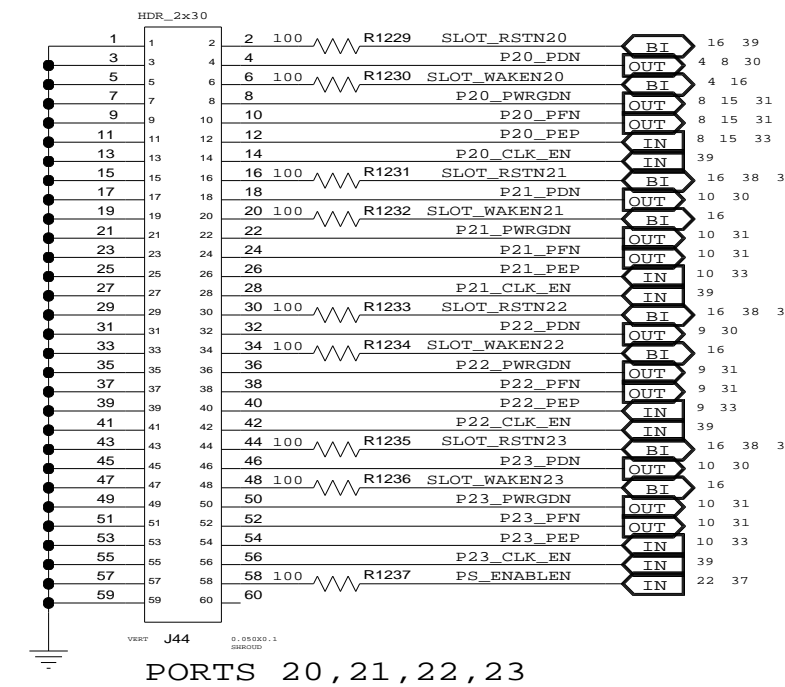
Thu Jun 10 11:24:55 2010

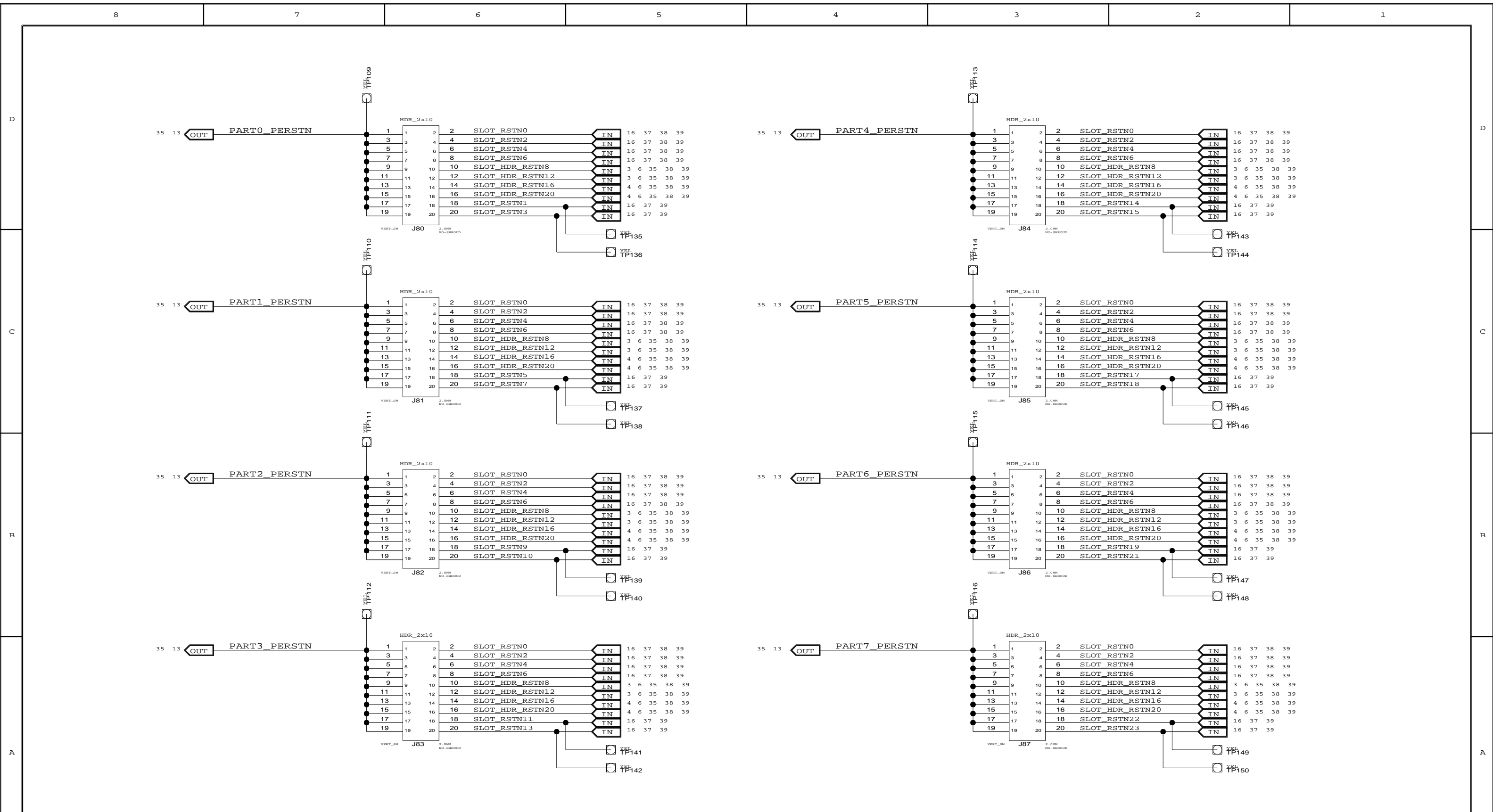
SHEET 36 OF 41


SLOT_RESETN
 CARD_PRESENTN
 WAKEN
 POWERGOOD
 PWR_FLTN
 PWR_ENABLE
 CLOCK_ENABLEN
 PS_ENABLEN
 CABLE SENSE



SLOT_RESETN
 CARD_PRESENTN
 WAKEN
 POWERGOOD
 PWR_FLTN
 PWR_ENABLE
 CLOCK_ENABLEN
 PS_ENABLEN
 CABLE SENSE

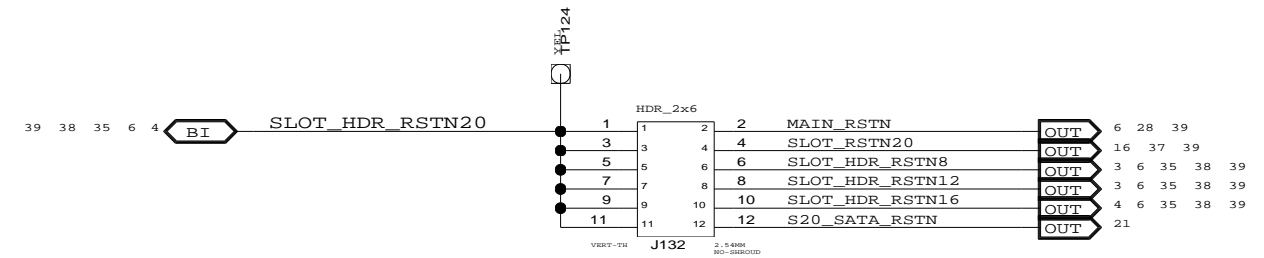
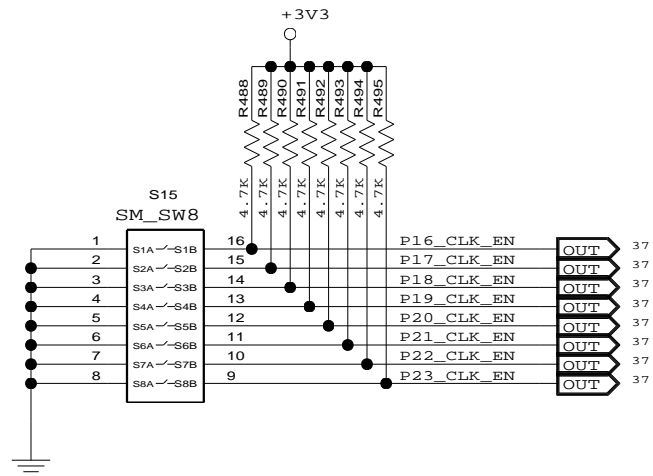
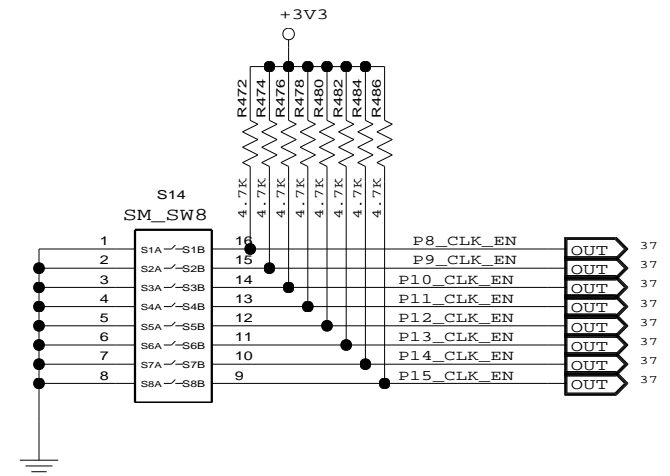
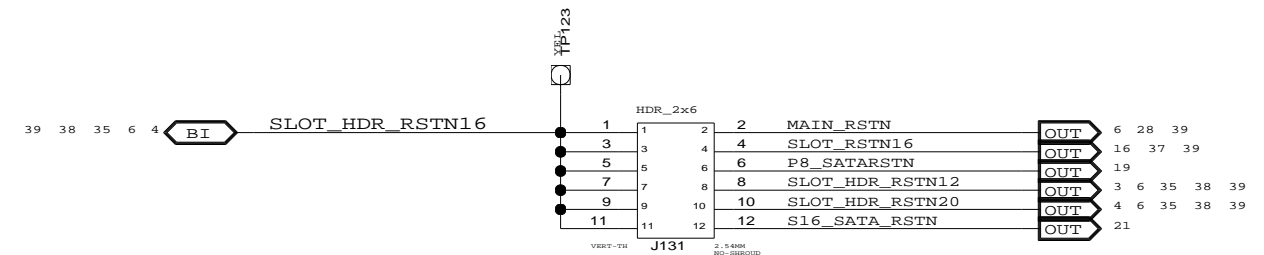
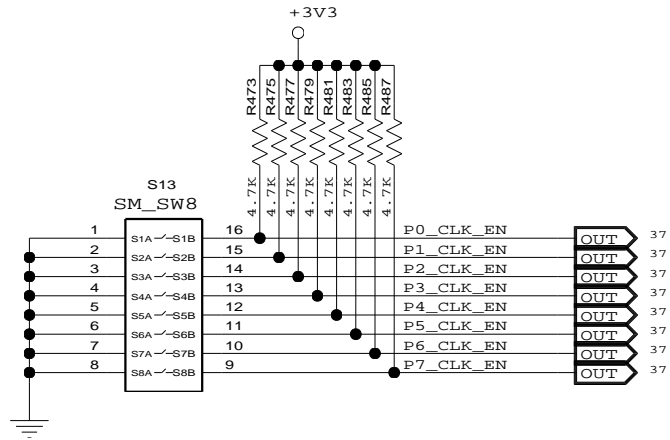
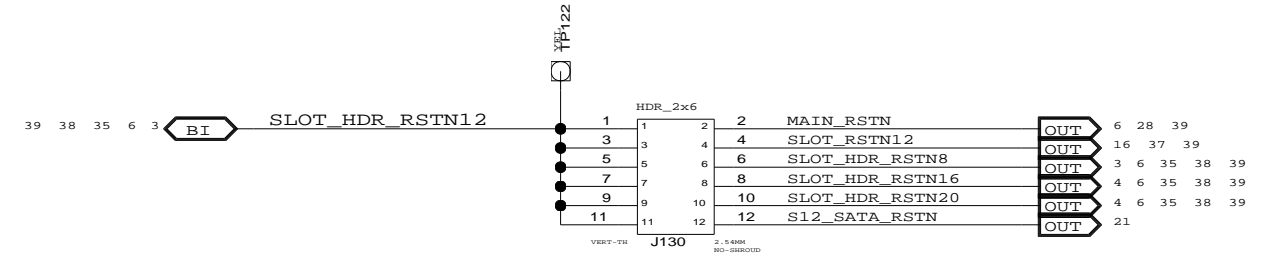
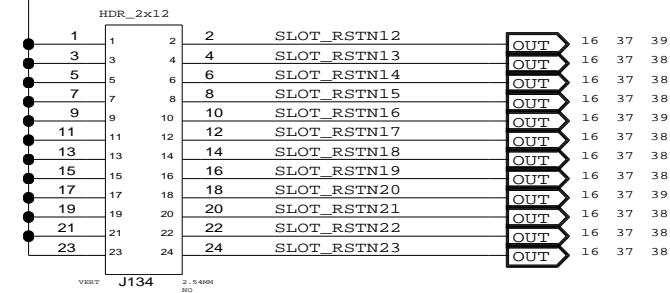
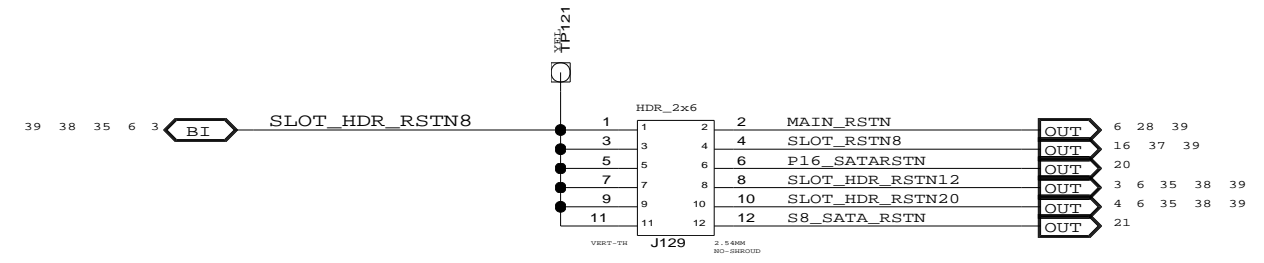
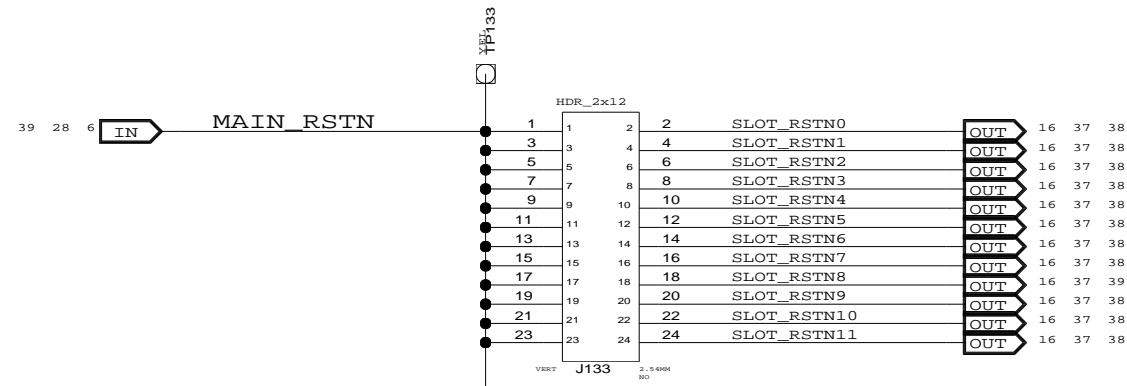




		TITLE EB-LOGAN-19	
		PARTITION RESET SELECT HEADERS	
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:56 2010			SHEET 38 OF 41

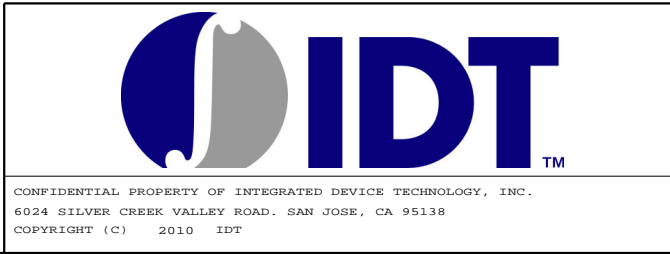
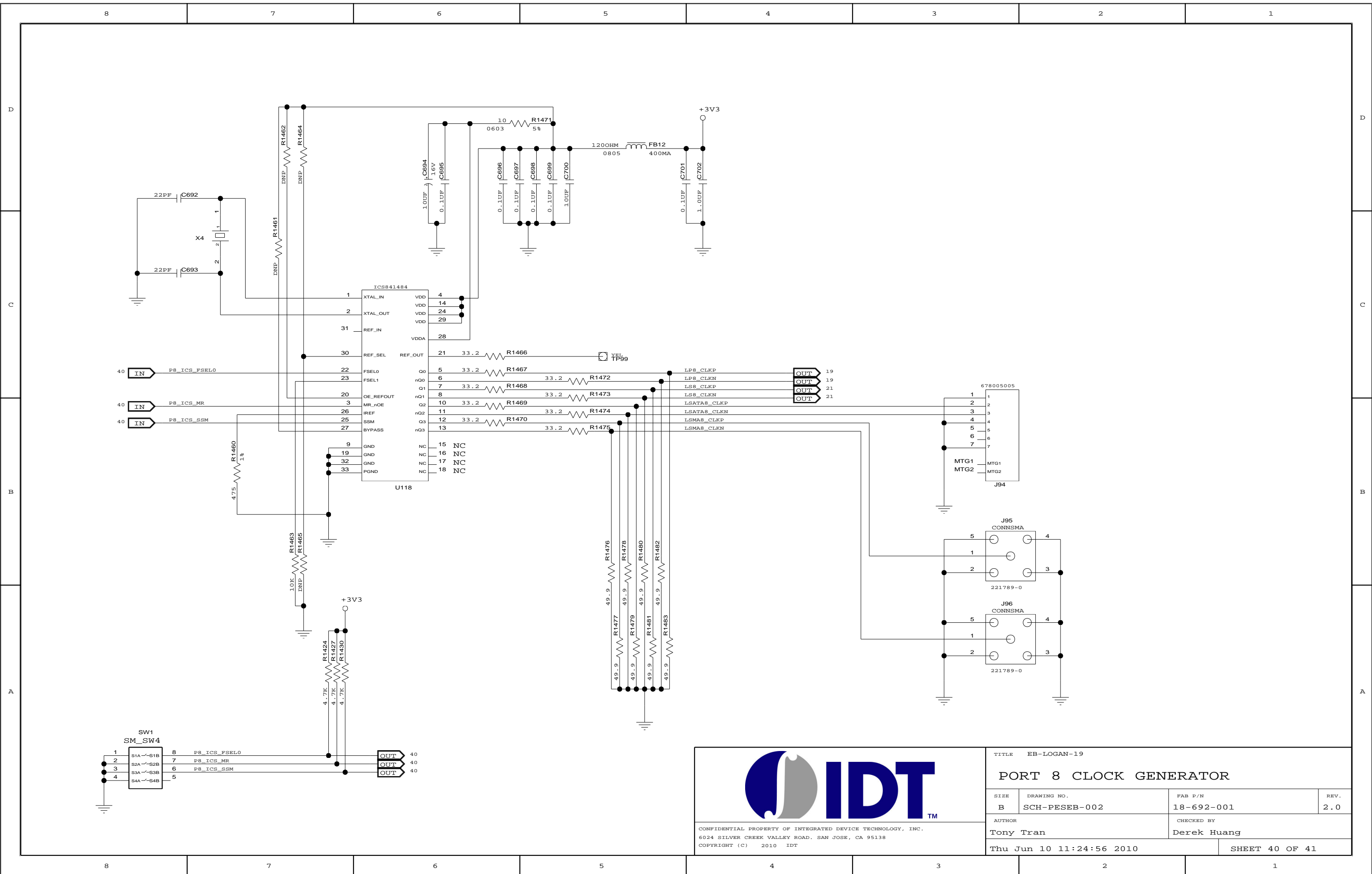
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NOTE: DNP JUMPERS WHEN IOEXPANDER IS ENABLED

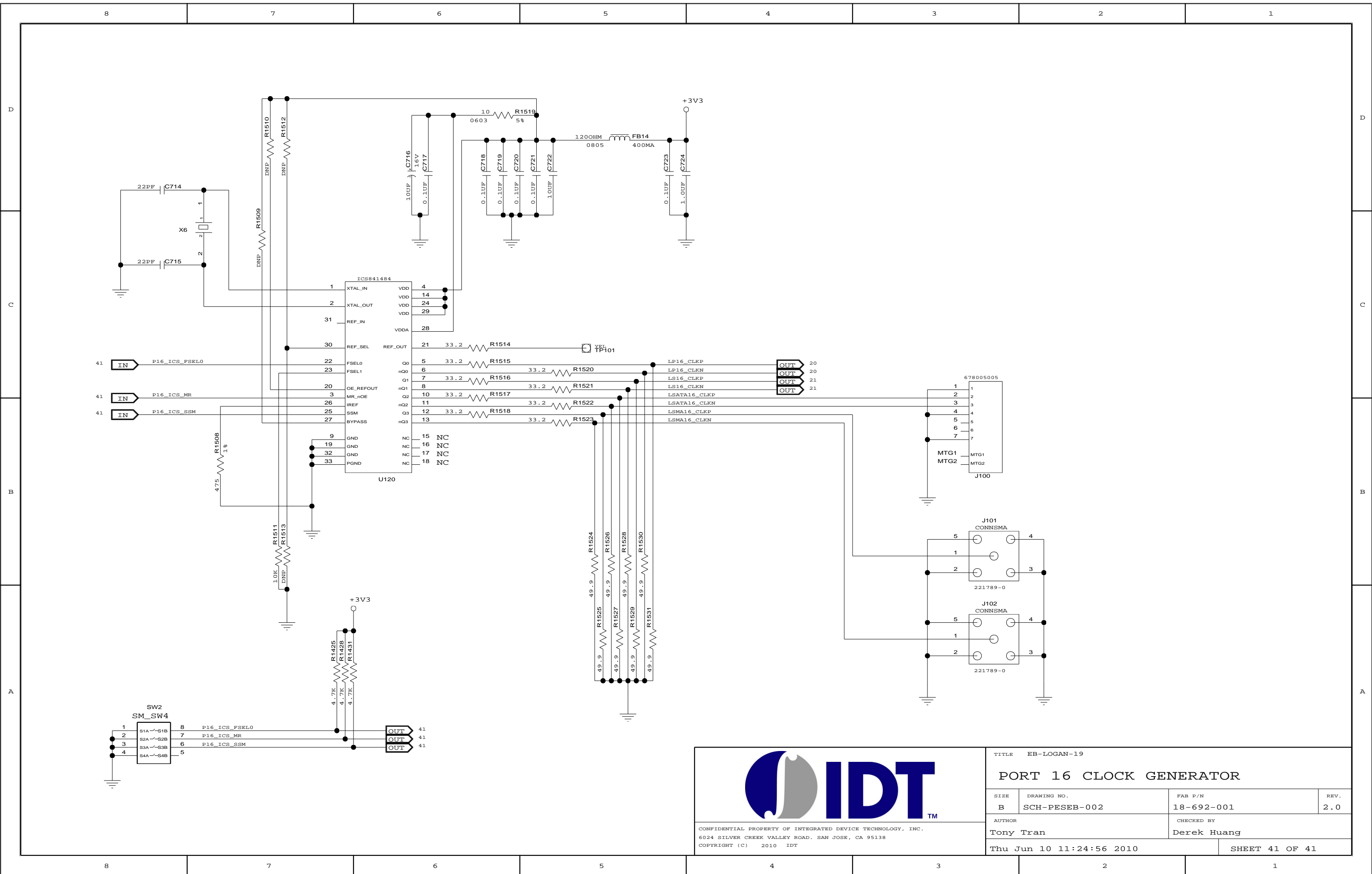



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TITLE EB-LOGAN-19			
SLOT RESET SELECT HEADERS			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:56 2010			SHEET 39 OF 41



TITLE EB-LOGAN-19			
PORT 8 CLOCK GENERATOR			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:56 2010			SHEET 40 OF 41





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TITLE EB-LOGAN-19

PORT 16 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:56 2010			SHEET 41 OF 41