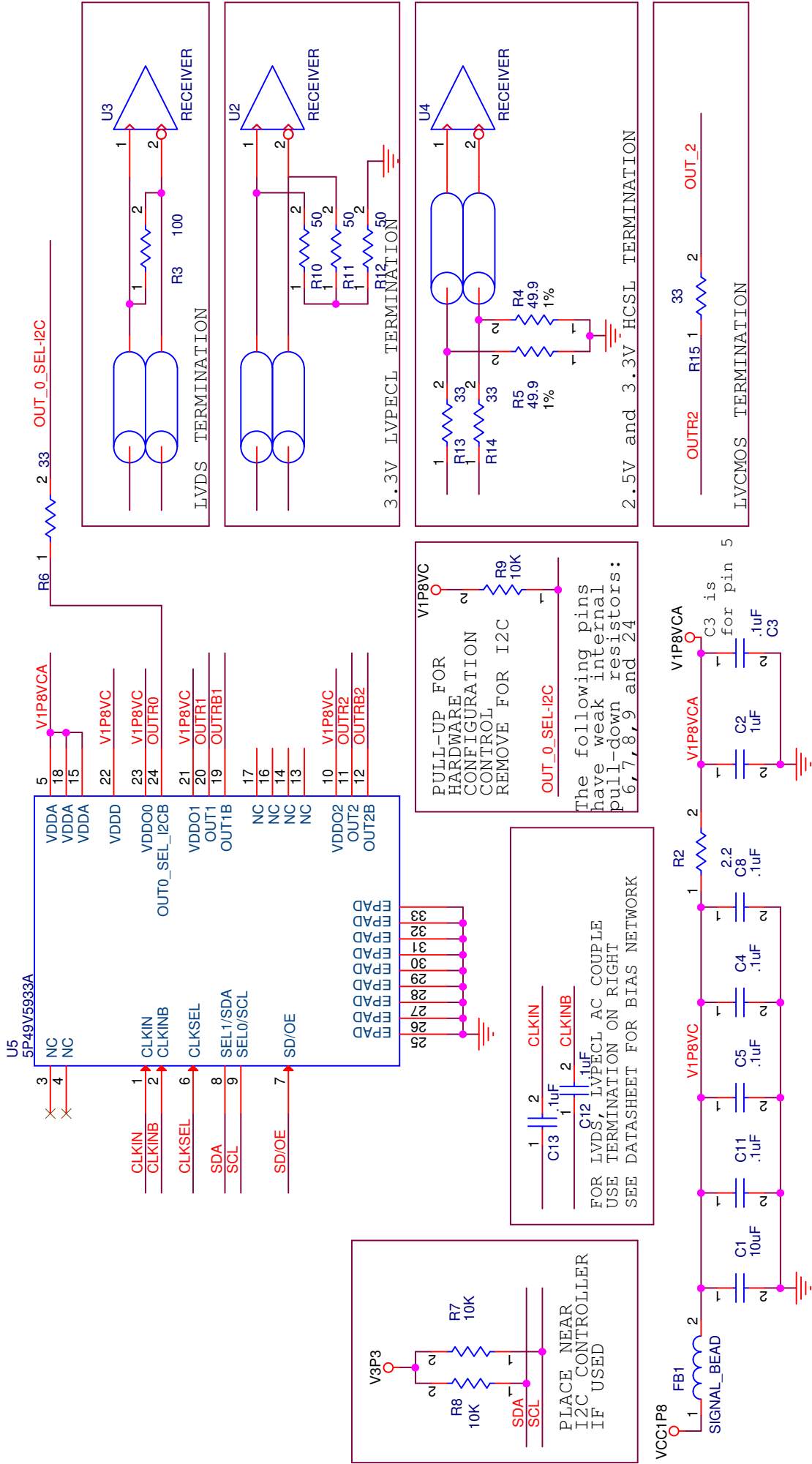




Layout notes:

- 1 Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
- 2 Do not share ground vias. One ground pin one ground via.

NOTE:FERRITE BEAD FB1 = Z@100MHz

Package	DC res.	Current (Ma)
0402	0.5	200
0402	0.18	200
0402	0.35	300
0402	0.35	300
0402	0.35	300