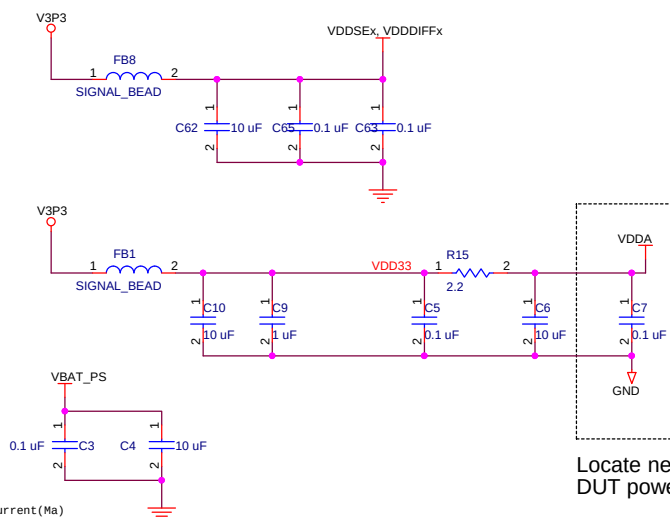
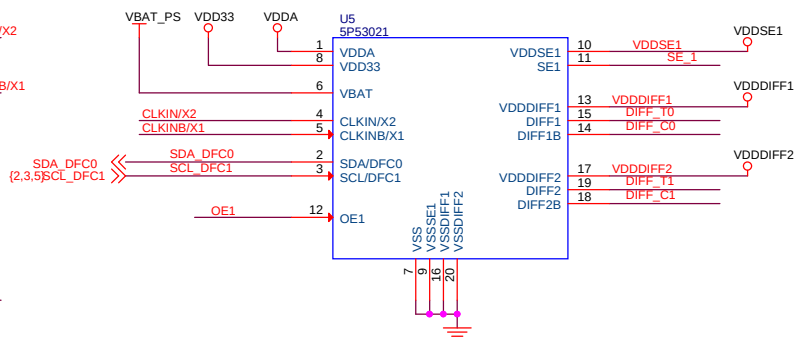
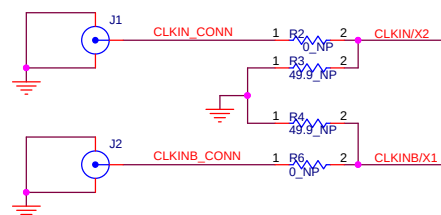
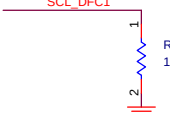




Manufacture	Part Number	Z@100MHz	PkgSz	DC res.	Current(Ma)
Fair-Rite	2504021217Y0	120	0402	0.5	200
muRata	BLM18AG601SN1D	220	0402	0.65	300
muRata	BLM15BB121SN1	120	0402	0.35	300
TDK	MMZ100S5241A	240	0402	0.18	200
TECSTAR	TB4532153121	120	0402	0.3	300

Revision history
0.1 02/24/16 first publication

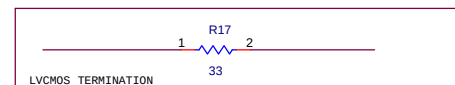
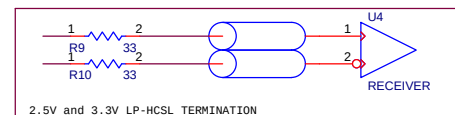
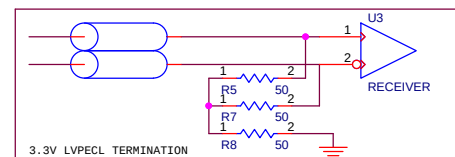
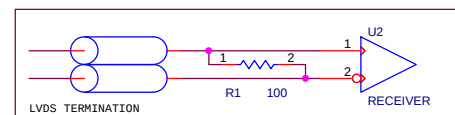
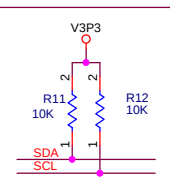
PULL-DOWN FOR
HARDWARE
CONFIGURATION
CONTROL
REMOVE FOR I2C



PLACE NEAR

1. I2C CONTROLLER IF USED
2. NO I2C, REMOVE 10K

FOR HARDWARE MODE



1. Separate Xout and Xin traces by at least 3 x the trace width.
2. Do not share crystal load capacitor ground via with other components.
3. Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
4. Do not share ground via. One ground pin one ground via.
5. Exposed pad should be grounded but is not required.

Integrated Device Technology

Size B	Document Number 5P35021_Reference Schematic	Rev 1.1
Date:	Monday, October 07, 2019	Sheet 1 of 1