

# Smart Configurator for RX V2.3.0

R20UT4487ES0231  
Rev.2.3.1  
Nov.18.19

## Release Note

### Introduction

Thank you for using the Smart Configurator for RX.

This document describes the restrictions and points for caution. Read this document before using the product.

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## 1. Introduction

Smart Configurator is a utility for combining software to meet your needs. It supports the following three functions related to the embedding of Renesas drivers in your systems: importing middleware, generating driver code, and setting pins.

### 1.1 System requirements

The operating environment is as follows.

#### 1.1.1 PC

- IBM PC/AT compatibles (Windows® 10, Windows® 8.1, Windows® 7)
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)
- Memory capacity: 2 GB or more recommended. Minimum requirement is 1 GB or more (64-bit Windows requires 2 GB or more)
- Hard disk capacity: 200 MB or more spare capacity
- Display: 1024 x 768 or higher resolution, 65,536 or more colors
- All other necessary software environments in addition to Windows OS: .NET Framework version 4.5

#### 1.1.2 Development Environments

- Renesas electronics Compiler for RX [CC-RX] V3.01.00 or later
- GCC for Renesas 4.8.4.201902 or later
- IAR Embedded Workbench 4.12.1 or later

## 2. Support List

### 2.1 Support Devices List

Below is a list of devices supported by the Smart Configurator for RX V2.3.0.

**Table 2-1 Support Devices**

Group (HW Manual number)	PIN	Device name
RX110 Group (R01UH0421EJ0120)	36pin	R5F5110HAxLM, R5F5110JAxLM, R5F51101AxLM, R5F51103AxLM
	40pin	R5F51101AxNF, R5F51103AxNF, R5F5110HAxNF, R5F5110JAxNF
	48pin	R5F51101AxNE, R5F51103AxNE, R5F51104AxNE, R5F51105AxNE, R5F5110JAxNE, R5F51101AxFL, R5F51103AxFL, R5F51104AxFL, R5F51105AxFL, R5F5110JAxFL
	64pin	R5F51101AxLF, R5F51103AxLF, R5F51104AxLF, R5F51105AxLF, R5F5110JAxLF, R5F51101AxFK, R5F51103AxFK, R5F51104AxFK, R5F51105AxFK, R5F5110JAxFK, R5F51101AxFM, R5F51103AxFM, R5F51104AxFM, R5F51105AxFM, R5F5110JAxFM
RX111 Group (R01UH0365EJ0130)	36pin	R5F51111AxLM, R5F51113AxLM, R5F5111JAxLM
	40pin	R5F51111AxNF, R5F51113AxNF, R5F5111JAxNF
	48pin	R5F51111AxFL, R5F51113AxFL, R5F51114AxFL, R5F51115AxFL, R5F51116AxFL, R5F51117AxFL, R5F51118AxFL, R5F5111JAxFL, R5F51111AxNE, R5F51113AxNE, R5F51114AxNE, R5F51115AxNE, R5F51116AxNE, R5F51117AxNE, R5F51118AxNE, R5F5111JAxNE
	64pin	R5F51111AxFM, R5F51113AxFM, R5F51114AxFM, R5F51115AxFM, R5F51116AxFM, R5F51117AxFM, R5F51118AxFM, R5F5111JAxFM, R5F51111AxFK, R5F51113AxFK, R5F51114AxFK, R5F51115AxFK, R5F51116AxFK, R5F51117AxFK, R5F51118AxFK, R5F5111JAxFK, R5F51111AxLF, R5F51113AxLF, R5F51114AxLF, R5F51115AxLF, R5F51116AxLF, R5F51117AxLF, R5F51118AxLF, R5F5111JAxLF
RX113 Group (R01UH0448EJ0110)	64pin	R5F51135AxFM, R5F51136AxFM, R5F51137AxFM, R5F51138AxFM
	100pin	R5F51135AxLJ, R5F51136AxLJ, R5F51137AxLJ, R5F51138AxLJ, R5F51135AxFP, R5F51136AxFP, R5F51137AxFP, R5F51138AxFP
RX130 Group (R01UH0560EJ0200)	48pin	R5F51303AxFL, R5F51305AxFL, R5F51303AxNE, R5F51305AxNE, R5F51306AxNE, R5F51306AxFL, R5F51307AxNE, R5F51307AxFL, R5F51308AxNE, R5F51308AxFL, R5F51306BxFL
	64pin	R5F51303AxFM, R5F51305AxFM, R5F51303AxFK, R5F51305AxFK, R5F51306AxFK, R5F51306AxFM, R5F51307AxFK, R5F51307AxFM, R5F51308AxFK, R5F51308AxFM R5F51308AxFK, R5F51308AxFM, R5F51306BxFK, R5F51306BxFM
	80pin	R5F51303AxFN, R5F51305AxFN, R5F51306AxFN, R5F51306BxFN
	100pin	R5F51305AxFP, R5F51306AxFP, R5F51307AxFP, R5F51308AxFP, R5F51305BxFP, R5F51306BxFP
RX230 Group (R01UH0496EJ0110)	48pin	R5F52305AxNE, R5F52306AxNE, R5F52305AxFL, R5F52306AxFL
	64pin	R5F52305AxND, R5F52306AxND, R5F52305AxFM, R5F52306AxFM, R5F52305AxLF, R5F52306AxLF
	100pin	R5F52305AxLA, R5F52306AxLA, R5F52305AxFP, R5F52306AxFP

Table 2-2 Support Devices

Group (HW Manual number)	PIN	Device name
RX231 Group (R01UH0496EJ0110)	48pin	R5F52315AxNE, R5F52316AxNE, R5F52317AxNE, R5F52318AxNE, R5F52315CxNE, R5F52316CxNE, R5F52317BxNE, R5F52318BxNE, R5F52315AxFL, R5F52316AxFL, R5F52317AxFL, R5F52318AxFL, R5F52315CxFL, R5F52316CxFL, R5F52317BxFL, R5F52318BxFL
	64pin	R5F52315AxND, R5F52316AxND, R5F52317AxND, R5F52318AxND, R5F52315CxND, R5F52316CxND, R5F52317BxND, R5F52318BxND, R5F52315AxFM, R5F52316AxFM, R5F52317AxFM, R5F52318AxFM, R5F52315CxFM, R5F52316CxFM, R5F52317BxFM, R5F52318BxFM, R5F52315CxLF, R5F52316CxLF
	100pin	R5F52315AxLA, R5F52316AxLA, R5F52317AxLA, R5F52318AxLA, R5F52315CxLA, R5F52316CxLA, R5F52317BxLA, R5F52318BxLA, R5F52315AxFP, R5F52316AxFP, R5F52317AxFP, R5F52318AxFP, R5F52315CxFP, R5F52316CxFP, R5F52317BxFP, R5F52318BxFP
RX23T Group (R01UH0520EJ0110)	48pin	R5F523T3AxFL, R5F523T5AxFL
	52pin	R5F523T5AxFD, R5F523T3AxFD
	64pin	R5F523T5AxFM, R5F523T3AxFM
RX24T Group (R01UH0576EJ0200)	64pin	R5F524TAAxFM, R5F524T8AxFM R5F524TAAxFK, R5F524T8AxFK
	80pin	R5F524TAAxFF, R5F524T8AxFF, R5F524TAAxFN, R5F524T8AxFN
	100pin	R5F524TCAxFP, R5F524T8AxFP, R5F524TBxFP, R5F524TEAxFP, R5F524TAAxFP
RX24U Group (R01UH0658EJ0100)	100pin	R5F524UEAxFP, R5F524UCAxFP, R5F524UBAxFP
	144pin	R5F524UEAxFB, R5F524UBAxFB, R5F524UCAxFB
RX64M Group (R01UH0377EJ0110)	100pin	R5F564MFCxFP, R5F564MFCxLJ, R5F564MFDxFP, R5F564MFDxLJ, R5F564MGCxFP, R5F564MGCxLJ, R5F564MGDxFP, R5F564MGDxLJ, R5F564MJCxFP, R5F564MJCxLJ, R5F564MJDxFP, R5F564MJDxLJ, R5F564MLCxFP, R5F564MLCxLJ, R5F564MLDxFP, R5F564MLDxLJ
	144/145pin	R5F564MFCxFB, R5F564MFCxLK, R5F564MFDxFB, R5F564MFDxLK, R5F564MGCxFB, R5F564MGCxLK, R5F564MGDxFB, R5F564MGDxLK, R5F564MJCxFB, R5F564MJCxLK, R5F564MJDxFB, R5F564MJDxLK, R5F564MLCxFB, R5F564MLCxLK, R5F564MLDxFB, R5F564MLDxLK
	176/177pin	R5F564MFDxFC, R5F564MFDxBG, R5F564MFDxLC, R5F564MFCxFC, R5F564MFCxBG, R5F564MFCxLC, R5F564MGDxFC, R5F564MGDxBG, R5F564MGDxLC, R5F564MGCxFC, R5F564MGCxBG, R5F564MGCxLC, R5F564MJDxFC, R5F564MJDxBG, R5F564MJDxLC, R5F564MJCxFC, R5F564MJCxBG, R5F564MJCxLC, R5F564MLDxFC, R5F564MLDxBG, R5F564MLDxLC, R5F564MLCxFC, R5F564MLCxBG, R5F564MLCxLC

Table 2-3 Support Devices

Group (HW Manual number)	PIN	Device name
RX65N Group (R01UH0590EJ0210)	100pin	R5F565N9AxLJ, R5F565N9BxLJ, R5F565N9ExLJ, R5F565N9FxLJ, R5F565N7AxLJ, R5F565N7BxLJ, R5F565N7ExLJ, R5F565N7FxLJ, R5F565N4AxLJ, R5F565N4BxLJ, R5F565N4ExLJ, R5F565N4FxLJ, R5F565N9AxFP, R5F565N9BxFP, R5F565N9ExFP, R5F565N9FxFP, R5F565N7AxFP, R5F565N7BxFP, R5F565N7ExFP, R5F565N7FxFP, R5F565N4AxFP, R5F565N4BxFP, R5F565N4ExFP, R5F565N4FxFP, R5F565NCHxLJ, R5F565NCDxLJ, R5F565NEHxLJ, R5F565NEDxLJ, R5F565NCHxFP, R5F565NCDxFP, R5F565NEHxFP, R5F565NEDxFP
	144/145pin	R5F565N9AxFB, R5F565N9BxFB, R5F565N9ExFB, R5F565N9FxFB, R5F565N7AxFB, R5F565N7BxFB, R5F565N7ExFB, R5F565N7FxFB, R5F565N4AxFB, R5F565N4BxFB, R5F565N4ExFB, R5F565N4FxFB, R5F565NCHxFB, R5F565NCDxFB, R5F565NEHxFB, R5F565NEDxFB, R5F565N9AxLK, R5F565N9BxLK, R5F565N9ExLK, R5F565N9FxLK, R5F565N7AxLK, R5F565N7BxLK, R5F565N7ExLK, R5F565N7FxLK, R5F565N4AxLK, R5F565N4BxLK, R5F565N4ExLK, R5F565N4FxLK, R5F565NCHxLK, R5F565NCDxLK, R5F565NEHxLK, R5F565NEDxLK
	176/177pin	R5F565NCHxBG, R5F565NCDxBG, R5F565NEHxBG, R5F565NEDxBG, R5F565NCHxFC, R5F565NCDxFC, R5F565NEHxFC, R5F565NEDxFC, R5F565NCHxLC, R5F565NCDxLC, R5F565NEHxLC, R5F565NEDxLC
RX651 Group (R01UH0590EJ0210)	64pin	R5F5651CHxFM, R5F56514FxFM, R5F5651EHxFM, R5F5651CDxFM, R5F56514FxBP, R5F56514BxFM, R5F56519FxBP, R5F5651CDxBP, R5F5651EDxBP, R5F5651EDxFM, R5F56517BxBP, R5F5651EHxBP, R5F56519BxBP, R5F56517FxBP, R5F5651CHxBP, R5F56519FxFM, R5F56517BxFM, R5F56514BxBP, R5F56519BxFM, R5F56517FxFM
	100pin	R5F56519AxLJ, R5F56519BxLJ, R5F56519ExLJ, R5F56519FxLJ, R5F56517AxLJ, R5F56517BxLJ, R5F56517ExLJ, R5F56517FxLJ, R5F56514AxLJ, R5F56514BxLJ, R5F56514ExLJ, R5F56514FxLJ, R5F56519AxFP, R5F56519BxFP, R5F56519ExFP, R5F56519FxFP, R5F56517AxFP, R5F56517BxFP, R5F56517ExFP, R5F56517FxFP, R5F56514AxFP, R5F56514BxFP, R5F56514ExFP, R5F56514FxFP
	144/145pin	R5F56519AxFB, R5F56519BxFB, R5F56519ExFB, R5F56519FxFB, R5F56517AxFB, R5F56517BxFB, R5F56517ExFB, R5F56517FxFB, R5F56514AxFB, R5F56514BxFB, R5F56514ExFB, R5F56514FxFB, R5F5651CDxFB, R5F5651CHxFB, R5F5651EDxFB, R5F5651EHxFB, R5F56519AxLK, R5F56519BxLK, R5F56519ExLK, R5F56519FxLK, R5F56517AxLK, R5F56517BxLK, R5F56517ExLK, R5F56517FxLK, R5F56514AxLK, R5F56514BxLK, R5F56514ExLK, R5F56514FxLK, R5F5651CDxLK, R5F5651CHxLK, R5F5651EDxLK, R5F5651EHxLK
176/177pin	R5F5651CDxBG, R5F5651CDxFC, R5F5651CHxBG, R5F5651CHxFC, R5F5651EDxBG, R5F5651EDxFC, R5F5651EHxBG, R5F5651EHxFC, R5F5651CDxLC, R5F5651CHxLC, R5F5651EDxLC, R5F5651EHxLC	

Table 2-4 Support Devices

Group (HW Manual number)	PIN	Device name
RX66T Group (R01UH0749EJ0100)	64pin	R5F566TAAxFM, R5F566TAExDFM, R5F566TEAxFM, R5F566TEExFM
	80pin	R5F566TAAxFF, R5F566TAExFF, R5F566TEAxFF, R5F566TEExFF, R5F566TAAxFN, R5F566TAExFN, R5F566TEAxFN, R5F566TEExFN
	100pin	R5F566TKCxFP, R5F566TAExFP, R5F566TFFxFP, R5F566TFCxFP, R5F566TFExFP, R5F566TFBxFP, R5F566TFExFP, R5F566TABxFP, R5F566TAFxFP, R5F566TEFxFP, R5F566TKFxFP, R5F566TKGxFP, R5F566TKAxFP, R5F566TKExFP, R5F566TKBxFP, R5F566TEBxFP, R5F566TEExFP, R5F566TEAxFP, R5F566TAAxFP, R5F566TFGxFP
	112pin	R5F566TAAxFH, R5F566TAExFH, R5F566TEExFH, R5F566TEAxFH
	144pin	R5F566TKCxFB, R5F566TFGxFB, R5F566TFCxFB, R5F566TKGxFB
RX71M Group (R01UH0493EJ0110)	100pin	R5F571MLCxFP, R5F571MLDxFP, R5F571MLGxFP, R5F571MLHxFP, R5F571MJCxFP, R5F571MJDxFP, R5F571MJGxFP, R5F571MJHxFP, R5F571MGCxFP, R5F571MGDxFP, R5F571MGGxFP, R5F571MGHxFP, R5F571MFCxFP, R5F571MFDxFP, R5F571MFGxFP, R5F571MFHxFP, R5F571MLCxLJ, R5F571MLDxLJ, R5F571MLGxLJ, R5F571MLHxLJ, R5F571MJCxLJ, R5F571MJDxLJ, R5F571MJGxLJ, R5F571MJHxLJ, R5F571MGCxLJ, R5F571MGDxLJ, R5F571MGGxLJ, R5F571MGHxLJ, R5F571MFCxLJ, R5F571MFDxLJ, R5F571MFGxLJ, R5F571MFHxLJ
	144/145pin	R5F571MLCxLK, R5F571MLDxLK, R5F571MLGxLK, R5F571MLHxLK, R5F571MJCxLK, R5F571MJDxLK, R5F571MJGxLK, R5F571MJHxLK, R5F571MGCxLK, R5F571MGDxLK, R5F571MGGxLK, R5F571MGHxLK, R5F571MFCxLK, R5F571MFDxLK, R5F571MFGxLK, R5F571MFHxLK, R5F571MLCxFB, R5F571MLDxFB, R5F571MLGxFB, R5F571MLHxFB, R5F571MJCxFB, R5F571MJDxFB, R5F571MJGxFB, R5F571MJHxFB, R5F571MGCxFB, R5F571MGDxFB, R5F571MGGxFB, R5F571MGHxFB, R5F571MFCxFB, R5F571MFDxFB, R5F571MFGxFB, R5F571MFHxFB
	176/177pin	R5F571MLCxFC, R5F571MLDxFC, R5F571MLGxFC, R5F571MLHxFC, R5F571MJCxFC, R5F571MJDxFC, R5F571MJGxFC, R5F571MJHxFC, R5F571MGCxFC, R5F571MGDxFC, R5F571MGGxFC, R5F571MGHxFC, R5F571MFCxFC, R5F571MFDxFC, R5F571MFGxFC, R5F571MFHxFC, R5F571MLCxLC, R5F571MLDxLC, R5F571MLGxLC, R5F571MLHxLC, R5F571MJCxLC, R5F571MJDxLC, R5F571MJGxLC, R5F571MJHxLC, R5F571MGCxLC, R5F571MGDxLC, R5F571MGGxLC, R5F571MGHxLC, R5F571MFCxLC, R5F571MFDxLC, R5F571MFGxLC, R5F571MFHxLC, R5F571MLCxBG, R5F571MLDxBG, R5F571MLGxBG, R5F571MLHxBG, R5F571MJCxBG, R5F571MJDxBG, R5F571MJGxBG, R5F571MJHxBG, R5F571MGCxBG, R5F571MGDxBG, R5F571MGGxBG, R5F571MGHxBG, R5F571MFCxBG, R5F571MFDxBG, R5F571MFGxBG, R5F571MFHxBG
RX72T Group (R01UH0803EJ0100)	100pin	R5F572TKExFP, R5F572TFFxFP, R5F572TKFxFP, R5F572TFGxFP, R5F572TKCxFP, R5F572TFBxFP, R5F572TFExFP, R5F572TFCxFP, R5F572TFAxFP, R5F572TKAxFP, R5F572TKBxFP, R5F572TKGxFP
	144pin	R5F572TKGxFB, R5F572TKCxFB, R5F572TFGxFB, R5F572TFCxFB
RX72M Group (R01UH0804EJ0100)	176pin	R5F572MNHxFC, R5F572MDDxBG, R5F572MNDxFC, R5F572MDHxBG, R5F572MDDxFC, R5F572MNHxBG, R5F572MNDxBG, R5F572MDHxFC
	224pin	R5F572MDDxBD, R5F572MDHxBD, R5F572MNHxBD, R5F572MNDxBD
RX23W Group (R01UH0823EJ0100)	56pin	R5F523W8BxNG, R5F523W8AxNG, R5F523W7BxNG, R5F523W7AxNG
	85pin	R5F523W7AxBL, R5F523W8AxBL, R5F523W8BxBL, R5F523W7BxBL

Table 2-5 Support Devices

Group (HW Manual number)	PIN	Device name
RX23E-A Group (R01UH0801EJ0100)	40pin	R5F523E5AxNF, R5F523E6AxNF
	48pin	R5F523E5AxFL, R5F523E6AxFL
RX13T Group (R01UH0822EJ0100)	32pin	R5F513T3AxFJ, R5F513T5AxFJ
	48pin	R5F513T5AxFL, R5F513T3AxFL



## 2.2 Support Components List

Below is a list of Components supported by the Smart Configurator for RX V2.3.0.

**Table 2-6 Support Components**

○: Support, /: Non-support

No	Components	Mode	RX110	RX111	RX113	RX130	RX13T	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	RX64M	RX65N, RX651	RX66T	RX71M	RX72M	RX72T	Remarks
1	8-Bit Timer	-	/	/	○	○	/	○	○	○	○	○	○	○	○	○	○	○	
2	CRC Calculator	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
3	D/A Converter	-	/	○	○	○	○	○	/	○	○	○	○	○	○	○	○	○	
4	DMA Controller	-	/	/	/	/	/	○	○	/	○	/	○	○	○	○	○	○	
5	I2C Slave Mode	I2C mode	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
		SMBus mode	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
6	I2C Master Mode	I2C mode	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Note 1
		SMBus mode	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
7	LCD Controller		/	/	○	/	/	/	/	/	/	/	/	/	/	/	/	/	
8	PWM Mode Timer	PWM mode 1	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
		PWM mode 2	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
9	SCI/SCIF Clock Synchronous Mode	Transmission	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Note 2, 3
		Reception	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Note 2, 3
		Transmission/Reception	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Note 2, 3
10	SCI/SCIF Asynchronous Mode	Transmission	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Note 2
		Reception	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Note 2
		Transmission/Reception	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Note 2
		Multi-processor Transmission	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Note 2
		Multi-processor Reception	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Note 2
		Multi-processor Transmission/Reception	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Note 2
11	SPI Clock Synchronous Mode	Slave transmit/receive	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
		Slave transmit only	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
		Master transmit/receive	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
		Master transmit only	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
12	SPI Operation Mode	Slave transmit/receive	○	○	○	○	/	○	○	○	○	○	○	○	○	○	○	○	
		Slave transmit only	○	○	○	○	/	○	○	○	○	○	○	○	○	○	○	○	
		Master transmit/receive	○	○	○	○	/	○	○	○	○	○	○	○	○	○	○	○	
		Master transmit only	○	○	○	○	/	○	○	○	○	○	○	○	○	○	○	○	
		Multi-master transmit/receive	○	○	○	○	/	○	○	○	○	○	○	○	○	○	○	○	
		Multi-master transmit only	○	○	○	○	/	○	○	○	○	○	○	○	○	○	○	○	
13	Event Link Controller	-	/	○	○	○	/	○	○	/	○	/	○	○	○	○	○		
14	Watchdog Timer	-	○	○	○	○	/	○	○	○	○	○	○	○	○	○	○		
15	Clock Frequency Accuracy Measurement Circuit	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○		

Note 1. Refer to No 1 in Table 5-1  
 Note 2. Refer to No 2, 3 in Table 6-2  
 Note 3. Refer to No 4 in Table 6-2

Table 2-7 Support Components

○: Support, /: Non-support

No	Components	Mode	RX110	RX111	RX113	RX130	RX13T	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	RX64M	RX65N, RX651	RX66T	RX71M	RX72M	RX72T	Remarks
16	Group Scan Mode S12AD	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Note 4
17	Comparator	-	/	/	○	○	○	○	/	/	○	/	/	/	○	/	○	○	
18	Compare Match Timer	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
19	Single Scan Mode S12AD	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Note 5
20	Smart Card Interface Mode	Transmission	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
		Reception	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
		Transmission/Reception	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
21	Dead-time Compensation Counter	-	○	○	○	○	○	○	○	○	/	○	○	○	○	○	○	○	
22	Data Transfer Controller	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	Note 6
23	Data Operation Circuit	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
24	Normal Mode Timer	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
25	Buses	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
26	Programmable Pulse Generator	-	/	/	/	/	/	/	/	/	/	/	○	○	/	○	/	/	
27	Ports	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
28	Port Output Enable	-	/	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
29	Real Time Clock	Binary	○	○	○	○	/	○	/	/	○	/	○	○	/	○	/	/	
		Calendar	○	○	○	○	/	○	/	/	○	/	○	○	/	○	/	/	
30	Remote Control Signal Receiver	-	/	/	/	○	/	/	/	/	/	/	/	/	/	/	/	/	
31	Low-Power Timer	-	/	/	○	○	/	○	○	/	○	/	/	/	/	/	/	/	
32	Phase Counting Mode Timer	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
33	Interrupt Controller	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
34	General PWM Timer	Saw-wave PWM mode	/	/	/	/	/	/	/	○	/	○	○	/	○	○	○	○	Note 7
		Saw-wave one-shot pulse mode	/	/	/	/	/	/	/	○	/	○	○	/	○	○	○	○	Note 7
		Triangle-wave PWM mode 1	/	/	/	/	/	/	/	○	/	○	○	/	○	○	○	○	Note 7
		Triangle-wave PWM mode 2	/	/	/	/	/	/	/	○	/	○	○	/	○	○	○	○	Note 7
		Triangle-wave PWM mode 3	/	/	/	/	/	/	/	○	/	○	○	/	○	○	○	○	Note 7
35	Low Power Consumption	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
36	Complementary PWM Mode Timer	Complementary PWM mode 1	/	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
		Complementary PWM mode 2	/	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
		Complementary PWM mode 3	/	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
37	Continuous Scan Mode S12AD	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	

Note 4. Refer to No 2 in Table 5-1  
 Note 5. Refer to No 3 in Table 5-1  
 Note 6. Refer to No 8 in Table 6-1  
 Note 7. Refer to No 1 in Table 6-1

Table 2-8 Support Components

○: Support, /: Non-support

No	Components	Mode	RX110	RX111	RX113	RX130	RX13T	RX230_RX231	RX23E-A	RX23T	RX23W	RX24T_RX24U	RX64M	RX65N_RX651	RX66T	RX71M	RX72M	RX72T	Remarks
38	Voltage Detection Circuit	-	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
39	Delta-Sigma Modulator Interface	Master	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	○	/
		Slave	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	○
40	Single Scan Mode DSAD	-	/	/	/	/	/	/	○	/	/	/	/	/	/	/	/	/	
41	Continuous Scan Mode DSAD	-	/	/	/	/	/	/	○	/	/	/	/	/	/	/	/	/	

## **2.3 New support**

### **2.3.1 Supports new RX23E-A group devices**

Support new RX23E-A group devices from Smart Configurator for RX V2.3.0.

### 3. Changes

This chapter describes changes to the Smart Configurator for RX V2.3.0.

#### 3.1 Correction of issues/limitations

**Table 3-1 List of Correction of issues/limitations**

○: Applicable, /: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX13T	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	RX64M	RX65N, RX651	RX66T	RX71M	RX72M	RX72T	Remarks
1	Fixed the build warning W0520177:Variable "w_count" was declared but never referenced	○	○	○	○	/	○	/	/	/	/	○	○	/	○	/	/	
2	Fixed ICLK setting restriction issue on clock page in RX231 group devices	/	/	/	/	/	○	/	/	/	/	/	/	/	/	/	/	RX231 only
3	Fixed the issue of MTCLKA and MTCLKB cannot be used for MTU2 in 16-bit Phase counting mode	/	/	/	/	/	/	/	/	/	/	/	/	○	/	/	○	
4	Fixed the incorrect restriction for multiple channel selection on using S12AD1 in Single Scan Mode and Continuous Scan Mode components	/	/	/	/	/	/	/	/	/	/	○	○	/	○	○	/	
5	Fixed the incorrect time issue when using Calendar counting mode of Real Time Clock component	/	○	○	/	/	○	/	/	○	/	/	/	/	○	○	/	
6	Fixed the part number (R5F51306BxNE) missing issue for RX130 group devices with 48-pin HWQFN package type	/	/	/	○	/	/	/	/	/	/	/	/	/	/	/	/	
7	Fixed build error E0520020 when using SPI Clock Synchronous Mode component with RSPI channels	/	/	/	/	/	/	/	/	/	/	○	○	○	○	○	○	
8	Fixed the FIT module location configuration issue while creating IAR project by standalone Smart Configurator	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
9	Fixed the build error E0520020:Identifier "IER_GPTA_ETGIP" or "IER_GPTA_ETGIN" is undefined when using General PWM Timer	/	/	/	/	/	/	/	/	/	/	○	/	/	○	/	/	
10	Fixed the issue of DTC virtual memory address in not set in linker_script.ld for GCC project	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
11	Fixed the complementary PWM mode timer code not be generated	/	/	/	/	/	/	/	/	/	/	○	/	/	/	/	/	
12	Fixed the SDCLK not be saved in project	/	/	/	/	/	/	/	/	/	/	○	○	/	○	/	/	

- 3.1.1 Fixed the build warning W0520177:Variable "w\_count" was declared but never referenced**  
The build warning "W0520177:Variable "w\_count" was declared but never referenced" when Oscillation source is set to "External oscillator input" on Clocks page has been fixed from SC for RX V2.3.0.
- 3.1.2 Fixed ICLK setting restriction issue on Clocks page**  
The issue of ICLK configuration value cannot be smaller than PCLK has been fixed for RX231.
- 3.1.3 Fixed the issue of MTCLKA and MTCLKB cannot be used for MTU2 in 16-bit Phase counting mode**  
The issue of Smart Configurator does not support using MTCLKA and MTCLKB as external clock input for MTU2 in 16-bit Phase counting mode has been fixed.
- 3.1.4 Fixed the incorrect restriction for multiple channel selection on using S12AD1 in Single Scan Mode and Continuous Scan Mode components**  
When using "Extend analog input mode" and select multiple analog input channels in Single Scan Mode and Continuous Scan Mode components of SC RX V2.2.1 and before, an error will be displayed beside "Extend analog input mode" check box with a tip "Setting is not valid because two or more analog input channels has been selected". This error is irrelevant and has been removed from Smart Configurator for RX V2.3.0.
- 3.1.5 Fixed the incorrect time issue when using Calendar counting mode of Real Time Clock component**  
The issue of "Real time clock initial value" displays the current local time instead of the time configured before closing project has been fixed.
- 3.1.6 Fixed the part number (R5F51306BxNE) missing issue for RX130 group devices with 48-pin HWQFN package type**  
The issue of Smart Configurator does not support RX130 group devices with 48-pin HWQFN package type (product part number: R5F51306BxNE) has been fixed.
- 3.1.7 Fixed build error E0520020 when using SPI Clock Synchronous Mode component with RSPI channels**  
The issue of build error E0520020 when error interrupt is not enabled: "Identifier "r\_Config\_RSPI\_error\_interrupt" is undefined" has been fixed.
- 3.1.8 Fixed the FIT module location configuration issue while creating IAR project by standalone Smart Configurator**  
The issue of unsuccessful configuration of FIT module location if configure using FIT Module Settings wizard has been fixed from Smart Configurator for RX V2.3.0.
- 3.1.9 Fixed the build error E0520020: Identifier "IER\_GPTA\_ETGIP" or "IER\_GPTA\_ETGIN" is undefined when using General PWM Timer**  
The issue of build errors when calling the macro function to disable ETGIP and ETGIN interrupts has been fixed.
- 3.1.10 Fixed the issue of DTC virtual memory address in not set in linker\_script.ld for GCC project**  
The issue of DTC virtual memory address is not set in linker\_script.ld file after code generation when using DTC component in SC for RX V2.2.0 and V2.2.1 has been fixed.

**3.1.11 Fixed the complementary PWM mode timer code not be generated**

The issue of complementary PWM mode timer code not be generated when changing the interrupt for unused interrupts of “software configuratble interrpt” in [interrupts] page has been fixed.

**3.1.12 Fixed the SDCLK not be saved in project**

The issue that SDCLK settings could not be saved in the project has been fixed.

### 3.2 Specification changes

Table 3-2 List of Specification changes

○: Applicable, /: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX13T	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	RX64M	RX65N, RX651	RX66T	RX71M	RX72M	RX72T	Remarks
1	Changed code specification of Port Output Enable component	/	/	/	/	/	/	/	/	/	○ *	/	/	/	/	/	/	* RX24T 64-pin



### 3.2.1 Changed code specification of Port Output Enable component

When using POE of RX24T 64-pin package devices, POE11# pin codes generated out are redundant and have been removed.

Redundant location :

*Source file : < Port Output Enable configuration name >.c*

*Function : R\_< Port Output Enable configuration name >\_Stop*

#### Example


```

/*****
* Function Name: R_Config_POE_Stop
* Description  : This function stops the POE3 module
* Arguments    : None
* Return Value : None
*****/
void R_Config_POE_Stop(void)
{
    : (codes are omitted)
/* Clear POE10F flag */
if (1U == POE.ICSR4.BIT.POE10F)
{
    POE.ICSR4.BIT.POE10F = 0U;
}

/* Clear POE11F flag */
if (1U == POE.ICSR5.BIT.POE11F)
{
    POE.ICSR5.BIT.POE11F = 0U;
}

/* Clear POE12F flag */
if (1U == POE.ICSR7.BIT.POE12F)
{
    POE.ICSR7.BIT.POE12F = 0U;
}
: (codes are omitted)
}

```



#### 4. List of RENESAS TOOL NEWS

Below is a list of notifications delivered by RENESAS TOOL NEWS.

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Sep. 1, 2017	R20TS0198	When using the I2C bus interface in slave mode <a href="https://www.renesas.com/search/keyword-search.html#genre=document&amp;q=R20TS0198">https://www.renesas.com/search/keyword-search.html#genre=document&amp;q=R20TS0198</a>	RX130, RX64M, RX651, RX65N	V1.3.0
Apr. 1, 2018	R20TS0294	When using the bus for peripheral functions <a href="https://www.renesas.com/search/keyword-search.html#genre=document&amp;q=R20TS0294">https://www.renesas.com/search/keyword-search.html#genre=document&amp;q=R20TS0294</a>	RX230, RX231	V1.4.0
Oct. 01, 2018	R20TS0351	Setting TPU0 channel of PWM Mode Timer <a href="https://www.renesas.com/search/keyword-search.html#genre=document&amp;q=R20TS0351">https://www.renesas.com/search/keyword-search.html#genre=document&amp;q=R20TS0351</a>	RX65N, RX651, RX64M	V1.5.0
Feb.01, 2019	R20TS0401	Point for caution when using the GTIOcnm pin (n = 0 to 9, m = A, B) of the general PWM timer (GPTW) as a hardware source <a href="https://www.renesas.com/search/keyword-search.html#genre=document&amp;q=R20TS0401">https://www.renesas.com/search/keyword-search.html#genre=document&amp;q=R20TS0401</a>	RX66T	V2.1.0
Apr.16, 2019	R20TS0425	When using the I2C bus interface in master mode <a href="https://www.renesas.com/search/keyword-search.html#q=R20TS0425">https://www.renesas.com/search/keyword-search.html#q=R20TS0425</a>	RX110, RX111, RX113, RX130, RX230, RX231, RX23T, RX24T, RX24U, RX64M, RX651, RX65N, RX71M	V2.2.0
Jun.01, 2019	R20TS0434	1. When using self-diagnosis function of 12-bit A/D converter in Single Scan Mode 2. When using Serial Peripheral Interface clock synchronous mode in slave transmit 3. When using I2C Bus Interface with Fast-mode Plus enabled <a href="https://www.renesas.com/search/keyword-search.html#q=R20TS0434">https://www.renesas.com/search/keyword-search.html#q=R20TS0434</a>	RX230, RX231, RX66T, RX72T, RX64M, RX651, RX65N, RX71M	V2.2.0
Jun.16, 2019	R20TS0436	When using general PWM timer <a href="https://www.renesas.com/search/keyword-search.html#q=R20TS0436">https://www.renesas.com/search/keyword-search.html#q=R20TS0436</a>	RX66T, RX72T	V2.2.0

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Aug.01, 2019	R20TS0466	When using the NACK reception transfer suspension function on the I <sup>2</sup> C bus interface <a href="https://www.renesas.com/search/keyword-search.html?q=R20TS0466">https://www.renesas.com/search/keyword-search.html?q=R20TS0466</a>	RX110, RX111, RX113, RX130, RX230, RX231, RX23T, RX24T, RX24U, RX64M, RX651, RX65N, RX66T, RX71M, RX72M, RX72T	V2.3.0

## 5. Points for Limitation

This section describes points for limitation regarding the Smart Configurator for RX V2.3.0. Please refer to a document of each module about a caution of a FIT module.

### 5.1 List of Limitation

Table 5-1 List of Limitation

○: Applicable, /: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX13T	RX230_RX231	RX23E-A	RX23T	RX23W	RX24T_RX24U	RX64M	RX65N_RX651	RX66T	RX71M	RX72M	RX72T	Remarks
1	Note on using I2C-bus Interface	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
2	Note on using S12AD Group Scan Mode	/	/	/	/	/	/	/	/	/	/	/	/	/	/	○	/	
3	Note on using double trigger mode in S12AD Single Scan Mode	/	/	/	/	/	/	/	/	/	/	/	/	/	○	○	/	
4	Note on using library type FIT modues	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
5	Note on using SDRAM External Bus	/	/	/	/	/	/	/	/	/	/	/	/	/	/	○	/	

## 5.2 Details of Limitation

### 5.2.1 Note on using I2C-bus Interface

When use the I2C Master Mode Component with RIICx resource, High width (ICBRH register) value and Low width (ICBRL register) value of SCL clock for SCL clock is not set properly. High width and Low width values may be set to less than the minimum value of the the I2C bus interface specification, and communication may not ve possible. Please set the ICBRH and ICBRL registers to properly value. About properly value is refer to “User’s Manual : Hardware”.

Modification location :

Source file : < I2C Master Mode configuration name >.c

Function : R\_< I2C Master Mode configuration name >\_Create

```

/*****
* Function Name: R_Config_RIIC0_Create
* Description  : This function initializes the RIIC0 channel
* Arguments    : None
* Return Value : None
*****/
void R_Config_RIIC0_Create (void)
{
    : (codes are omitted)
    /* Set transfer bit rate */
    RIIC0.ICMR1.BYTE |= _00_IIC_PCLK_DIV_1;
    RIIC0.ICBRL.BYTE = _FF_IIC0_SCL_LOW_LEVEL_PERIOD;
    RIIC0.ICBRH.BYTE = _E2_IIC0_SCL_HIGH_LEVEL_PERIOD;
    RIIC0.ICMR2.BYTE = 0x00U;
    RIIC0.ICMR3.BIT.NF = _00_IIC_NOISE_FILTER_1;
    RIIC0.ICMR3.BIT.SMBS = 0U;
    : (codes are omitted)
}
    
```

Modify this

### 5.2.2 Note on using S12AD Group Scan Mode

Dedicated sample and hold circuit text box input value should be greater than 0.4μs, but Smart Configurator for RX does not support this checking in version V2.3.0 and before. This limitation will be fixed in next version.

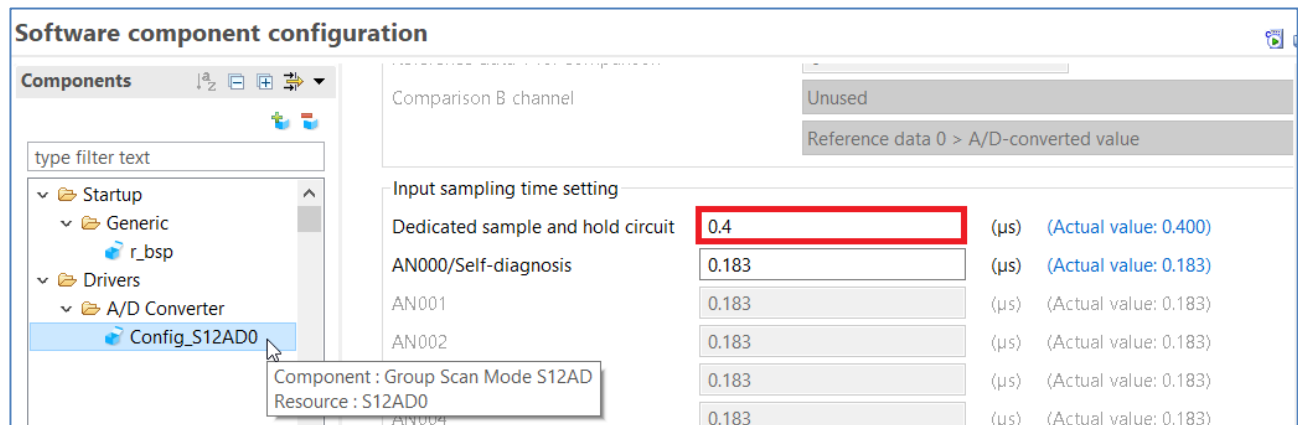
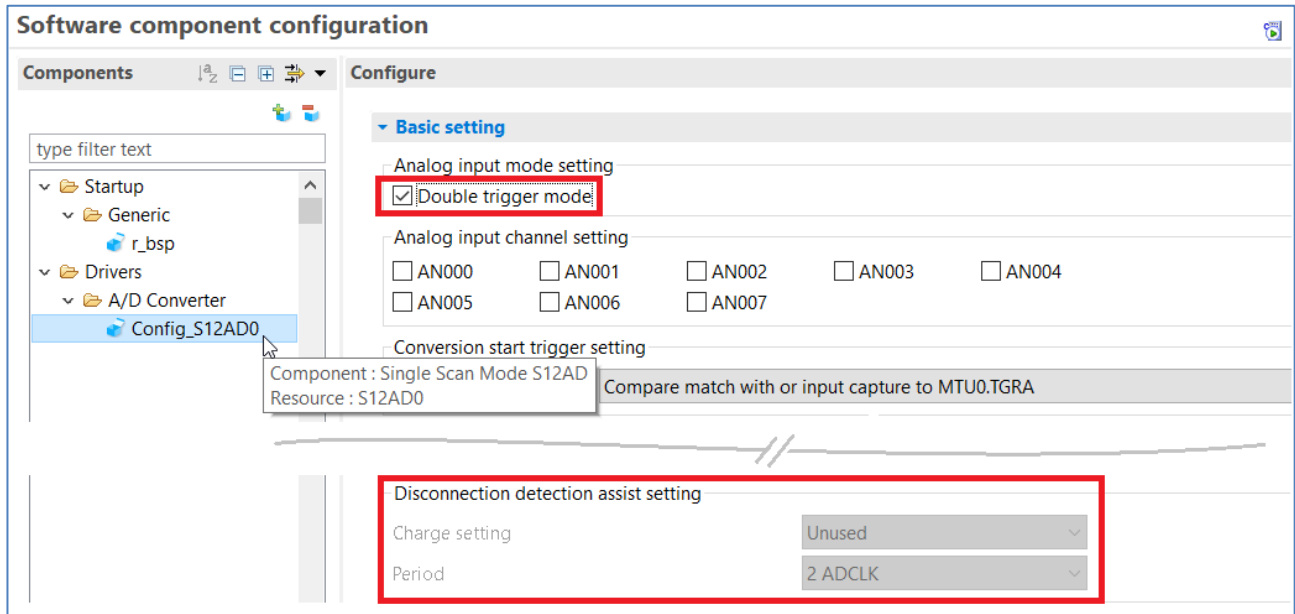


Figure 5-1 Dedicated sample and hold circuit setting

**5.2.3 Note on using double trigger mode in S12AD Single Scan Mode**

When Double trigger mode is used, Disconnection detection assist settings are grey off and cannot be configured. There is no workaround. This limitation will be fixed in next version. If you use the disconnection detection assist, please set to ADDISCR register.



**Figure 5-2 Disconnection detection assist setting**

Modification location :

Source file : < Single Scan Mode S12AD configuration name >.c

Function : R\_< Single Scan Mode S12AD configuration name >\_Create

```

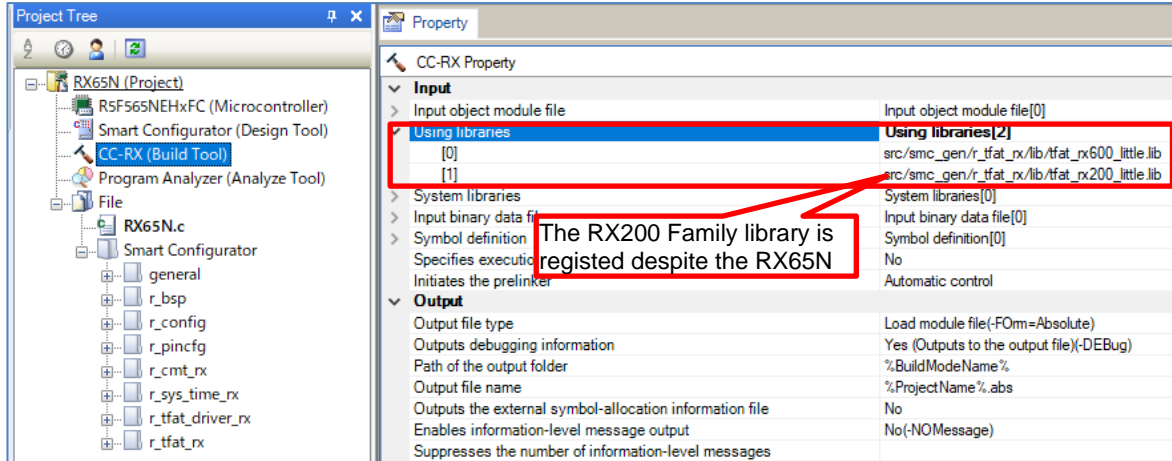
/*****
* Function Name: R_Config_S12AD0_Create
* Description  : This function initializes the S12AD channel
* Arguments   : None
* Return Value : None
*****/
void R_Config_S12AD0_Create (void)
{
    : (codes are omitted)
    /* Set S12AD control registers */
    S12AD.ADCSR.WORD = _0000_ADDBLTRIGGER_ENABLE |
                      _0000_AD_SYNCASYNCTRIG_DISABLE |
                      _0000_AD_SINGLE_SCAN_MODE;
    S12AD.ADDISCR.BYTE = _10_AD_DISCONNECT_PRE_CHARGE |
                        _02_AD_DISCONNECT_2ADCLK;
    S12AD.ADCER.WORD = _0000_AD_RESOLUTION_12BIT |
                      _0000_AD_AUTO_CLEARING_DISABLE |
                      _0000_AD_SELFDIAGST_DISABLE |
                      _0000_AD_RIGHT_ALIGNMENT;
    : (codes are omitted)
}
    
```

Add this

### 5.2.4 Note on using Library style FIT module

When using FIT modules provided by library style in the CS+ project, the build warning may occur because libraries other than the target device are added into CS+ CC-RX [Link Options]-[Using libraries] option. If the build warning occurs, please remove libraries other than the target device from [Link Options]-[Using libraries] option manually.

Example : When adding FIT module "r\_tfat\_rx" on RX65N project



### 5.2.5 Note on using SDRAM External Bus

When using SDRAM external bus (used SDCS) in BSC component with bus width set to "32 bits", the code to set PFBCR0.DH32E bit is not generated out. As workaround, manually add codes "\_20\_BSC\_DH32E\_ENABLED" to set DH32E bit.

Source file : < Buses configuration name>.c

Function : < Buses configuration name >\_Create

```

/*****
* Function Name: R_Config_BSC_Create
* Description  : This function initializes the BUSES module
* Arguments    : None
* Return Value : None
*****/
void R_Config_BSC_Create (void)
{
    : (codes are omitted)
    /* Set MPC registers for external bus interface */
    MPC.PFBCR0.BYTE |= ( _01_BSC_ADRLE_ENABLED |
                        _10_BSC_DHE_ENABLED |
                        _20_BSC_DH32E_ENABLED );
    MPC.PFBCR1.BYTE |= ( _10_BSC_MDSDE_ENABLED |
                        _40_BSC_DQM1E_ENABLED );
    : (codes are omitted)
}
    
```

Add this

## 6. Points for Caution

This section describes points for caution regarding the Smart Configurator for RX V2.3.0. Please refer to a document of each module about a caution of a FIT module.

### 6.1 List of Caution

Table 6-1 List of Caution

○: Applicable, /: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX13T	RX230_RX231	RX23E-A	RX23T	RX23W	RX24T_RX24U	RX64M	RX65N_RX651	RX66T	RX71M	RX72M	RX72T	Remarks
1	Note on configuring GPT interrupt	/	/	/	/	/	/	/	/	/	○	○	/	○	○	○	○	
2	Note on SCR.TE bit setting sequence in SCI Clock Synchronous Mode and SCI Clock Asynchronous Mode	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
3	Note on using only reception in SCI Clock Synchronous Mode	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
4	Notes on using high transfer speed in SCIF Synchronous Mode	/	/	/	/	/	/	/	/	/	/	○	/	/	○	/	/	
5	Note on device change functionality	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
6	Note on using Smart Configurator for RTOS project	/	/	/	○	/	○	/	/	/	/	○	○	○	○	○	○	Refer to FreeRTOS packages
7	Note on using Smart Configurator for GCC project in e <sup>2</sup> studio 7.4.0	○	○	○	○	○	○	○	○	/	○	○	○	○	○	/	○	
8	Note on using Data Transfer Controller	/	/	/	/	/	/	/	/	/	/	/	○	/	/	○	/	
9	Note on using Library style FIT module	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	



## 6.2 Details of Caution

### 6.2.1 Note on configuring GPT interrupts

The GPT interrupts are not specified as the Software Configurable Interrupt in the initial state even after the GPT interrupts are configured by GPT component. To specify GPT interrupts as Software Configurable Interrupt source, release unused Software Configurable interrupt source on the Interrupt sheet and allocate GPT interrupts instead.

### 6.2.2 Note on SCR.TE bit setting sequence in SCI Clock Synchronous Mode and SCI Clock Asynchronous Mode

Sequence of setting SCR.TE bit does not follow the usage note in User's Manual: Hardware. Instead, SCR.TE bit is set to 1 after changing the pin function to TXDn. Output of TXDn pin becomes high impedance.

Please connect a pull-up resistor to the TXDn line, prevent the TXDn line from becoming high impedance.

### 6.2.3 Note on using only reception in SCI Clock Synchronous Mode

In SCI Clock Synchronous Mode using internal clock, if only reception is enabled in high communication speed, extra clocks are generated even though reception has been completed. This is due to the delay in disabling RE to stop the clock after the desired number of data is received.

To prevent this issue, select Transmission/Reception work mode when using Smart Configurator. Use "R\_<Configuration Name>\_Serial\_Send\_Receive" function instead of "R\_<Configuration Name>\_Serial\_Receive". The same number of data for tx\_num and rx\_num should be specified. Disable TXDn pin in Smart Configurator Pins page and send dummy data if transmission is not required.

There will be warnings when TXDn pin is disabled. These warnings can be ignored as TXDn pin is not intended to be used originally.

Enabled	Function	Assignment	Pin Number	Direction	Remarks
<input type="checkbox"/>	CTS0#	Not assigned	Not assigned	None	
<input type="checkbox"/>	RTS0#	Not assigned	Not assigned	None	
<input checked="" type="checkbox"/>	RXD0	P33/EDREQ1/MTIOC0D/TIOC0D/TMRI3/PO11/POE4#...	K1	I	
<input checked="" type="checkbox"/>	SCK0	P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/ET0...	J3	IO	
<input type="checkbox"/>	TXD0	Not assigned	Not assigned	None	Component requires a pin

Description	Type
Pin (2 items)	
E04010002: TXD0 used by Config_SCI0 is not allocated to any pin.	Pin
E05000011: TXD0 requires a pin, please assign a pin to it at "Pins" page.	Pin

Figure 6-1 Ignore warnings when TXDn pin is disabled (Example with TXD0)

### 6.2.4 Note on using high transfer speed in SCIF Synchronous Mode

If the number of reception data specified for the API ( R\_<Configuration Name>\_Serial\_Receive or R\_<Configuration Name>\_Serial\_Send\_Receive ) and reception FIFO threshold specified on GUI do not satisfy the formula below:

$$(\text{Reception Data Size}) = n * (\text{Reception FIFO threshold}) \quad (n=1,2,3,\dots)$$

extra clock generation may occur after the desired number of data is received in high communication speed when using internal clock.

To prevent this issue, specify the reception data size and reception FIFO threshold that satisfy the formula.

### 6.2.5 Note on device change functionality

Save project settings before performing change device operation. After change device, perform these operations:

1. Visual check on Components window and Configuration Problems window. Resolve error and conflicts if there is any.
2. Check each component and converted settings.
3. Re-generate codes.

### 6.2.6 Note on using Smart Configurator for RTOS project

When using Smart Configurator for RTOS project, only FIT modules are supported. From Smart Configurator for RX V2.2.0, all FIT modules are displayed in "Add component" dialog by default.

### 6.2.7 Note on using Smart Configurator for GCC project in e<sup>2</sup> studio 7.4.0

When using default options to create new "GCC for Renesas RX Executable Project" with Smart Configurator in e<sup>2</sup> studio 7.4.0, build error occurs.

```
C:\example\src\smc_gen\r_bsp\mcu/all/r_bsp_common.h:55:24:  
fatal error: stdbool.h: No such file or directory
```

As workaround, use e<sup>2</sup> studio 7.5.0 to create new "GCC for Renesas RX Executable Project" with Smart Configurator.

### 6.2.8 Note on using Data Transfer Controller

Smart Configurator does not support sequence transfer, write-back skip, write-skip disable and displacement addition features.

### 6.2.9 Note on using Library style FIT module

Added Library style FIT modules into CS+ CC-RX [Link Options]-[Using libraries] option is not removed automatically even if Library type FIT modules are removed from the project. After removing FIT modules from the project, please remove related libraries from [Link Options]-[Using libraries] option manually.

**Revision History**

Rev.	Date	Description	
		Page	Summary
2.20	Jul.22 19	33	Create new
2.21	Oct.08.19	44	Update to Rev.2.2.1
2.30	Nov.05 19	27	Update to Rev.2.3.0
2.31	Nov.12 19	15	Add changes No.11, 12
		22	Add workaround

## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.4.0-1 November 2017)

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