

Smart Configurator for RL78 Plug-in in e² studio 2026-07

Smart Configurator for RL78 V1.18.0

Release Note

Introduction

Thank you for using the Smart Configurator for RL78.

This document describes the restrictions and points for caution. Read this document before using the product.

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1. Introduction

Smart Configurator is a utility for combining software to meet your needs. It supports the following three functions related to the embedding of Renesas drivers in your systems: importing middleware, generating driver code, and setting pins.

Smart Configurator for RL78 V1.18.0 is equivalent to Smart Configurator for RL78 Plug-in in e² studio 2026-07.

1.1 System Requirements

The operating environment is as follows.

1.1.1 Windows PC

- System: x64/x86 based processor
Windows® 11
- Memory capacity: We recommend 4 GB or more.
- Capacity of hard disk: At least 400 MB of free space.
- Display: Graphics resolution should be at least 1024 x 768, and the mode should display at least 65,536 colors.
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)

1.1.2 Linux PC

Smart Configurator for RL78 plug-in in e² studio 2023-01 or later is supported on Linux OS.

- System: x64 based processor, 2 GHz or faster (with multicore CPUs)
Ubuntu 24.04 LTS Desktop (64-bit version)
Ubuntu 22.04 LTS Desktop (64-bit version)
- Memory capacity: We recommend 2 GB or more.
- Capacity of hard disk: At least 2 GB of free space.

1.1.3 Mac OS

Smart Configurator for RL78 plug-in in e² studio 2026-04.1 or later is supported on Mac OS.

- System: Apple ARM-based systems-on-a-chip (SoCs)
Mac OS 26 (Tahoe)
Mac OS 15 (Sequoia)
- Memory capacity: We recommend 8 GB or more.
- Capacity of hard disk: At least 2 GB of free space.

1.1.4 Development Environments

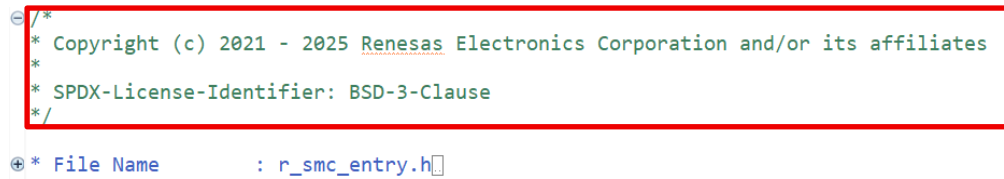
- Renesas Electronics Compiler for RL78 [CC-RL] V1.16 or later (Windows PC)
- Renesas Electronics Compiler for RL78 [CC-RL] V1.16.01 or later (Mac OS)
- LLVM for Renesas RL78 17.0.1.202512 or later (Windows PC, Linux PC, Mac OS)
- IAR Embedded Workbench for Renesas RL78 V5.20.2 or later (Windows PC)
- SMS Assembler V1.01.00 or later (Windows PC)
- FAA Assembler V1.06.00 or later (Windows PC)
- CS+ for CC V8.16.00 ^{Note1} or later (Windows PC)

Note:

1.Smart Configurator for RL78 V1.18.0 has been evaluated in the CS+ for CC V8.16.00 environment.
When using Smart Configurator for RL78 V1.17.0 or lower, please refer to Release Note [\(R20UT5808EC0100\)](#) about the target version of CS+ for CC.

1.2 Disclaimer

From Smart Configurator for RL78 V1.16.0, the disclaimer of generated code has been updated to BSD-3-Clause.



```
/*  
 * Copyright (c) 2021 - 2025 Renesas Electronics Corporation and/or its affiliates  
 *  
 * SPDX-License-Identifier: BSD-3-Clause  
 */  
  
* File Name      : r_smc_entry.h
```

Figure 1-1 Disclaimer of generated code

2. Support List

2.1 Support Devices List

Below is a list of devices supported by the Smart Configurator for RL78 V1.18.0.

Table 2-1 Support Devices (1/2)

Group (HW Manual number)	PIN	Device name
RL78/G23 Group (R01UH0896EJ0200)	30pin	R7F100GAFxSP, R7F100GAGxSP, R7F100GAHxSP, R7F100GAJxSP
	32pin	R7F100GBFxBP, R7F100GBGxBP, R7F100GBHxBP, R7F100GBJxBP, R7F100GBFxFP, R7F100GBGxFP, R7F100GBHxFP, R7F100GBJxFP, R7F104GBGxFP
	36pin	R7F100GCFxLA, R7F100GCGxLA, R7F100GCHxLA, R7F100GCJxLA
	40pin	R7F100GEFxBP, R7F100GEGxBP, R7F100GEHxBP, R7F100GEJxBP
	44pin	R7F100GFFxFP, R7F100GFGxFP, R7F100GFHxFP, R7F100GFJxFP, R7F100GFKxFP, R7F100GFLxFP, R7F100GFNxFP, R7F104GFJxFP
	48pin	R7F100GGFxFB, R7F100GGGxFB, R7F100GGHxFB, R7F100GGJxFB, R7F100GGKxFB, R7F100GGLxFB, R7F100GGNxFB, R7F100GGFxBP, R7F100GGGxBP, R7F100GGHxBP, R7F100GGJxBP, R7F100GGKxBP, R7F100GGLxBP, R7F100GGNxBP, R7F104GGJxFB
	52pin	R7F100GJFxFA, R7F100GJGxFA, R7F100GJHxFA, R7F100GJJxFA, R7F100GJKxFA, R7F100GJLxFA, R7F100GJNxFA
	64pin	R7F100GLFxFA, R7F100GLGxFA, R7F100GLHxFA, R7F100GLJxFA, R7F100GLKxFA, R7F100GLLxFA, R7F100GLNxFA, R7F100GLFxFB, R7F100GLGxFB, R7F100GLHxFB, R7F100GLJxFB, R7F100GLKxFB, R7F100GLLxFB, R7F100GLNxFB, R7F100GLFxFA, R7F100GLGxFA, R7F100GLHxFA, R7F100GLJxFA, R7F100GLKxFA, R7F100GLLxFA, R7F100GLNxFA
	80pin	R7F100GMGxFA, R7F100GMHxFA, R7F100GMJxFA, R7F100GMKxFA, R7F100GMLxFA, R7F100GMNxFA, R7F100GMGxFB, R7F100GMHxFB, R7F100GMJxFB, R7F100GMKxFB, R7F100GMLxFB, R7F100GMNxFB
	100pin	R7F100GPGxFB, R7F100GPHxFB, R7F100GPJxFB, R7F100GPKxFB, R7F100GPLxFB, R7F100GPNxFB, R7F100GPGxFA, R7F100GPHxFA, R7F100GPJxFA, R7F100GPKxFA, R7F100GPLxFA, R7F100GPNxFA
	128pin	R7F100GSJxFB, R7F100GSKxFB, R7F100GSLxFB, R7F100GSNxFB
RL78/F24 Group (R01UH0944EJ0100)	32pin	R7F124FBJ3xNP, R7F124FBJ4xNP, R7F124FBJ5xNP
	48pin	R7F124FGJ3xFB, R7F124FGJ4xFB, R7F124FGJ5xFB
	64pin	R7F124FLJ3xFB, R7F124FLJ4xFB, R7F124FLJ5xFB
	80pin	R7F124FMJ3xFB, R7F124FMJ4xFB, R7F124FMJ5xFB
	100pin	R7F124FPJ3xFB, R7F124FPJ4xFB, R7F124FPJ5xFB
RL78/G15 Group (R01UH0959EJ0140)	8pin	R5F12008xNS, R5F12007xNS, R5F12008xSN
	10pin	R5F12018xSP, R5F12017xSP
	16pin	R5F12048xNA, R5F12047xNA, R5F12048xSP, R5F12047xSP
	20pin	R5F12068xSP, R5F12067xSP, R5F12068xSM
RL78/F23 Group (R01UH0944EJ0100)	32pin	R7F123FBG3xNP, R7F123FBG4xNP, R7F123FBG5xNP
	48pin	R7F123FGG3xFB, R7F123FGG4xFB, R7F123FGG5xFB
	64pin	R7F123FLG3xFB, R7F123FLG4xFB, R7F123FLG5xFB
	80pin	R7F123FMG3xFB, R7F123FMG4xFB, R7F123FMG5xFB
RL78/G22 Group (R01UH0978EJ0100)	16pin	R7F102G4ExNP, R7F102G4CxNP
	20pin	R7F102G6ExSP, R7F102G6CxSP
	24pin	R7F102G7ExNP, R7F102G7CxNP
	25pin	R7F102G8ExLA, R7F102G8CxLA
	30pin	R7F102GAExSP, R7F102GACxSP
	32pin	R7F102GBExNP, R7F102GBCxNP, R7F102GBExFP, R7F102GBCxFP
	36pin	R7F102GCExLA, R7F102GCCxLA
	40pin	R7F102GEEExNP, R7F102GECxNP
	44pin	R7F102GFEExFP, R7F102GFCxFP
	48pin	R7F102GGEExFB, R7F102GGEExNP, R7F102GGCxFB, R7F102GGCxNP

Table 2-2 Support Devices (2/2)

Group (HW Manual number)	PIN	Device name
RL78/G24 Group (R01UH0961EJ0100)	20pin	R7F101G6GxSP, R7F101G6ExSP
	24pin	R7F101G7GxNP, R7F101G7ExNP
	25pin	R7F101G8GxLA, R7F101G8ExLA
	30pin	R7F101GAGxSP, R7F101GAExSP
	32pin	R7F101GBGxNP, R7F101GBExNP, R7F101GBGxFP, R7F101GBExFP
	40pin	R7F101GEGxNP, R7F101GEEExNP
	44pin	R7F101GFGxFP, R7F101GFEExFP
	48pin	R7F101GGGxFB, R7F101GGEExFB, R7F101GGGxNP, R7F101GGEExNP
	52pin	R7F101GJGxFA, R7F101GJExFA
	64pin	R7F101GLGxFA, R7F101GLGxFB, R7F101GLEExFA, R7F101GLEExFB
RL78/G16 Group (R01UH0980EJ0130)	10pin	R5F1211AxSP, R5F1211CxSP
	16pin	R5F1214AxNA, R5F1214AxSP, R5F1214CxNA, R5F1214CxSP
	20pin	R5F1216AxSP, R5F1216CxSP, R5F1216CxSM
	24pin	R5F1217AxNA, R5F1217CxNA
	32pin	R5F121BAxFP, R5F121BAxNA, R5F121BCxFP, R5F121BCxNA
RL78/F25 Group (R01UH1061EJ0050)	48pin	R7F125FGL3xFB, R7F125FGL4xFB
	64pin	R7F125FLL3xFB, R7F125FLL4xFB
	80pin	R7F125FML3xFB, R7F125FML4xFB
	100pin	R7F125FPL3xFB, R7F125FPL4xFB
RL78/F22 Group (R01UH1061EJ0050)	24pin	R7F122F7G3xNP, R7F122F7G4xNP
	32pin	R7F122FBG3xNP, R7F122FBG4xNP
	48pin	R7F122FGG3xFB, R7F122FGG4xFB
RL78/L23 Group (R01UH1082EJ0100)	44pin	R7F100LFJxFP, R7F100LFLxFP, R7F100LFG, R7F100LFE
	48pin	R7F100LGJxFB, R7F100LGJxNP, R7F100LGLxFB, R7F100LGLxNP, R7F100LGG, R7F100LGE
	52pin	R7F100LJJxFA, R7F100LJLxFA, R7F100LJG, R7F100LJE
	64pin	R7F100LLJxFA, R7F100LLJxFB, R7F100LLLxFA, R7F100LLLxFB, R7F100LLG, R7F100LLE
	80pin	R7F100LMGxFA, R7F100LMGxFB, R7F100LMJxFA, R7F100LMJxFB, R7F100LMLxFA, R7F100LMLxFB
	100pin	R7F100LPGxFA, R7F100LPGxFB, R7F100LPJxFA, R7F100LPJxFB, R7F100LPLxFA, R7F100LPLxFB
RL78/G21 Group (R01UH1177EJ0100)	20pin	R7F103G6GxSP, R7F103G6JxSP
	32pin	R7F103GBGxFP, R7F103GBJxFP
	44pin	R7F103GFGxFP, R7F103GFJxFP
	48pin	R7F103GGGxFB, R7F103GGJxFB
	64pin	R7F103GLGxFA, R7F103GLGxFB, R7F103GLJxFA, R7F103GLJxFB

2.2 Support Components List

Below is a list of Components supported by the Smart Configurator for RL78 V1.18.0.

Table 2-3 Support Components (1/3)

✓ : Support, -: Non-support

No	Components	Mode	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
1	12 Bit A/D Single Scan	-	-	✓	-	✓	-	-	-	✓	
2	12 Bit A/D Continuous Scan	-	-	✓	-	✓	-	-	-	✓	
3	12 Bit A/D Group Scan	-	-	✓	-	✓	-	-	-	✓	
4	A/D Converter	Normal mode	✓	-	✓	-	✓	✓	✓	-	Only RL78/G24 A/D converter has mode selection GUI. For other devices, the default mode is "Normal mode" and no GUI is provided for mode selection.
		Advanced mode	-	-	-	-	-	-	✓	-	
5	Clock Output/Buzzer Output-Controller	-	✓	✓	✓	✓	✓	✓	✓	✓	
6	Comparator	-	✓	✓	✓	-	-	✓	✓	✓	
7	D/A Converter	-	✓	✓	-	-	-	-	✓	✓	
8	Data Transfer Controller	-	✓	✓	-	✓	✓	-	✓	✓	
9	Delay Counter	-	✓	✓	✓	✓	✓	✓	✓	✓	
10	Divider Function	-	✓	✓	✓	✓	✓	✓	✓	✓	
11	Event Link Controller	-	-	✓	-	-	✓	-	✓	✓	
12	External Event Counter	-	✓	✓	✓	✓	✓	✓	✓	✓	
13	IIC Communication (Master mode)	-	✓	✓	✓	✓	✓	✓	✓	✓	
14	IIC Communication (Master mode, EEPROM communication)	-	✓	✓	✓	✓	✓	✓	✓	✓	
15	IIC Communication (Slave mode)	-	✓	✓	✓	✓	✓	✓	✓	✓	
16	Input Capture Function	-	-	✓	-	✓	-	-	✓	✓	
17	Input Pulse Interval/Period Measurement	-	✓	✓	✓	✓	✓	✓	✓	✓	
18	Input Signal High-/Low-Level Width Measurement	-	✓	✓	✓	✓	✓	✓	✓	✓	
19	Interrupt Controller	-	✓	✓	✓	✓	✓	✓	✓	✓	
20	Interval Timer	8 bit count mode	✓	✓	✓	✓	✓	✓	✓	✓	
		12 bit count mode	-	-	✓	-	-	✓	-	-	
		16 bit count mode	✓	✓	✓	✓	✓	✓	✓	✓	
		16 bit capture mode	✓	-	-	-	✓	-	✓	-	
		32 bit count mode	✓	-	-	-	✓	-	✓	-	
21	Key Interrupt	-	✓	✓	-	✓	✓	-	✓	✓	
22	One-Shot Pulse Output	One-Shot Pulse Output	✓	✓	✓	✓	✓	✓	✓	✓	
		Two-Channel Input with One-Shot Pulse Output	-	-	✓	-	-	✓	-	-	
23	Output Compare Function	-	-	✓	-	✓	-	-	✓	✓	
24	Ports	-	✓	✓	✓	✓	✓	✓	✓	✓	
25	PWM Option Unit A	-	-	✓	-	✓	-	-	✓	✓	

Table 2-4 Support Components (2/3)

✓ : Support, -: Non-support

No	Components	Mode	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
26	DALI Communication (Control devices)	-	-	-	-	-	-	-	✓	-	
27	DALI Communication (Control gear)	-	-	-	-	-	-	-	✓	-	
28	Real-Time Clock	-	✓	✓	-	✓	✓	✓	✓	✓	
29	PWM Output	PWM Mode	✓	✓	✓	✓	✓	✓	✓	✓	
		PWM3 Mode	-	✓	-	✓	-	-	✓	✓	
		Extended PWM Mode	-	✓	-	✓	-	-	✓	✓	
		PWM2 Mode	-	-	-	-	-	-	✓	-	
		Timer KB3 PWM Output Gate Mode	-	-	-	-	-	-	✓	-	
		Standalone Mode (Period controlled by the TKBCRn0 register)	-	-	-	-	-	-	✓	-	
		Standalone Mode (Period controlled by external trigger input)	-	-	-	-	-	-	✓	-	
		Simultaneous Start/Stop Mode (Period controlled by the TKBCRn0 register)	-	-	-	-	-	-	✓	-	
		Simultaneous Start/Stop Mode (Period controlled by external trigger input)	-	-	-	-	-	-	✓	-	
		Simultaneous Start/Clear Mode (Period controlled by master)	-	-	-	-	-	-	✓	-	
		Interleaved PFC Output Mode	-	-	-	-	-	-	✓	-	
		Remote Control Function	-	-	-	-	-	-	-	-	
30	Remote Control Signal Receiver	-	✓	-	-	-	-	-	-	-	
31	SNOOZE Mode Sequencer	-	✓	-	-	-	✓	-	-	-	
32	SPI (CSI) Communication	Transmission	✓	✓	✓	✓	✓	✓	✓	✓	
		Reception	✓	✓	✓	✓	✓	✓	✓	✓	
		Transmission/reception	✓	✓	✓	✓	✓	✓	✓	✓	
33	Square Wave Output	-	✓	✓	✓	✓	✓	✓	✓	✓	
34	Three-phase PWM Output	Reset Synchronous PWM Mode	-	✓	-	✓	-	-	✓	✓	
		Complementary PWM Mode	-	✓	-	✓	-	-	✓	✓	
		Extended Complementary PWM Mode	-	✓	-	✓	-	-	✓	✓	
35	UART Communication	Transmission	✓	✓	✓	✓	✓	✓	✓	✓	
		Reception	✓	✓	✓	✓	✓	✓	✓	✓	
		Transmission/reception	✓	✓	✓	✓	✓	✓	✓	✓	
36	Voltage Detector	-	✓	✓	-	✓	✓	-	✓	✓	
37	Watchdog Timer	-	✓	✓	✓	✓	✓	✓	✓	✓	
38	Logic & Event Link Controller	-	✓	-	-	-	-	-	-	-	To use ELCL modules of fixed function, need download in Smart Configurator RL78.

Table 2-5 Support Components (3/3)

✓ : Support, -: Non-support

No	Components	Mode	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
39	Phase Counting Mode	-	-	-	-	-	-	-	✓	-	
40	Programmable Gain Amplifier	-	-	-	-	-	-	-	✓	-	
41	Flexible Application Accelerator	-	-	-	-	-	-	-	✓	-	
42	LCD Controller / Driver	-	-	-	-	-	-	-	-	-	
43	Oscillation Stop Detector	-	-	-	-	-	-	-	-	-	
44	External Signal Sampler	-	-	-	-	-	-	-	-	-	

Table 2-6 Support Components (1/3)

✓: Support, -: Non-support

No	Components	Mode	RL78/F22	RL78/L23	RL78/G21	Remarks
1	12 Bit A/D Single Scan	-	✓	-	-	
2	12 Bit A/D Continuous Scan	-	✓	-	-	
3	12 Bit A/D Group Scan	-	✓	-	-	
4	A/D Converter	Normal mode	-	✓	✓	Only RL78/G24 A/D converter has mode selection GUI. For other devices, the default mode is "Normal mode" and no GUI is provided for mode selection.
		Advanced mode	-	-	-	
5	Clock Output/Buzzer Output Controller	-	✓	✓	-	
6	Comparator	-	-	✓	-	
7	D/A Converter	-	-	✓	-	
8	Data Transfer Controller	-	✓	✓	-	
9	Delay Counter	-	✓	✓	✓	
10	Divider Function	-	✓	✓	✓	
11	Event Link Controller	-	-	-	-	
12	External Event Counter	-	✓	✓	✓	
13	IIC Communication (Master mode)	-	✓	✓	✓	
14	IIC Communication (Master mode, EEPROM communication)	-	✓	✓	✓	
15	IIC Communication (Slave mode)	-	✓	✓	✓	
16	Input Capture Function	-	✓	-	-	
17	Input Pulse Interval/Period Measurement	-	✓	✓	✓	
18	Input Signal High-/Low-Level Width Measurement	-	✓	✓	✓	
19	Interrupt Controller	-	✓	✓	✓	
20	Interval Timer	8 bit count mode	✓	✓	✓	
		12 bit count mode	-	-	-	
		16 bit count mode	✓	✓	✓	
		16 bit capture mode	-	✓	✓	
		32 bit count mode	-	✓	✓	
21	Key Interrupt	-	✓	✓	✓	
22	One-Shot Pulse Output	One-Shot Pulse Output	✓	✓	✓	
		Two-Channel Input with One-Shot Pulse Output	-	-	-	
23	Output Compare Function	-	✓	-	-	
24	Ports	-	✓	✓	✓	
25	PWM Option Unit A	-	✓	-	-	
26	DALI Communication (Control devices)	-	-	-	-	
27	DALI Communication (Control gear)	-	-	-	-	
28	Real-Time Clock	-	✓	✓	-	

Table 2-7 Support Components (2/3)

✓ : Support, -: Non-support

No	Components	Mode	RL78/F22	RL78/L23	RL78/G21	Remarks
29	PWM Output	PWM Mode	✓	✓	✓	
		PWM3 Mode	✓	-	-	
		Extended PWM Mode	✓	-	-	
		PWM2 Mode	-	-	-	
		Timer KB3 PWM Output Gate Mode	-	-	-	
		Standalone Mode (Period controlled by the TKBCRn0 register)	-	✓	-	
		Standalone Mode (Period controlled by external trigger input)	-	✓	-	
		Simultaneous Start/Stop Mode (Period controlled by the TKBCRn0 register)	-	✓	-	
		Simultaneous Start/Stop Mode (Period controlled by external trigger input)	-	✓	-	
		Simultaneous Start/Clear Mode (Period controlled by master)	-	✓	-	
		Interleaved PFC Output Mode	-	✓	-	
		Remote Control Function	-	✓	-	
30	Remote Control Signal Receiver	-	-	-	-	
31	SNOOZE Mode Sequencer	-	-	✓	-	
32	SPI (CSI) Communication	Transmission	✓	✓	✓	
		Reception	✓	✓	✓	
		Transmission/reception	✓	✓	✓	
33	Square Wave Output	-	✓	✓	✓	
34	Three-phase PWM Output	Reset Synchronous PWM Mode	✓	-	-	
		Complementary PWM Mode	✓	-	-	
		Extended Complementary PWM Mode	✓	-	-	
35	UART Communication	Transmission	✓	✓	✓	
		Reception	✓	✓	✓	
		Transmission/reception	✓	✓	✓	
36	Voltage Detector	-	✓	✓	✓	
37	Watchdog Timer	-	✓	✓	✓	
38	Logic & Event Link Controller	-	-	✓	-	To use ELCL modules of fixed function, need download in Smart Configurator RL78.
39	Phase Counting Mode	-	-	-	-	
40	Programmable Gain Amplifier	-	-	-	-	
41	Flexible Application Accelerator	-	-	-	-	

Table 2-8 Support Components (3/3)

✓ : Support, -: Non-support

No	Components	Mode	RL78/F22	RL78/L23	RL78/G21	Remarks
42	LCD Controller / Driver	-	-	✓	-	
43	Oscillation Stop Detector	-	-	✓	-	
44	External Signal Sampler	-	-	✓	-	

2.3 New support

2.3.1 BSP (Board Support Package) revision update

BSP rev2.00 is supported and will be added as default BSP when creating Smart Configurator project.

2.3.2 Support RL78/G23 devices

From Smart Configurator for RL78 V1.18.0, the following RL78/G23 chips are supported: R7F104GBGxFP, R7F104GFJxFP, R7F104GGJxFB. Please see 2.1 Support Devices List for details on supported packages.

2.3.3 Support RL78/G15 devices

From Smart Configurator for RL78 V1.18.0, the following RL78/G15 chips are supported: R5F12068xSM. Please see 2.1 Support Devices List for details on supported packages.

2.3.4 Support RL78/G16 devices

From Smart Configurator for RL78 V1.18.0, the following RL78/G16 chips are supported: R5F1216CxSM. Please see 2.1 Support Devices List for details on supported packages.

2.3.5 Support RL78/G21 devices

Please see 2.1 Support Devices List for details on supported packages.

3. Changes

This chapter describes changes to the Smart Configurator for RL78 V1.18.0.

3.1 Correction of issues/limitations

Table 3-1 List of Correction of issues/limitations (1/2)

✓ : Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
1	Fixed the issue of not saving user's code after re-generating code for ELCL flexible circuit component	✓	-	-	-	-	-	-	-	
2	Fixed the issue of fHP value is wrong in Clock page	-	-	-	-	-	-	✓	-	
3	Fixed the issue of setting 64/48 MHz as operation clock in 32-bit Interval Timer	-	-	-	-	-	-	✓	-	
4	Fixed the issue of not correcting the errors in the User's Manual	-	-	-	-	-	✓	-	-	

Table 3-2 List of Correction of issues/limitations (2/2)

✓ : Applicable, -: Not Applicable

No	Description	RL78/F22	RL78/L23	RL78/G21	Remarks
1	Fixed the issue of not saving user's code after re-generating code for ELCL flexible circuit component	-	✓	-	
2	Fixed the issue of fHP value is wrong in Clock page	-	-	-	
3	Fixed the issue of setting 64/48 MHz as operation clock in 32-bit Interval Timer	-	✓	-	
4	Fixed the issue of not correcting the errors in the User's Manual	-	-	-	

3.1.1 Fixed the issue of not saving user's code after re-generating code for ELCL flexible circuit component

From Smart Configurator for RL78 V1.18.0, the user's code will not be removed between user code area after re-generating code.

```
void R_Config_ELCL_Create_UserInit(void)
{
    /* Start user code for user init. Do not edit comment generated here */
    NOP();
    /* End user code. Do not edit comment generated here */
}
```

Figure 3-1 User's code between user code area

3.1.2 Fixed the issue of fIHP value is wrong in Clock page

In some configurations, the fIHP value was displayed incorrectly. From Smart Configurator for RL78 V1.18.0, Smart Configurator fixed this issue. Please refer to **Figure 3-3** for detailed information about under which setting fIHP has error.

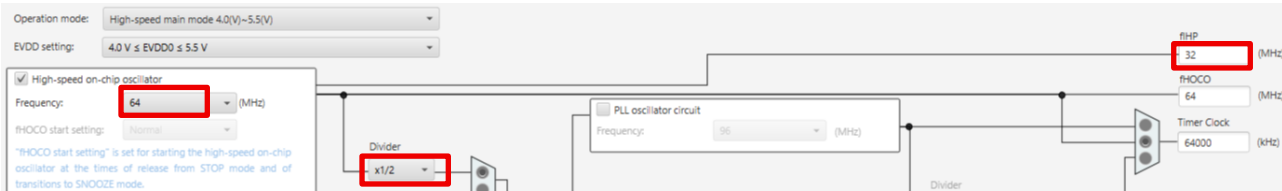


Figure 3-2 fHOCO value, fIHP value and Divider in Clock page

fHOCO	Divider	fIHP (before)	fIHP (after)
64MHz	x1/2	32MHz	64MHz
32MHz	x1/2	32MHz	64MHz
16MHz	x1/2	32MHz	64MHz
8MHz	x1/2	32MHz	64MHz
4MHz	x1/2	32MHz	64MHz
2MHz	x1/2	32MHz	64MHz

Figure 3-3 fIHP value in Clock page

3.1.3 Fixed the issue of setting 64/48 MHz as operation clock in 32-bit Interval Timer

When fIHP is set to 64/48 MHz in Clock page, it shouldn't select fIHP as "Operation clock (fITL0)" and set fITL0 as "Clock source" for 8-bit/16-bit/32-bit Interval Timer function or 16-bit Capture Timer function. From Smart Configurator for RL78 V1.18.0, Smart Configurator fixed this issue.

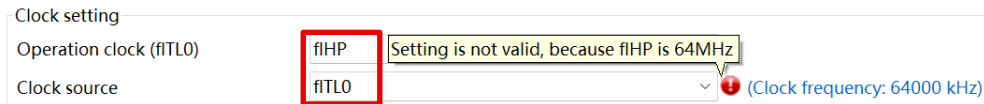


Figure 3-4 Set clock source as 64MHz

When fIHP is set to 64/48 MHz in Clock page, it shouldn't select fIHP as "Operation clock (fITL1)" for 16-bit Capture Timer function. From Smart Configurator for RL78 V1.18.0, Smart Configurator fixed this issue.

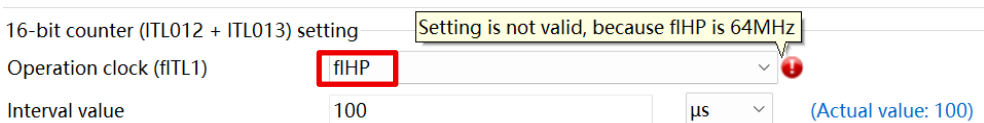


Figure 3-5 Set operation clock as 64MHz

3.1.4 Fixed the issue of not correcting the errors in the User's Manual

There are some errors in RL78/G16 User's Manual (R01UH0980EJ0130). Smart Configurator corrects these errors from Smart Configurator for RL78 V1.18.0 according to [TN-RL*-A0150A/E](#). The modified pin setting code of peripheral functions are PORT, CSI, INTP, TAU.

3.2 Specification changes

Table 3-3 List of Specification changes (1/2)

✓: Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
1	Improvement for blinky sample project	-	-	-	-	-	-	-	-	
2	Improvement for the specification according to RL78G23 User's Manual Hardware from V1.20 to V2.00	✓	-	-	-	-	-	-	-	
3	Improvement for the specification according to RL78G15 User's Manual Hardware from V1.00 to V1.40	-	-	✓	-	-	-	-	-	
4	Improvement for the specification according to RL78G16 User's Manual Hardware from V1.00 to V1.30	-	-	-	-	-	✓	-	-	

Table 3-4 List of Specification changes (2/2)

✓: Applicable, -: Not Applicable

No	Description	RL78/F22	RL78/L23	RL78/G21	Remarks
1	Improvement for blinky sample project	-	-	✓	
2	Improvement for the specification according to RL78G23 User's Manual Hardware from V1.20 to V2.00	-	-	-	
3	Improvement for the specification according to RL78G15 User's Manual Hardware from V1.00 to V1.40	-	-	-	
4	Improvement for the specification according to RL78G16 User's Manual Hardware from V1.00 to V1.30	-	-	-	

3.2.1 Improvement for blinky sample project

Smart Configurator improves to support blinky sample project with blink 2 LEDs by using TAU interval timer to get different frequency.

```
volatile uint32_t count = 0; /* use count to toggle alternatively 2 LEDs */

int main(void)
{
    EI();
    /* Start SW Interrupt */
    R_Config_INTC_INTP0_Start();

    /* Start TAU0 channel0 */
    R_Config_TAU0_0_Start();

    /* WAIT_LOOP */
    while (1) {
        while (0 == g_tau_interrupt_flag);

        g_tau_interrupt_flag = 0;
        count++;

        /* Write to the first LED pin */
        PIN_WRITE(LED1) = ~PIN_READ(LED1);

        if ((count % 2) == 0) {
            /* Write to the second LED pin */
            PIN_WRITE(LED2) = ~PIN_READ(LED2);
        }
    }

    return 0;
}
```

Figure 3-6 Improved code of blinky sample project

3.2.2 Improvement for the specification according to RL78G23 User's Manual Hardware from V1.20 to V2.00

Improved the specification according to RL78G23 User's Manual Hardware V2.00. Please refer to chapter "REVISION HISTORY" in User's Manual Hardware for detail.

3.2.3 Improvement for the specification according to RL78G15 User's Manual Hardware from V1.00 to V1.40

Improved the specification according to RL78G15 User's Manual Hardware V1.40. Please refer to chapter "REVISION HISTORY" in User's Manual Hardware for detail.

3.2.4 Improvement for the specification according to RL78G16 User's Manual Hardware from V1.00 to V1.30

Improved the specification according to RL78G16 User's Manual Hardware V1.30. Please refer to chapter "REVISION HISTORY" in User's Manual Hardware for detail.

4. List of RENESAS TOOL NEWS AND TECHNICAL UPDATE

Below is a list of notifications delivered by RENESAS TOOL NEWS and TECHNICAL UPDATE.

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Oct. 01, 2021	R20TS0757	1. Notes on creating LLVM for Renesas RL78 C/C++ Executable Project 2. Notes on using Port Input buffer function https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rl78	RL78/G23	V1.2.0
Mar. 16, 2022	R20TS0822	1. Notes when build or clean e ² studio Smart Configurator project https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rl78-0	RL78/G23	V1.3.0
Dec. 01, 2022	R20TS0895	1. Notes when changing version of Board Support Program (BSP) or RL78 Software Integration System (SIS) modules https://www.renesas.com/us/en/document/tnn/notes-e-studio-smart-configurator-rl78-plug-smart-configurator-rl78	RL78/G23 RL78/F24 RL78/G15	V1.5.0

5. Points for Limitation

This section describes points for limitation regarding the Smart Configurator for RL78 V1.18.0.

5.1 List of Limitation

Table 5-1 List of Limitation (1/2)

✓: Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
1	Note on extra help document issue	✓	✓	✓	✓	✓	✓	✓	✓	
2	Note on ELCL D flip flop component GUI warning display incorrectly	✓	-	-	-	-	-	-	-	
3	Note on the unsupported setting items for some ELCL components	✓	-	-	-	-	-	-	-	
4	Note on the user code protection feature will only be supported on the files that are generated by the Code Generation component	✓	✓	✓	✓	✓	✓	✓	✓	
5	Note on UI display with High Contrast theme on Linux OS	✓	✓	✓	✓	✓	✓	✓	✓	
6	Note on emulator setting in System page	-	✓	-	✓	-	-	-	✓	
7	Note on the default value of voltage boosting pin in LCD	-	-	-	-	-	-	-	-	
8	Note on the pin occupation in LCD	-	-	-	-	-	-	-	-	
9	Note on the disappearance of assembler macro definition	✓	✓	✓	✓	✓	✓	✓	✓	

Table 5-2 List of Limitation (2/2)

✓: Applicable, -: Not Applicable

No	Description	RL78/F22	RL78/L23	RL78/G21	Remarks
1	Note on extra help document issue	✓	✓	✓	
2	Note on ELCL D flip flop component GUI warning display incorrectly	-	-	-	
3	Note on the unsupported setting items for some ELCL components	-	-	-	
4	Note on the user code protection feature will only be supported on the files that are generated by the Code Generation component	✓	✓	✓	
5	Note on UI display with High Contrast theme on Linux OS	✓	✓	✓	
6	Note on emulator setting in System page	✓	-	-	
7	Note on the default value of voltage boosting pin in LCD	-	✓	-	
8	Note on the pin occupation in LCD	-	✓	-	
9	Note on the disappearance of assembler macro definition	✓	✓	✓	

5.2 Details of Limitation

5.2.1 Note on extra help document issue

For Smart Configurator, there is an extra help “Smart Browser” under “[Help] > [Help Contents]”. Please ignore it.

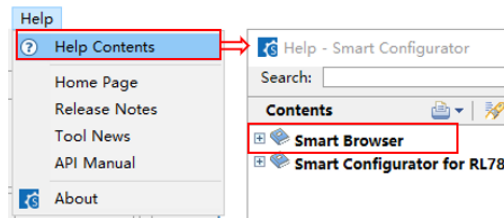


Figure 5-1 Extra help issue

5.2.2 Note on ELCL D flip flop component GUI warning display incorrectly

When selecting the event signal in ELCL D flip flop component, even if the selected signal consists with the hardware specification, there still displays the warning on the GUI.

[Workaround]

Make reference to the hardware manual and set the selectable event signal though warning appeared in GUI, the warning is no impact for the code generation.

The following is example of using flip-flop 0 and flip-flop 1 in ELCL logic cell block L1.

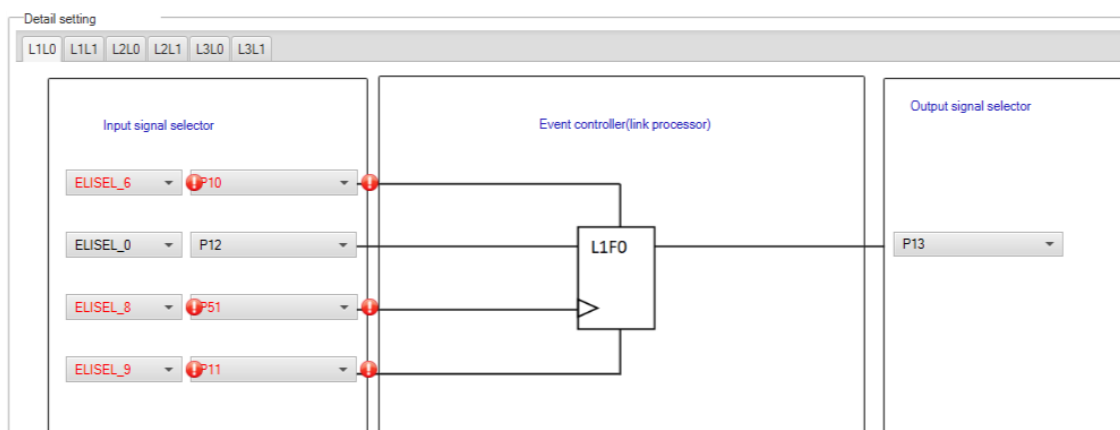


Figure 5-2 The flip-flop 0 in ELCL logic cell block L1 usage example

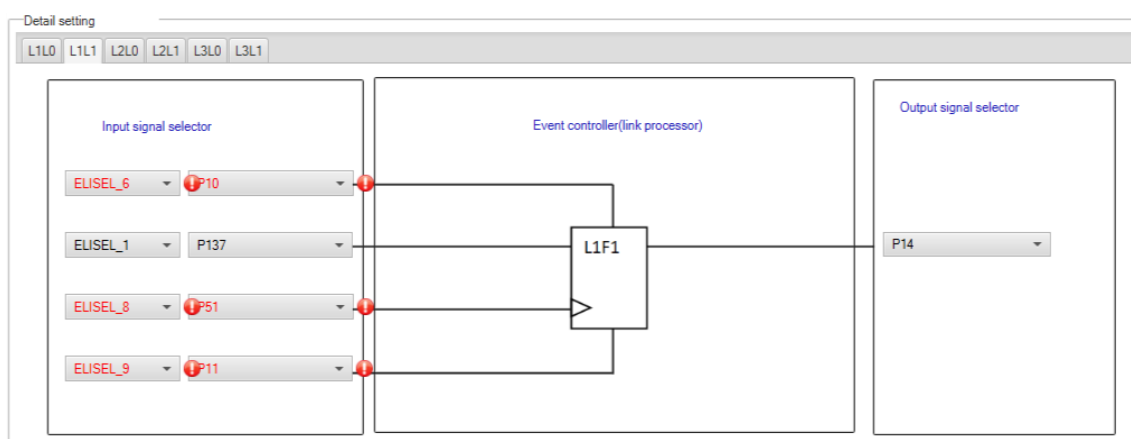


Figure 5-3 The flip-flop 1 in ELCL logic cell block L1 usage example

5.2.3 Note on the unsupported setting items for some ELCL components

In the following ELCL modules, it is not possible to set “no selection (fixed to 0)” as the input signal of the logic cell block and “negative logic output (inverted)” as the output level of the event signal.

- ELCL AND
- ELCL D flip flop
- ELCL EXOR
- ELCL selector
- ELCL Through

[Workaround] None

5.2.4 Note on the user code protection feature will only be supported on the files that are generated by the Code Generation component

The user code protection feature will only be supported on the files that are generated by the Code Generation component. Hence, the user code protection feature is not available for non-Code Generation components.

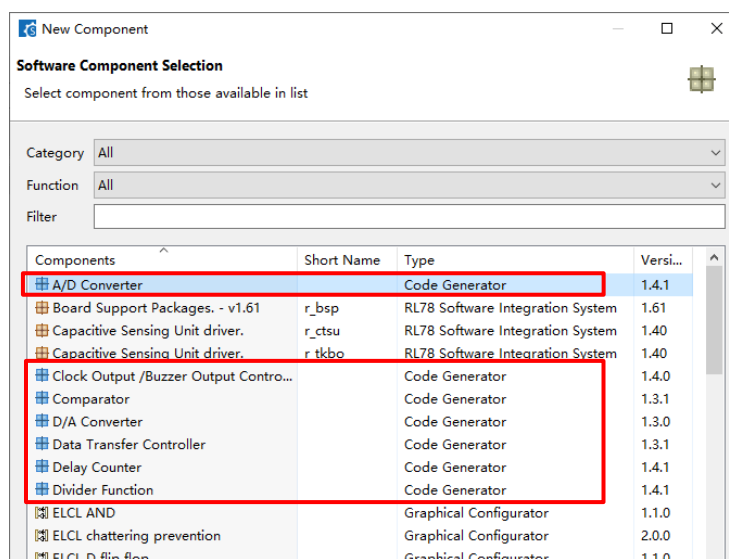


Figure 5-4 Code Generation component in red frame

5.2.5 Note on UI display with High Contrast theme on Linux OS

When using e² studio with High Contrast theme on Linux OS, some display texts of Smart Configurator can't be seen. To avoid this issue, please use other themes.

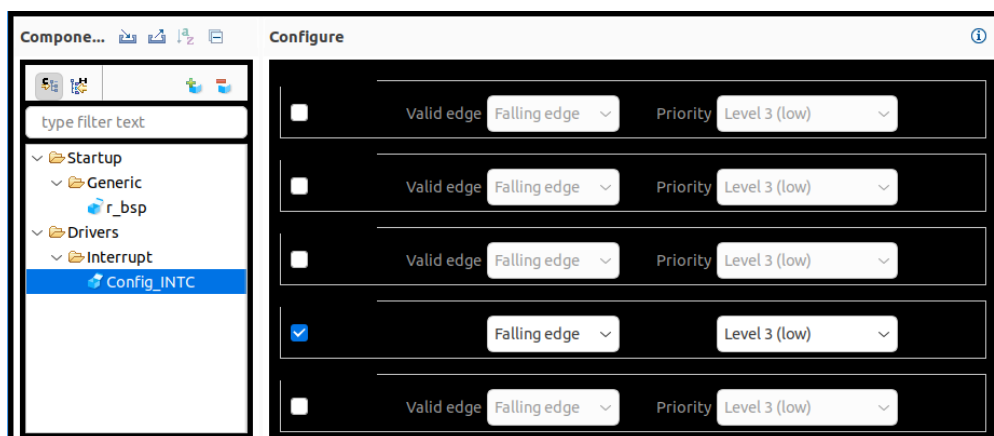


Figure 5-5 UI display with High Contrast theme

5.2.6 Note on emulator setting in System page

Smart Configurator shouldn't support emulator E20. It will be removed in next Smart Configurator release.

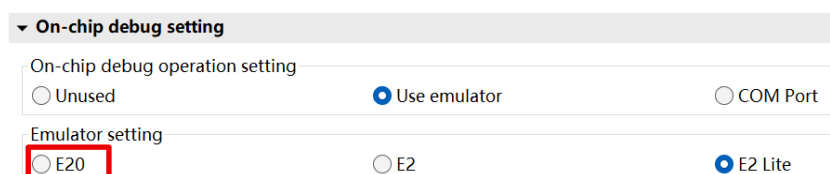


Figure 5-6 Emulator E20 in System page

5.2.7 Note on the default value of voltage boosting pin in LCD

Smart Configurator set a wrong value to the default value of voltage boosting pin when using external resistance division method or capacitor split method. It will be fixed in next Smart Configurator release.

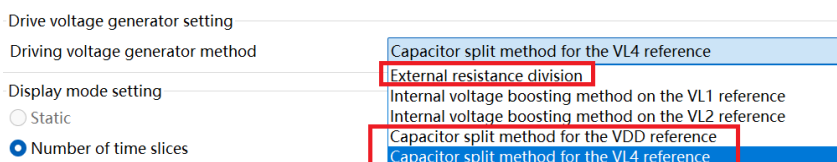


Figure 5-7 Driving voltage generator method

[Workaround]

Change the content of R_Config_LCD_Create() function manually. If code generation is executed again after adding the code, the code will be overwritten, so be caution.

[Current]

```
LCDON = 0U; /* display off (all segment outputs are deselected) */
LCDVLM = 1U; /* VDD voltage is 4.2 V or less */
LCDM0 = (_20_LCD_DISPLAY_WAVEFORM_B | _14_LCD_TIMESLICE_8 | _01_LCD_BIAS_MODE_3);
LCDM0 |= _00_LCD_VOLTAGE_MODE_EXTERNAL;
```

[Expect]

```
LCDON = 0U; /* display off (all segment outputs are deselected) */
LCDVLM = 0U; /* VDD voltage is 2.7 V or higher */
LCDM0 = (_20_LCD_DISPLAY_WAVEFORM_B | _14_LCD_TIMESLICE_8 | _01_LCD_BIAS_MODE_3);
LCDM0 |= _40_LCD_VOLTAGE_MODE_INTERNAL;
```

5.2.8 Note on the pin occupation in LCD

In some configurations, the pin occupation is wrong. It will be fixed in next Smart Configurator release.

Display waveform setting

Type A waveform

Type B waveform

Drive voltage generator setting

Driving voltage generator method

External resistance division

Display mode setting

Static

Number of time slices

2 (1/2 bias mode)

Figure 5-8 Display mode setting

[Workaround]
Change the pin occupation in Pins page manually refer to **Table 5-3** and ignore the pin error information.

Pin Function				
type filter text (* = any string, ? = any character)				
All				
Enabled	Function	PIOR	Assignment	Pin Number
☐	CAPH		Not assigned	Not assigned
☐	CAPL		Not assigned	Not assigned
☒	COM0		P90/COM0/TS31/TI00/TO00/INTP1	66
☒	COM1		P91/COM1/TS30/INTP2	65
☒	COM2		P92/COM2/TS29/TI01/TO01	64
☒	COM3		P93/COM3/TS28/INTP3/SCK01/SCL01	63
☐	COM4		Not assigned	Not assigned
☐	COM5		Not assigned	Not assigned
☐	COM6		Not assigned	Not assigned
☐	COM7		Not assigned	Not assigned
☒	SEG0		P94/COM4/SEG0/TS27/INTP2/SI01/SDA01/TIO0	62
☒	SEG1		P95/COM5/SEG1/TS26/TI02/TO02/INTP1/SO01	61
☒	SEG2		P96/COM6/SEG2/TS25/INTP5/SI01/SDA01/SDA	60
☒	SEG3		P97/COM7/SEG3/TS24/TI03/TO03/INTP4/SCK01/	59

Figure 5-9 Change pin occupation in Pins page

Hardware Resource

Type filter text

Serial Interface UARTA

UARTA0

UARTA1

UARTA2

UARTA3

LCD Controller/Driver

Logic and Event Link Controller

Interrupt Function

Key Interrupt

On-Chip Debug

Power Supply

Voltage Regulator

Capacitive Sensing Unit

Reset Function

Pin Function

type filter text (* = any string, ? = any character)

All

Enabled	Function	PIOR	Assignment	Pin Number
☐	CAPH		Not assigned	Not assigned
☐	CAPL		Not assigned	Not assigned
☒	COM0		P90/COM0/TS31/TI00/TO00/INTP1	66
☒	COM1		P91/COM1/TS30/INTP2	65
☒	COM2		P92/COM2/TS29/TI01/TO01	64
☐	COM3		Not assigned	Not assigned
☐	COM4		Not assigned	Not assigned
☐	COM5		Not assigned	Not assigned
☐	COM6		Not assigned	Not assigned
☐	COM7		Not assigned	Not assigned
☒	SEG0		P94/COM4/SEG0/TS27/INTP2/SI01/SDA01/TIO0	62
☒	SEG1		P95/COM5/SEG1/TS26/TI02/TO02/INTP1/SO01	61
☒	SEG2		P96/COM6/SEG2/TS25/INTP5/SI01/SDA01/SDA	60
☒	SEG3		P97/COM7/SEG3/TS24/TI03/TO03/INTP4/SCK01/	59

Pin Function

Pin Number

Overview

Board

Clocks

System

Components

Pins

Interrupt

Configuration Problems

Console

error, 0 warnings, 0 others

Description

✓ Pin (1 item)

✗ E05000011: The pin COM3 should be set in Pins page

Figure 5-10 Pin error information

Table 5-3 List of pin occupation (1/2)

Display Waveform Setting	Driving Voltage Generator Method	Number of Time Slices	Current Pin Information	Expect Pin Information
Type A waveform	External resistance division	2 (1/2 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4	COM0, COM1, VL2, VL4
		3 (1/2 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4	COM0, COM1, COM2, VL2, VL4
		3 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4	COM0, COM1, COM2, VL1, VL2, VL4
	Internal voltage boosting method on the VL1 reference	3 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4	COM0, COM1, COM2, VL1, VL2, VL4, CAPH, CAPL
		4 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4	COM0, COM1, COM2, COM3, VL1, VL2, VL4, CAPH, CAPL
		6 (1/3 bias mode)	COM0, COM1, COM2, COM3, COM4, COM5, VL1, VL2, VL4	COM0, COM1, COM2, COM3, COM4, COM5, VL1, VL2, VL4, CAPH, CAPL
		8 (1/3 bias mode)	COM0, COM1, COM2, COM3, COM4, COM5, COM6, COM7, VL1, VL2, VL4	COM0, COM1, COM2, COM3, COM4, COM5, COM6, COM7, VL1, VL2, VL4, CAPH, CAPL
		6 (1/4 bias mode)	COM0, COM1, COM2, COM3, COM4, COM5, VL1, VL2, VL3, VL4	COM0, COM1, COM2, COM3, COM4, COM5, VL1, VL2, VL3, VL4, CAPH, CAPL
		8 (1/4 bias mode)	COM0, COM1, COM2, COM3, COM4, COM5, COM6, COM7, VL1, VL2, VL3, VL4	COM0, COM1, COM2, COM3, COM4, COM5, COM6, COM7, VL1, VL2, VL3, VL4, CAPH, CAPL
	Internal voltage boosting method on the VL2 reference	3 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4	COM0, COM1, COM2, VL1, VL2, VL4, CAPH, CAPL
		4 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4	COM0, COM1, COM2, COM3, VL1, VL2, VL4, CAPH, CAPL
		6 (1/3 bias mode)	COM0, COM1, COM2, COM3, COM4, COM5, VL1, VL2, VL4	COM0, COM1, COM2, COM3, COM4, COM5, VL1, VL2, VL4, CAPH, CAPL
		8 (1/3 bias mode)	COM0, COM1, COM2, COM3, COM4, COM5, COM6, COM7, VL1, VL2, VL4	COM0, COM1, COM2, COM3, COM4, COM5, COM6, COM7, VL1, VL2, VL4, CAPH, CAPL
	Capacitor split method for the VDD reference	3 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4, CAPH, CAPL	COM0, COM1, COM2, VL1, VL2, VL4, CAPH, CAPL
	Capacitor split method for the VL4 reference	3 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4, CAPH, CAPL	COM0, COM1, COM2, VL1, VL2, VL4, CAPH, CAPL

Table 5-4 List of pin occupation (2/2)

Display Waveform Setting	Driving Voltage Generator Method	Number of Time Slices	Current Pin Information	Expect Pin Information
Type B waveform	External resistance division	3 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4	COM0, COM1, COM2, VL1, VL2, VL4
	Internal voltage boosting method on the VL1 reference	3 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4	COM0, COM1, COM2, VL1, VL2, VL4, CAPH, CAPL
		4 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4	COM0, COM1, COM2, COM3, VL1, VL2, VL4, CAPH, CAPL
		6 (1/3 bias mode)	COM0, COM1, COM2, COM3, COM4, COM5, VL1, VL2, VL4	COM0, COM1, COM2, COM3, COM4, COM5, VL1, VL2, VL4, CAPH, CAPL
		8 (1/3 bias mode)	COM0, COM1, COM2, COM3, COM4, COM5, COM6, COM7, VL1, VL2, VL4	COM0, COM1, COM2, COM3, COM4, COM5, COM6, COM7, VL1, VL2, VL4, CAPH, CAPL
		8 (1/4 bias mode)	COM0, COM1, COM2, COM3, COM4, COM5, COM6, COM7, VL1, VL2, VL3, VL4	COM0, COM1, COM2, COM3, COM4, COM5, COM6, COM7, VL1, VL2, VL3, VL4, CAPH, CAPL
	Internal voltage boosting method on the VL2 reference	3 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4	COM0, COM1, COM2, VL1, VL2, VL4, CAPH, CAPL
		4 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4	COM0, COM1, COM2, COM3, VL1, VL2, VL4, CAPH, CAPL
		6 (1/3 bias mode)	COM0, COM1, COM2, COM3, COM4, COM5, VL1, VL2, VL4	COM0, COM1, COM2, COM3, COM4, COM5, VL1, VL2, VL4, CAPH, CAPL
		8 (1/3 bias mode)	COM0, COM1, COM2, COM3, COM4, COM5, COM6, COM7, VL1, VL2, VL4	COM0, COM1, COM2, COM3, COM4, COM5, COM6, COM7, VL1, VL2, VL4, CAPH, CAPL
	Capacitor split method for the VDD reference	3 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4, CAPH, CAPL	COM0, COM1, COM2, VL1, VL2, VL4, CAPH, CAPL
	Capacitor split method for the VL4 reference	3 (1/3 bias mode)	COM0, COM1, COM2, COM3, VL1, VL2, VL4, CAPH, CAPL	COM0, COM1, COM2, VL1, VL2, VL4, CAPH, CAPL

5.2.9 Note on the disappearance of assembler macro definition

The assembler macro definition may disappear after clicking “Generate code” in e² studio. It will be fixed in next Smart Configurator release.

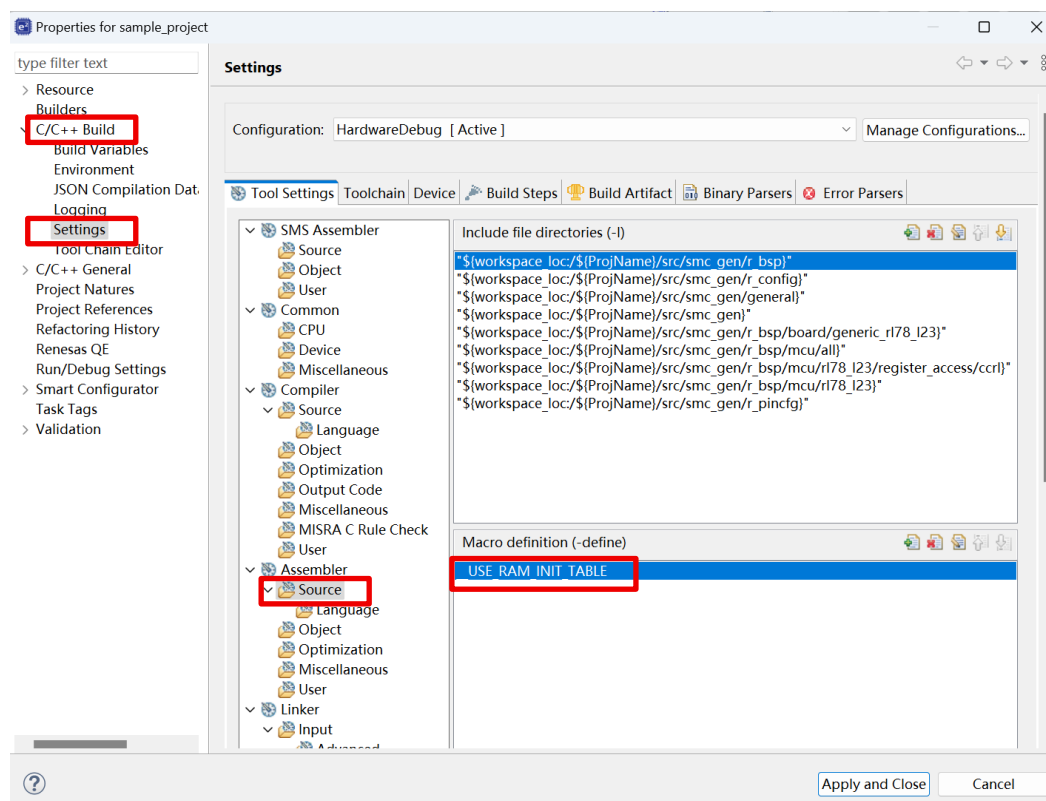


Figure 5-11 Assembler macro definition

[Workaround]

Add assembler macro definition manually. If code generation is executed again, the assembler macro definition may disappear, so be caution.

6. Points for Caution

This section describes points for caution regarding the Smart Configurator for RL78 V1.18.0.

6.1 List of Caution

Table 6-1 List of Caution (1/2)

✓ : Applicable, - : Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
1	Note on the build error message such as "section .bss virtual address range overlaps with .dgc vectortable"	✓	✓	-	✓	✓	-	✓	✓	
2	Note on the installation of the Smart Configurator	✓	✓	✓	✓	✓	✓	✓	✓	
3	Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time	-	✓	-	✓	-	-	✓	✓	
4	Note on pulse width calculation of Timer RD input capture function	-	✓	-	✓	-	-	✓	✓	
5	Note on the include path update issue when renaming the component's configuration name	✓	✓	✓	✓	✓	✓	✓	✓	
6	Note on TAU Input Signal High/Low level Measurement components.	✓	✓	✓	✓	✓	✓	✓	✓	
7	Note on CC-RL V1.12 C++ project	✓	✓	✓	✓	✓	✓	✓	✓	
8	Note on browsing "Release Notes" and "Tool News" URL from the help menu	✓	✓	✓	-	-	-	-	-	
9	Note on using the user code protection feature	✓	✓	✓	✓	✓	✓	✓	✓	
10	Note on IAR build error when using SNOOZE Mode Sequencer (SMS) function	✓	-	-	-	-	-	-	-	
11	Note on A/D conversion time setting after performing [Change device] or [Change resource]	✓	✓	✓	✓	✓	✓	✓	✓	
12	Note on changing Hardware Debug Configuration on project generation wizard	✓	✓	✓	✓	✓	✓	✓	✓	
13	Note on Pin Number maybe wrong in [Pins] page when loading project	-	-	-	-	-	-	✓	-	
14	Note on Pin assignment with PIOR maybe wrong in [Pins] page when changing device	✓	✓	✓	✓	✓	✓	✓	✓	
15	Note on the case that a pin of an unsupported component is assigned when the device is changed	✓	✓	✓	✓	✓	✓	✓	✓	
16	Note on the Pin assignement and pin setting maybe wrong when loading project	-	-	-	-	-	-	-	-	
17	Note on the Developer Assistance can't jump correctly to another HTML file	✓	✓	✓	✓	✓	✓	✓	✓	
18	Note on the clock UI display issue when changing screen scale	✓	✓	✓	✓	✓	✓	✓	✓	

Table 6-2 List of Caution (2/2)

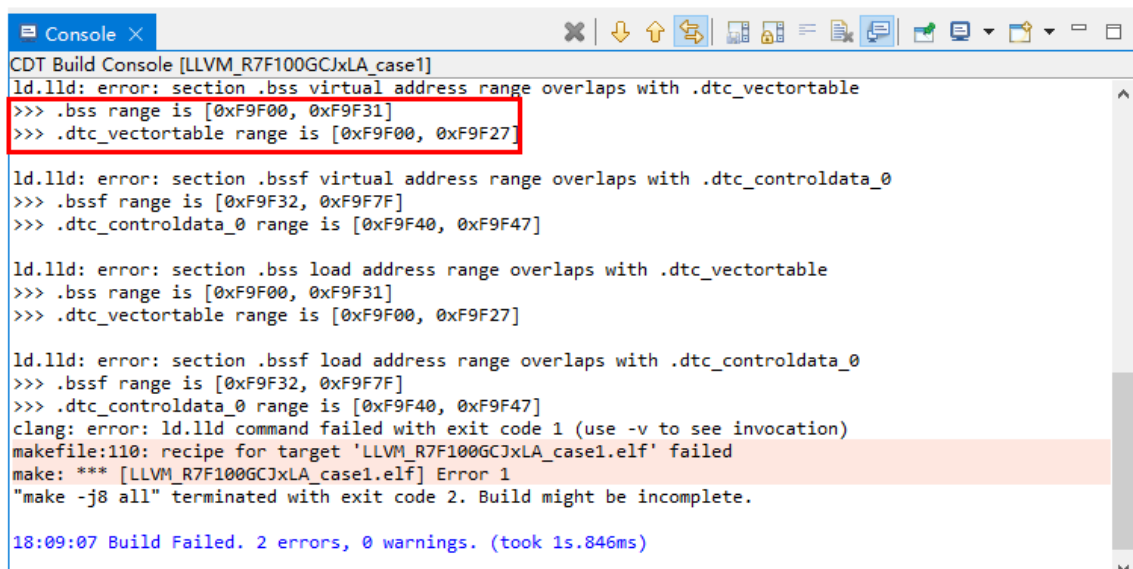
✓ : Applicable, -: Not Applicable

No	Description	RL78/F22	RL78/L23	RL78/G21	Remarks
1	Note on the build error message such as "section .bss virtual address range overlaps with .dtc_vectortable"	✓	✓	-	
2	Note on the installation of the Smart Configurator	✓	✓	✓	
3	Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time	✓	-	-	
4	Note on pulse width calculation of Timer RD input capture function	✓	-	-	
5	Note on the include path update issue when renaming the component's configuration name	✓	✓	✓	
6	Note on TAU Input Signal High/Low level Measurement components.	✓	✓	✓	
7	Note on CC-RL V1.12 C++ project	✓	✓	✓	
8	Note on browsing "Release Notes" and "Tool News" URL from the help menu	-	-	-	
9	Note on using the user code protection feature	✓	✓	✓	
10	Note on IAR build error when using SNOOZE Mode Sequencer (SMS) function	-	-	-	
11	Note on A/D conversion time setting after performing [Change device] or [Change resource]	✓	✓	✓	
12	Note on changing Hardware Debug Configuration on project generation wizard	✓	✓	✓	
13	Note on Pin Number maybe wrong in [Pins] page when loading project	-	-	-	
14	Note on Pin assignment with PIOR maybe wrong in [Pins] page when changing device	✓	✓	✓	
15	Note on the case that a pin of an unsupported component is assigned when the device is changed	✓	✓	✓	
16	Note on the Pin assignement and pin setting maybe wrong when loading project	-	✓	-	
17	Note on the Developer Assistance can't jump correctly to another HTML file	✓	✓	✓	
18	Note on the clock UI display issue when changing screen scale	✓	✓	✓	

6.2 Details of Caution

6.2.1 Note on the build error message such as "section .bss virtual address range overlaps with .dtc_vectortable"

When the user uses many components and DTC component together, the generated code build might fail due to some section address overlaps.



```
CDT Build Console [LLVM_R7F100GCJxLA_case1]
ld.lld: error: section .bss virtual address range overlaps with .dtc_vectortable
>>> .bss range is [0xF9F00, 0xF9F31]
>>> .dtc_vectortable range is [0xF9F00, 0xF9F27]

ld.lld: error: section .bssf virtual address range overlaps with .dtc_controldata_0
>>> .bssf range is [0xF9F32, 0xF9F7F]
>>> .dtc_controldata_0 range is [0xF9F40, 0xF9F47]

ld.lld: error: section .bss load address range overlaps with .dtc_vectortable
>>> .bss range is [0xF9F00, 0xF9F31]
>>> .dtc_vectortable range is [0xF9F00, 0xF9F27]

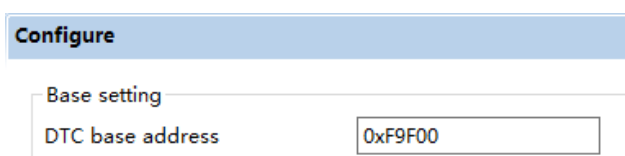
ld.lld: error: section .bssf load address range overlaps with .dtc_controldata_0
>>> .bssf range is [0xF9F32, 0xF9F7F]
>>> .dtc_controldata_0 range is [0xF9F40, 0xF9F47]
clang: error: ld.lld command failed with exit code 1 (use -v to see invocation)
makefile:110: recipe for target 'LLVM_R7F100GCJxLA_case1.elf' failed
make: *** [LLVM_R7F100GCJxLA_case1.elf] Error 1
"make -j8 all" terminated with exit code 2. Build might be incomplete.

18:09:07 Build Failed. 2 errors, 0 warnings. (took 1s.846ms)
```

Figure 6-1 Build error message

[Workaround]

The Smart Configurator cannot set ".bss" and ".bssf" section address. So user should consider to modify ".bss" and ".bssf" section address manually in "linker_script.ld" file or change the DTC base address to avoid such section overlap error.



Configure	
Base setting	
DTC base address	0xF9F00

Figure 6-2 DTC base address setting

6.2.2 Note on the installation of the Smart Configurator

Do not set more than 64 characters for the installation directory.

The user might see an error message "The specified path is too long" and will not be able to install Smart Configurator.

6.2.3 Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time

If the user sets up TRDIOA0 for Input capture and TRDIOB0 for Output compare at the same time. Smart Configurator will output a Peripheral conflict error.

The user can ignore this Smart Configurator error message and use these two functions at the same time.

6.2.4 Note on pulse width calculation of Timer RD input capture function

The pulse width calculation code is with the assumption that the counter is not cleared between two interrupts occurrence, except the input pulse width which is selected as counter clear trigger on GUI.

For example, when "Clear by TRDGRA_n input capture" is selected, only TRDIOA_n pulse width calculation handle counter clear, other input pulse width calculation doesn't handle counter clear.



Figure 6-3 Counter clear setting in Input capture function

6.2.5 Note on the include path update issue when renaming the component's configuration name

When renaming the added component's configuration in e² studio Smart Configurator project that has self-defined include path setting for any folder or file, include path setting for that folder or file will keep the old name setting after code generation. This will cause build error when compiling the newly generated codes so please manually update the include path.

The folder or file which has self-defined include path setting can be recognized by checking the overlay icon (📁) on that folder or file. Below is an example on how to handle the include path update after renaming Compare Match Timer component configuration.

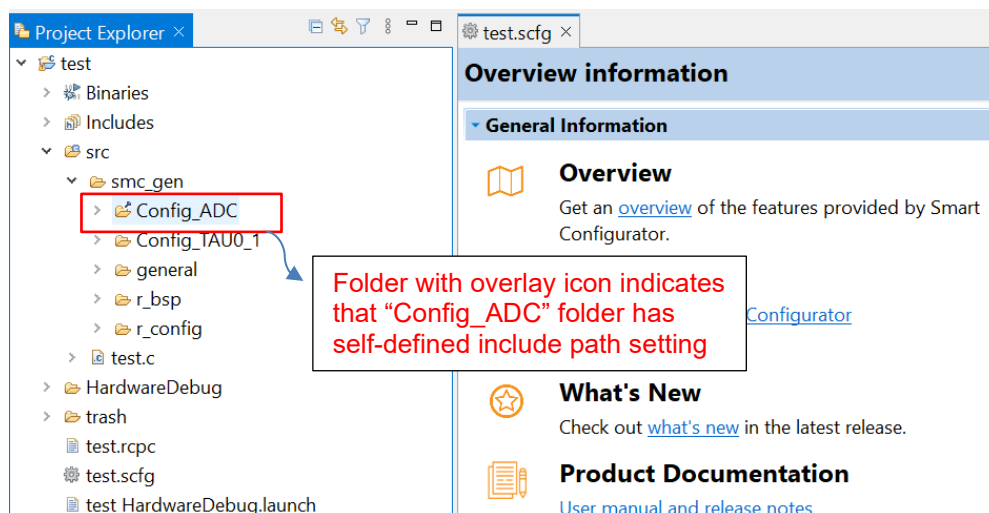


Figure 6-4 Interval Timer component configuration before renaming

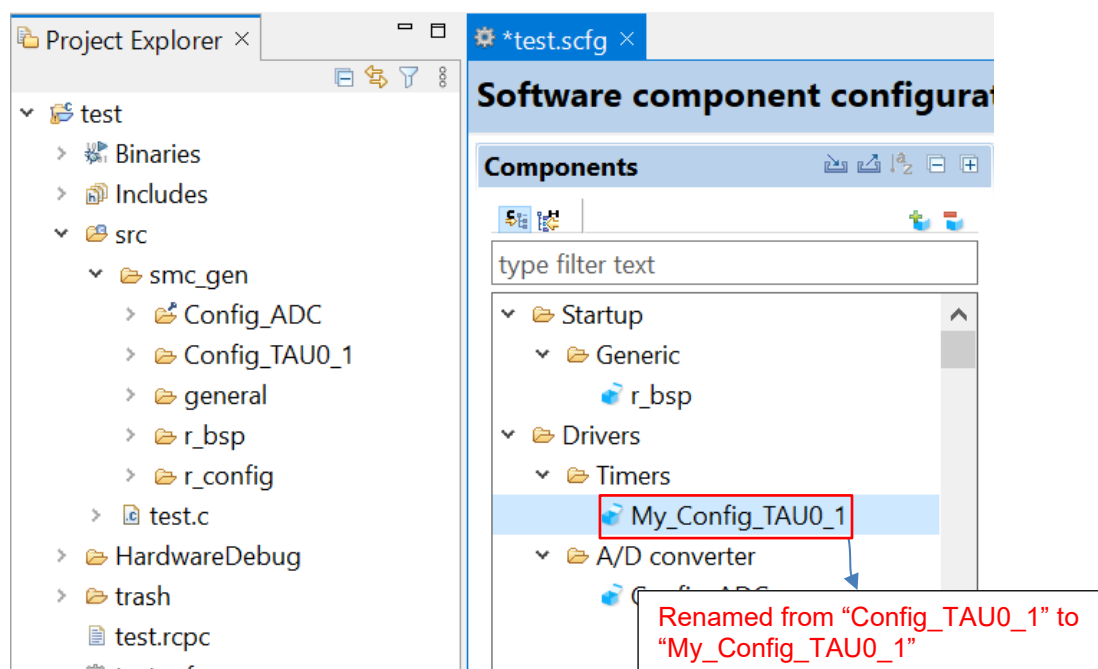


Figure 6-5 The Interval Timer component configuration after renaming

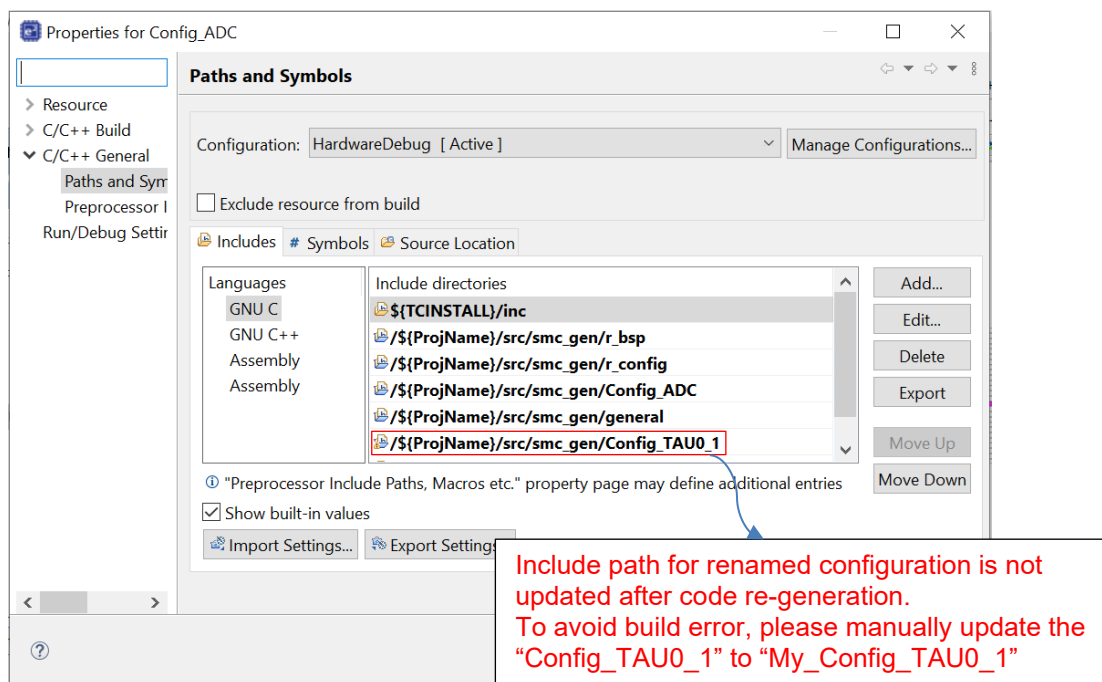


Figure 6-6 Include path setting for the “Config_ADC” configuration

6.2.6 Note on TAU Input Signal High/Low level Measurement component

When using TAU Input Signal High/Low level Measurement component, after used noise filter function for TImn input pulse, please make sure the High/Low level width min value needs to be greater than two times the minimum value prompted on the UI.

For example, the High/Low level width min value is 0.032us (min value), when use noise filter function, the width min value should be 0.064us.



Figure 6-7 High/Low level width min value

6.2.7 Note on CC-RL V1.12 C++ project

In CC-RL V1.12 or later C++ project, there are some dummy issues such as "EI()" in editor. However this is editor specification and does not affect the program operation. Please ignore it.

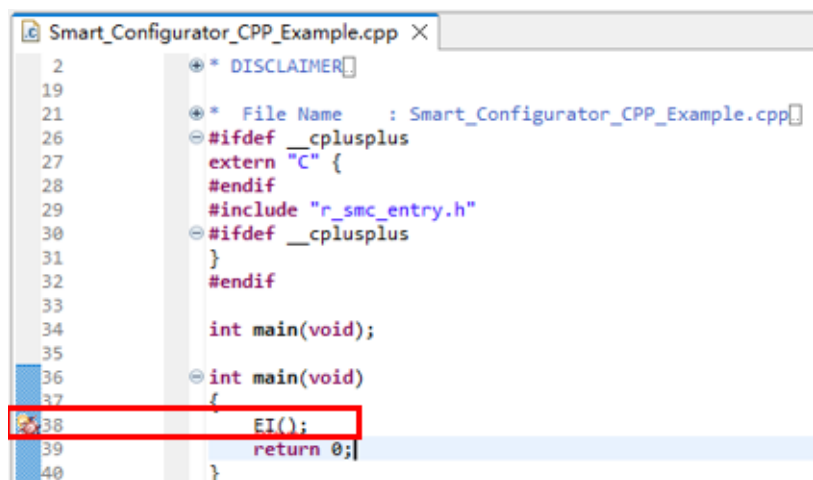


Figure 6-8 CODAN issue in CC-RL V1.12 C++ project

6.2.8 Note on browsing "Release Notes" and "Tool News" URL from the help menu

For Smart Configurator for RL78 V1.15.0 or before version, "Release Notes" and "Tools News" in the help menu cannot access the correct URL. Please access the URL below directly for Smart Configurator for RL78 V1.15.0 or before version.

Release Notes:

<https://www.renesas.com/en/software-tool/rl78-smart-configurator?documents-type-filter=release-note#documents>

Tool News:

<https://www.renesas.com/en/software-tool/rl78-smart-configurator?documents-type-filter=tool-news-note#documents>

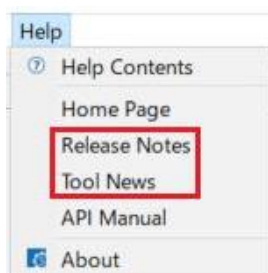


Figure 6-9 Release Notes and Tool News in Smart Configurators

6.2.9 Note on using the user code protection feature

From Smart Configurator for RL78 V1.5.0 onwards, the user code protection feature will be supported for all Code Generation components. Please use the following specific tags to add user code when using the user code protection feature. If the specific tags do not match exactly, inserted user code will not be protected after the code generation.

/* Start user code */

User code can be added between the specific tags

/* End user code */

6.2.10 Note on IAR build error when using SNOOZE Mode Sequencer (SMS) component

When using SNOOZE Mode Sequencer (SMS) component, if the following build error is met in IAR Embedded workbench, please check the build order setting in project [Options...] -> [Custom Build] page.

- 1) When using IAR Embedded workbench V5.10 or later, select "Run before compiling/assembling" (refer to Figure 6-11)
- 2) When using IAR Embedded workbench V4.21, make "Run this tool before all other tools" checked (refer to Figure 6-12)

The above setting can eliminate this build error.



Figure 6-10 IAR build error

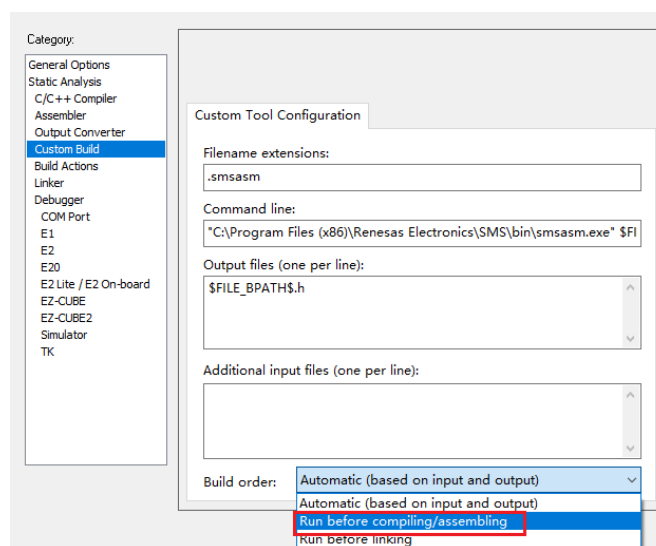


Figure 6-11 "Build order" setting of IAR Embedded workbench V5.10 or later

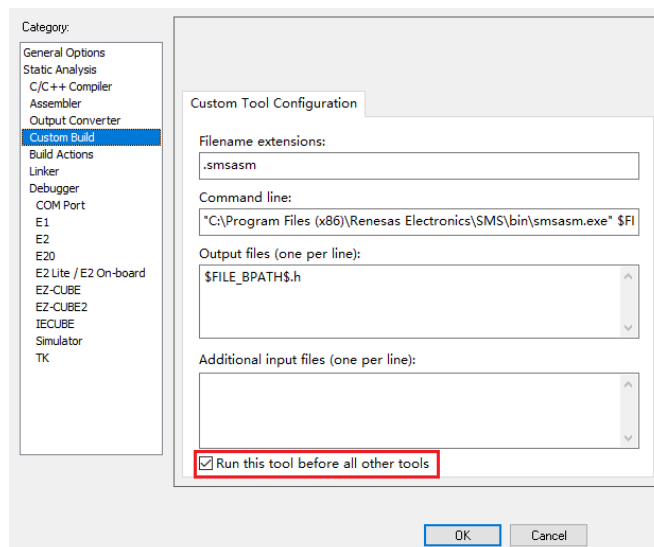


Figure 6-12 Custom build setting of IAR Embedded workbench V4.21

6.2.11 Note on A/D conversion time setting after performing [Change device] or [Change resource]

After performing [Change device] (for example, change from RL78/G23 to RL78/G24), the A/D conversion time setting can't be kept. The user should take note to reconfirm the conversion time setting as he wants.

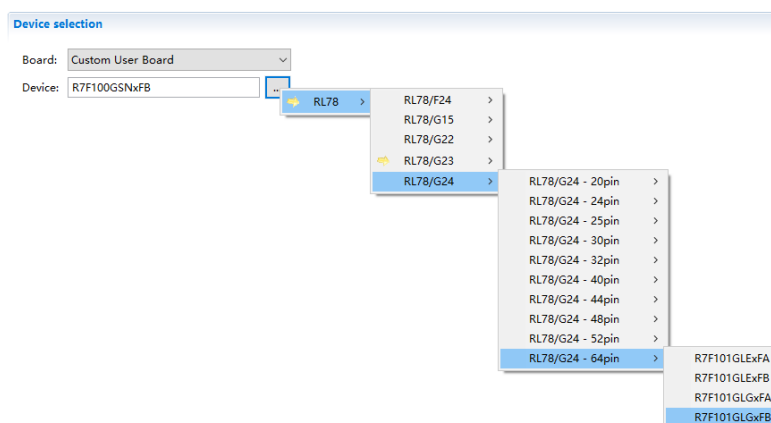


Figure 6-13 [Change device] operation

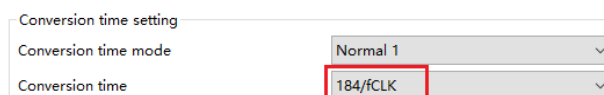


Figure 6-14 A/D conversion time setting

When changing resource, for example from RL78/G24 normal A/D and RL78/G24 advanced A/D, the A/D conversion time can't be kept.

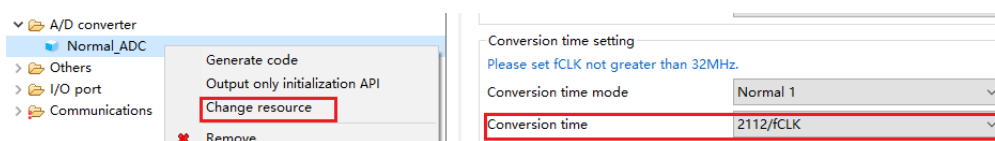


Figure 6-15 [Change resource] operation

6.2.12 Note on changing Hardware Debug Configuration on project generation wizard

When a target board (except custom) is selected during creating a new project, please don't change the Hardware Debug Configuration manually. The reason is that the Hardware Debug Configuration has been decided by target board automatically. The user setting can't be reflected into Smart Configurator.

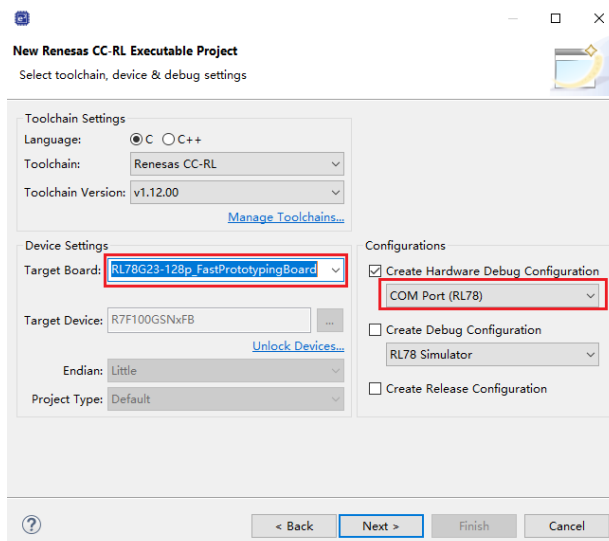


Figure 6-16 Select a target board when creating a project in e² studio

6.2.13 Note on Pin Number maybe wrong in [Pins] page when loading project

The Pin Number maybe wrong for SCL00, SDA00, SI00, SO00, SCK00 when the user loads a 48/52/64pin project. The user needs to re-assign these pins manually.

Pin Function							
type filter text (* = any string, ? = any character)							
Ena...	Function	PIOR	Assignment	Pin Number	Direct...	Remarks	Comments
☒	RxD0	PIOR06, ...	P16/ANI26/CCD00/TI01/TO01/I	16	I	There is no software ...	
☐	SCK00	PIOR01	Not assigned	Not assigned	None		
☐	SCL00	PIOR01	Not assigned	Not assigned	None		
☐	SDA00	PIOR01	Not assigned	Not assigned	None		
☐	SI00	PIOR01	Not assigned	Not assigned	None		
☒	SO00	PIOR01	Not assigned	-	O	There is no software ...	
☐	TxD0	PIOR06, ...	Not assigned	Not assigned	None		
☐	_SSI00		Not assigned	Not assigned	None		

Figure 6-17 Pin Number maybe wrong in [Pins] page

6.2.14 Note on Pin assignment with PIOR maybe wrong in [Pins] page when changing device

After performing [Change device] (for example, change from RL78/G23 to RL78/F24), the Pin assignment with PIOR may change according to PIOR setting automatically. When it has pin conflict, Smart Configurator will output pin conflict message and doesn't change pin assignment automatically. The user needs to re-assign these pins manually.

Pin Function					
type filter text (* = any string, ? = any character)					
Enabled	Function	PIOR	Assignment	Pin Number	Direction
☒	RxD2	PIOR1	Not assigned	Not assigned	None
☐	RxDA0		Not assigned	Not assigned	None
☐	SCK00	PIOR1	Not assigned	Not assigned	None
☐	SCK01		Not assigned	Not assigned	None

Figure 6-18 Pin assignment with PIOR maybe wrong in [Pins] page

6.2.15 Note on the case that a pin of an unsupported component is assigned when the device is changed

After performing [Change device] (for example, change from RL78/L23 to RL78/G15), the Pin assignment may keep “Enabled” though the component doesn’t exist. When the pin is enabled and exists in changed device, Smart Configurator doesn’t change pin assignment automatically. The user needs re-assign these pins manually.

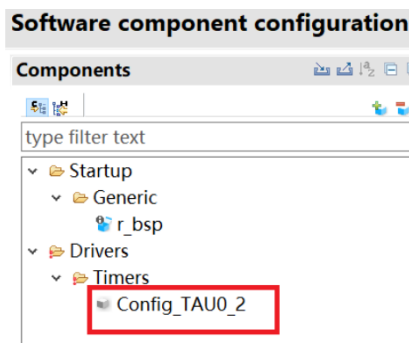


Figure 6-19 The component doesn’t exist after changing device

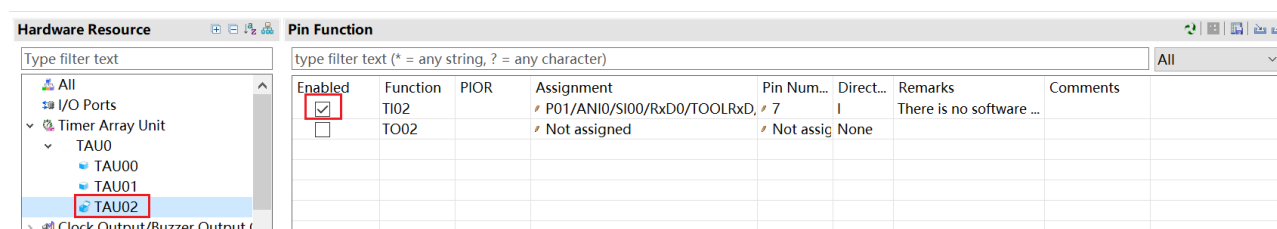


Figure 6-20 Pin assignment keeps “Enabled” in [Pins] page after changing device

6.2.16 Note on the Pin assignment and pin setting maybe wrong when loading project

From Smart Configurator for RL78 V1.14.0, Smart Configurator supports RL78/L23 100 pin LQFP package for R7F100LPGxFA, R7F100LPJxFA and R7F100LPLxFA. If the user loads a project which is created by R7F100LPGxFA, R7F100LPJxFA and R7F100LPLxFA in Smart Configurator for RL78 V1.13.0, the Pin assignment and pin setting maybe wrong. The following is an example.

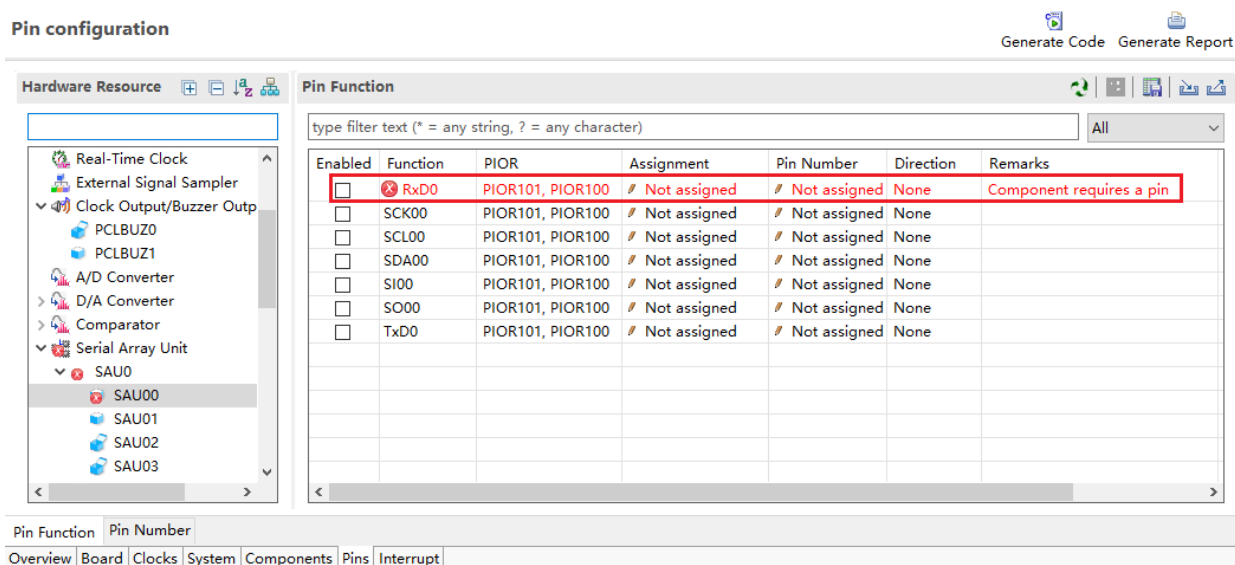


Figure 6-21 RxD0 isn’t assigned in [Pins] page

```

void R_UART0_Create(void)
{
    ...
    SOL0 |= _0001_SAU_CHANNEL0_INVERTED; /* output level reverse */
    SOE0 |= _0001_SAU_CH0_OUTPUT_ENABLE; /* enable UART0 output */
    PFOE1 &= 0xFFE0; /* only used for input to ELCL, not for Tx0 pin */
    R_UART0_Create_UserInit();
}

```

Figure 6-22 Rx0 pin setting isn't generated in Create()

[Workaround]

The user performs [Change device] (select same chip). And then the user should check and re-assign all the pins in [Pins] page manually. When the user generates code again, the pin setting will generate correctly.

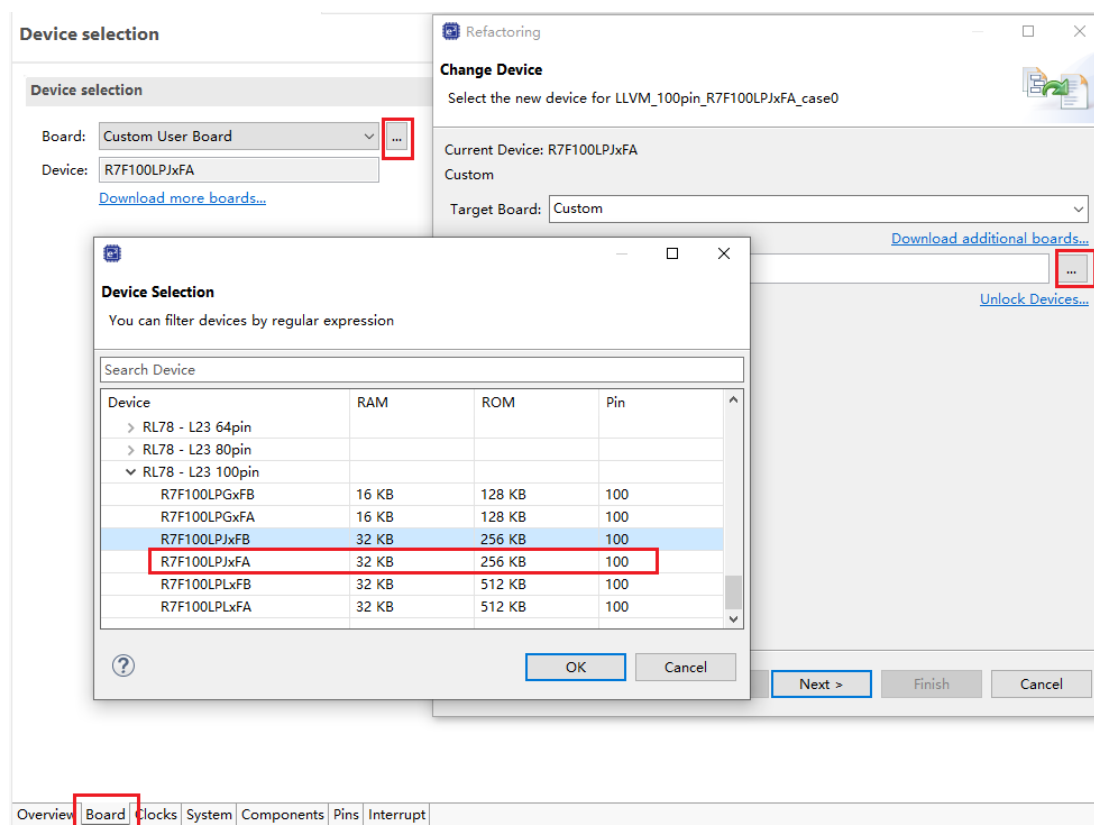


Figure 6-23 Change device in [Board] page

6.2.17 Note on the Developer Assistance can't jump correctly to another HTML file

When the user clicks the link in Developer Assistance, it can't jump correctly to another HTML file and will show "File not found".

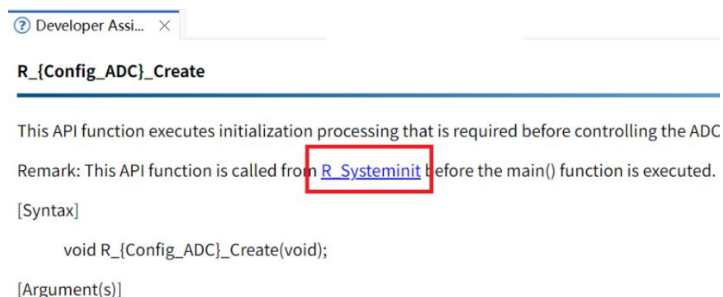


Figure 6-24 Can't jump correctly when clicking the link to another HTML file

[Workaround] Please click “Developer assistance” node in project tree and select the API function in Developer Assist Browser to check API guide information.

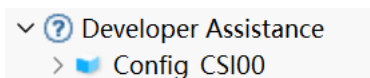


Figure 6-25 “Developer assistance” node

6.2.18 Note on the clock UI display issue when changing screen scale

The clock UI display incorrectly after changing the screen scale.

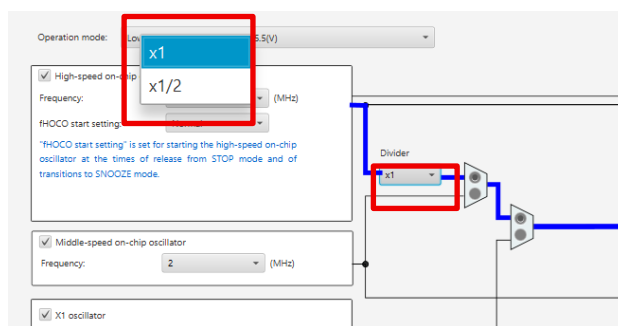


Figure 6-26 UI display incorrectly when clicking

[Workaround]

Uncheck “Use monitor-specific UI scaling” in Preferences -> General -> Appearance in e² studio.

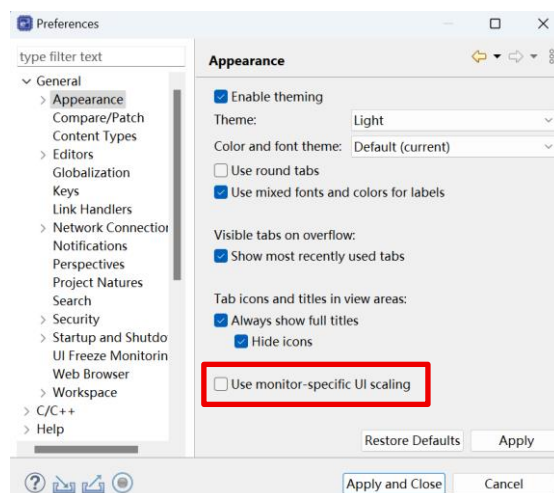


Figure 6-27 Uncheck “Use monitor-specific UI scaling”

Revision History

Rev.	Section	Description
1.00	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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