RZ/T2L Group

SPI Interface Usage Sample Program for HIPERFACE DSL Safety

Summary

This document describes the SPI interface usage sample program for the RZ/T2L Encoder I/F HIPERFACE DSL® Safety package.

For HIPERFACE DSL® communication protocol specifications and encoder specifications, contact SICK AG.

Functionality Checked Device

RSK+RZT2L Board (RTK9RZT2L0C00000BJ)

Contents

HIPERFACE DSL is a registered trademark of SICK AG.

1. Package Contents

This package is a sample program for your information and reference to use HIPERFACE DSL Safety SPI interface. The function to access SPI interface is added to the base program package - RZ/T2L group HIPERFACE DSL Safety release package (r11an0761xx0200-rzt2l-hfdsl-safety.zip). For the driver specification and detail of the functions, refer application note (r11an0760ej0200-rzt2l-hfdsl-safety.pdf) included in the based sample program package.

For checking operation, this package uses SPI module of the same RZ/T2L device as the SPI master. The SPI master access to the HIPERFACE DSL SPI interface. SPI master of the other devise can be used in the same way.

This package contains the following contents.

1.1 Software

- Source Code

No.	Name	Version number
1	RZ/T2L HIPERFACE DSL Safety SPI Interface Usage Sample Program	2.0

1.2 Document

No.	Document name	Version	File name
1	RZ/T2L Group SPI Interface Usage Sample Program for HIPERFACE DSL Safety Release Note	2.00	(j) r11an0983jj0200-rzt2l.pdf (e) r11an0983ej0200-rzt2l.pdf (this document)

2. File Structure

The file structure and contents of this package are detailed below.

```
  Top
  ├── r11an0983jj0200-rzt2l.pdf
  ├── r11an0983ej0200-rzt2l.pdf
  └── workspace
        └── Software
              ├── iccarm
              │     └── RZ_T2L_hfdsl.zip : RZ/T2L HIPERFACE DSL Safety
              │                            SPI interface usage sample program set (IAR)
              └── gcc
                    └── RZ_T2L_hfdsl.zip : RZ/T2L HIPERFACE DSL Safety
                                           SPI interface usage sample program set (e2 studio)
```

The file structure of the RZ_T2L_hfdsl.zip is shown below.

```
  Top folder
  ├── configuration.xml                  : FSP Configuration Data
  ├── ( Environment File Depending on Build Tool )
  └── src
        ├── hal_entry.c                  : HIPERFACE DSL Safety sample program
        ├── hfdsl_main.c                 : HIPERFACE DSL Safety sample program
        ├── siochar.c                    : SCI_UART sample program
        ├── siorw.c                      : SCI_UART sample program
        ├── sio_char.h                   : SCI_UART sample program
        └── drv
              └── hfdsl
                    ├── iodefine_hfdsl.h     : HFDSL register definition file
                    ├── r_hfdsl_rzt2.c       : HFDSL driver file
                    ├── r_hfdsl_rzt2_config.h : HFDSL driver file
                    ├── r_hfdsl_rzt2_dat.h   : HFDSL driver file
                    └── r_hfdsl_rzt2_if.h    : HFDSL driver file
```

3. About SPI Interface Usage Sample Program

This section contains information necessary to use the SPI interface usage sample program for HIPERFACE DSL Safety.

3.1 Software Information

3.1.1 Base OS

This sample program is OS-independent.

3.1.2 Memory Size

Memory size used by this sample program and HFDSL driver is shown in the following table. This table does not include the memory size used by Flexible Software Package or C language libraries of the compiler.

Items		Memory Size	
		EWARM [kBytes]	e^2 studio [kBytes]
HFDSL driver	Code	3.5	2.6
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.1	0.1
	Constant Data	0.1	0.1
Sample program	Code	2.9	3.3
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.4	0.4
	Constant Data	1.1	1.1

3.2 Hardware Information

3.2.1 Device

RZ/T2L

3.2.2 Target Board

(1) Board Name

RSK+RZT2L (RTK9RZT2L0C00000BJ)

(2) Setting of the Target Board

The target board configuration is as follows.

SW4-1: ON, SW4-2: ON, SW4-3: OFF

SW4-4: OFF

SW4-5: ON

SW4-6: ON

SW4-7: OFF

SW5-1: OFF, SW5-2: ON, SW5-3: OFF, SW5-4: OFF, SW5-5: OFF

SW6-1: OFF, SW6-2: ON, SW6-3: OFF, SW6-4: OFF

SW6-5: OFF, SW6-6: ON, SW6-7: OFF, SW6-8: OFF

SW8-7: OFF

SW8-8: OFF

SW8-9: OFF

SW8-10: OFF

CN17: Short between 1-2 pins (Set VCC1833_2 to 3.3V)

CN32: Short between 1-2 pins (Set VCC1833_3 to 3.3V)

(3) Used Pins of the Target Board

The correspondence between the pin used as the encoder I/F and the pin header of the target board is as follows.

Channel	Port Name	I/O Port	Pin Header	Input/ Output	Description
HFDSL0	ENCIFDI0 (dsl_in0)	P02_2	J26 #2	Input	Data input
	ENCIFDO0 (dsl_out0)	P02_3	J26 #1	Output	Data output
	ENCIFOE0 (dsl_en0)	P01_7	J26 #4	Output	Drive/receive control
	HDSL0_CLK1	P18_6	JA6 #16	Input	HFDSL0 SPI clock safe ch1
	HDSL0_SEL1	P00_0	JA6 #10	Input	HFDSL0 SPI selection safe ch1
	HDSL0_MISO1	P02_1	JA3-A #38	Output	HFDSL0 SPI data output safe ch1
	HDSL0_MOSI1	P06_0	JA3-A #13	Input	HFDSL0 SPI data input safe ch1
	HDSL0_CLK2	P06_1	JA3-A #11	Input	HFDSL0 SPI clock safe ch2
	HDSL0_SEL2	P06_4	JA3-A #8	Input	HFDSL0 SPI selection safe ch2
	HDSL0_MISO2	P06_5	JA3-A #7	Output	HFDSL0 SPI data output safe ch2
	HDSL0_MOSI2	P00_2	JA3-A #25	Input	HFDSL0 SPI data input safe ch2
HFDSL1	ENCIFDI1 (dsl_in1)	P10_1	CN1 #5	Input	Data input
	ENCIFDO1 (dsl_out1)	P10_0	CN1 #4	Output	Data output
	ENCIFOE1 (dsl_en1)	P09_7	CN1 #3	Output	Drive/receive control
	HDSL1_CLK1	P07_1	CN1 #8	Input	HFDSL1 SPI clock safe ch1
	HDSL1_SEL1	P07_2	CN1 #12	Input	HFDSL1 SPI selection safe ch1
	HDSL1_MISO1	P07_3	CN1 #13	Output	HFDSL1 SPI data output safe ch1
	HDSL1_MOSI1	P08_4	CN1 #14	Input	HFDSL1 SPI data input safe ch1
	HDSL1_CLK2	P17_4	CN1 #16	Input	HFDSL1 SPI clock safe ch2
	HDSL1_SEL2	P09_3	CN1 #17	Input	HFDSL1 SPI selection safe ch2
	HDSL1_MISO2	P09_4	CN1 #18	Output	HFDSL1 SPI data output safe ch2
	HDSL1_MOSI2	P09_5	CN1 #19	Input	HFDSL1 SPI data input safe ch2
SPI1	SPI_RSPCK1	P01_5	JA3-A #48	Output	Clock output
	SPI_SSL10	P15_1	JA3-A #49	Output	Slave selection signal output
	SPI_MISO1	P14_7	JA3-A #43	Input	Slave transmission data input
	SPI_MOSI1	P15_0	JA3-A #46	Output	Master transmission data output
SPI2	SPI_RSPCK2	P18_4	CN27 #11	Output	Clock output
	SPI_SSL20	P21_1	J27 #1	Output	Slave selection signal output
	SPI_MISO2	P21_2	J27 #2	Input	Slave transmission data input
	SPI_MOSI2	P18_5	CN27 #12	Output	Master transmission data output

(4) Pin Connection on the Target Board

The SPI channel access of the HIPERFACE DSL Safety is operated via the SPI interface assigned to the I/O ports by this sample program. Please connect between the RZ/T2L SPI master module pins and the corresponding HIPERFACE DSL SPI interface pins on the target board according to the HFDSL channel.

Connections according to the using channel are as follows.

Channel	HIPERFACE DSL SPI interface		SPI master to connect to	
	Port Name	Pin Header	Pin Header	Port Name
Case of HFDSL0 to use	HDSL0_CLK1	JA6 #16	JA3-A #48	SPI_RSPCK1
	HDSL0_SEL1	JA6 #10	JA3-A #49	SPI_SSL10
	HDSL0_MISO1	JA3-A #38	JA3-A #43	SPI_MISO1
	HDSL0_MOSI1	JA3-A #13	JA3-A #46	SPI_MOSI1
	HDSL0_CLK2	JA3-A #11	CN27 #11	SPI_RSPCK2
	HDSL0_SEL2	JA3-A #8	J27 #1	SPI_SSL20
	HDSL0_MISO2	JA3-A #7	J27 #2	SPI_MISO2
	HDSL0_MOSI2	JA3-A #25	CN27 #12	SPI_MOSI2
Case of HFDSL1 to use	HDSL1_CLK1	CN1 #8	JA3-A #48	SPI_RSPCK1
	HDSL1_SEL1	CN1 #12	JA3-A #49	SPI_SSL10
	HDSL1_MISO1	CN1 #13	JA3-A #43	SPI_MISO1
	HDSL1_MOSI1	CN1 #14	JA3-A #46	SPI_MOSI1
	HDSL1_CLK2	CN1 #16	CN27 #11	SPI_RSPCK2
	HDSL1_SEL2	CN1 #17	J27 #1	SPI_SSL20
	HDSL1_MISO2	CN1 #18	J27 #2	SPI_MISO2
	HDSL1_MOSI2	CN1 #19	CN27 #12	SPI_MOSI2

3.3 Procedures on Development Environments

3.3.1 Preparation before Executing the Sample Program

This sample program communicates with a PC. The USB connection terminal on the target board is CN16.

The terminal software of the host PC is set as shown in the following table.

Function	Setting
Communication method	Asynchronous serial transmission/reception
Sending / receiving order	LSB first
Transfer rate	19200 bps
Character length	8 bits
Stop bit length	1 bit
Parity function	None
Hardware flow control	None

3.3.2 EWARM from IAR Systems

(1) Build Environment

Operation is checked with the following tools.

IAR Embedded Workbench for Arm (EWARM) Version 9.50.1

RENESAS FSP Smart Configurator (FSP SC) 2024-01.1

RENESAS Flexible Software Package (FSP) for RZ/T2 v2.0.0

(2) Execution Environment ICE

IAR I-jet

(3) Build Procedure for Sample Programs

The build procedure for the sample program is as follows.

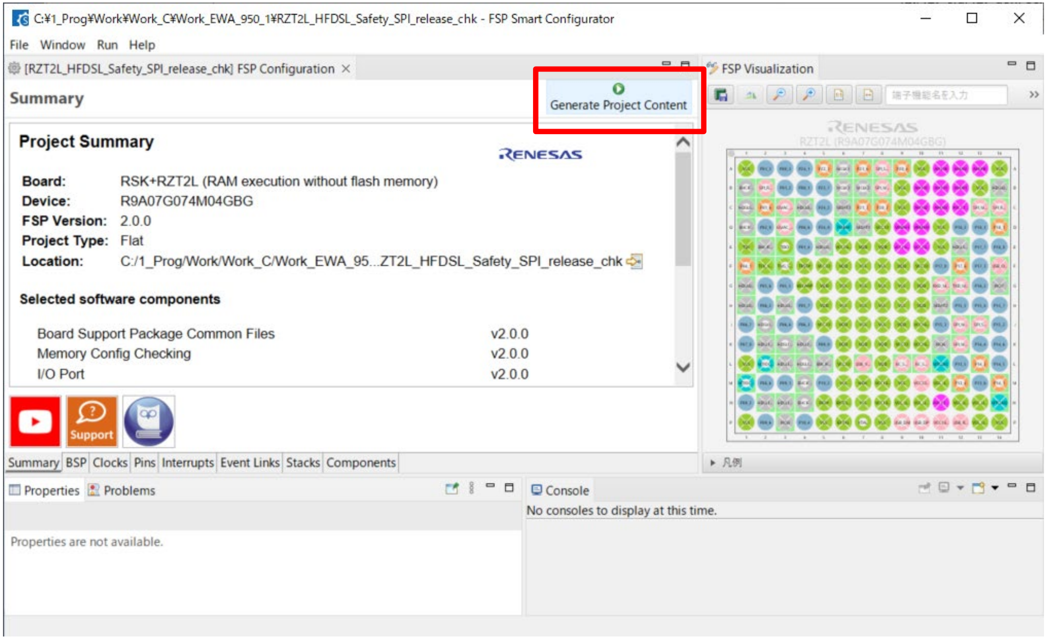
1 Copy the extracted source files to the desired location.
2 Activate EWARM.
3 Select [File] menu -> [Open Workspace].
4 Open the extracted source file RZ_T2L_hfdsl.eww.
5 Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE. *

Note: The following procedure adds the activation of the FSP Smart Configurator to the [Tools] menu of the EWARM IDE. Select [Tools] menu -> [Tool Configuration] in the EWARM IDE. Select the [New] button, specify a table string in each field, and press [OK].

Field	String
Menu text	FSP Smart Configurator
Command	$RASC_EXE_PATH$
Argument	--compiler IAR configuration.xml
Initial directory	$PROJ_DIR$

String for the command is variable holding the path of the Smart Configurator execution file, rasc.exe. You can also start the FSP Smart Configurator directly from the command prompt by specifying the folder where it is installed.

6 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rzt, rzt_cfg, rzt_gen, script and .setting folders will be generated.



C:¥1_Prog¥Work¥Work_C¥Work_EWA_950_1¥RZT2L_HFDSL_Safety_SPI_release_chk - FSP Smart Configurator

[RZT2L_HFDSL_Safety_SPI_release_chk] FSP Configuration

Summary

Project Summary

Board: RSK+RZT2L (RAM execution without flash memory)
Device: R9A07G074M04GBG
FSP Version: 2.0.0
Project Type: Flat
Location: C:/1_Prog/Work/Work_C/Work_EWA_95...ZT2L_HFDSL_Safety_SPI_release_chk

Selected software components

Board Support Package Common Files	v2.0.0
Memory Config Checking	v2.0.0
I/O Port	v2.0.0

Properties are not available.

No consoles to display at this time.

7 When project generation is complete, close the Smart Configurator.

8 Select [Rebuild All] from the [Project] menu of EWARM.
The file Debug\Exe\RZ_T2L_hfdsl.out is generated.

(4) Sample Program Execution Procedure

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

1 Select [Project] menu -> [Download and Debug].

2 Select [Debug] menu -> [Execute].

(5) Execution Result of the Sample Program

Please refer “3.4.2, Execution Examples of the Sample Program” for the execution results.

3.3.3 e^2 studio from RENESAS

(1) Build Environment

Operation is checked with the following tools.

RENESAS e^2 studio 2024-01.1

Toolchain version: GNU ARM Embedded 12.2.1.arm-12-24

RENESAS Flexible Software Package (FSP) for RZ/T2 v2.0.0

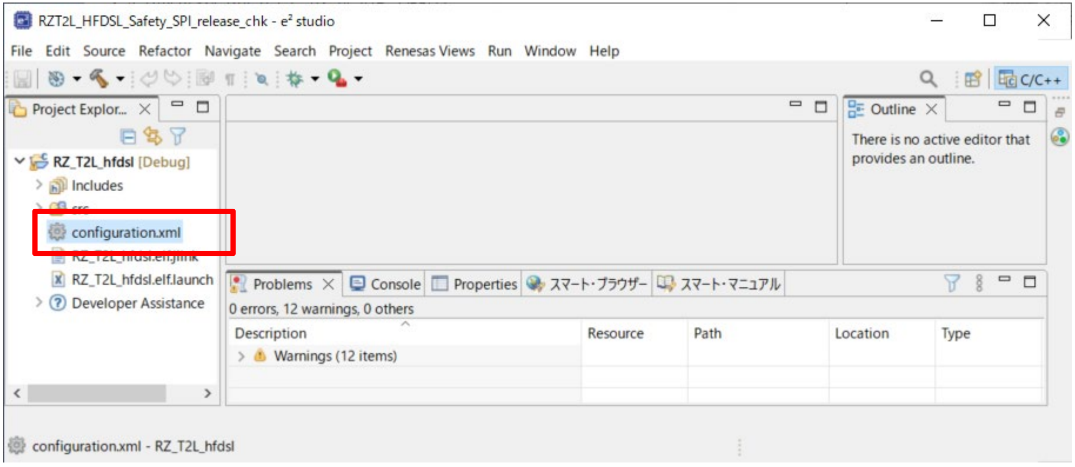
(2) Execution Environment ICE

SEGGER J-Link v7.94h

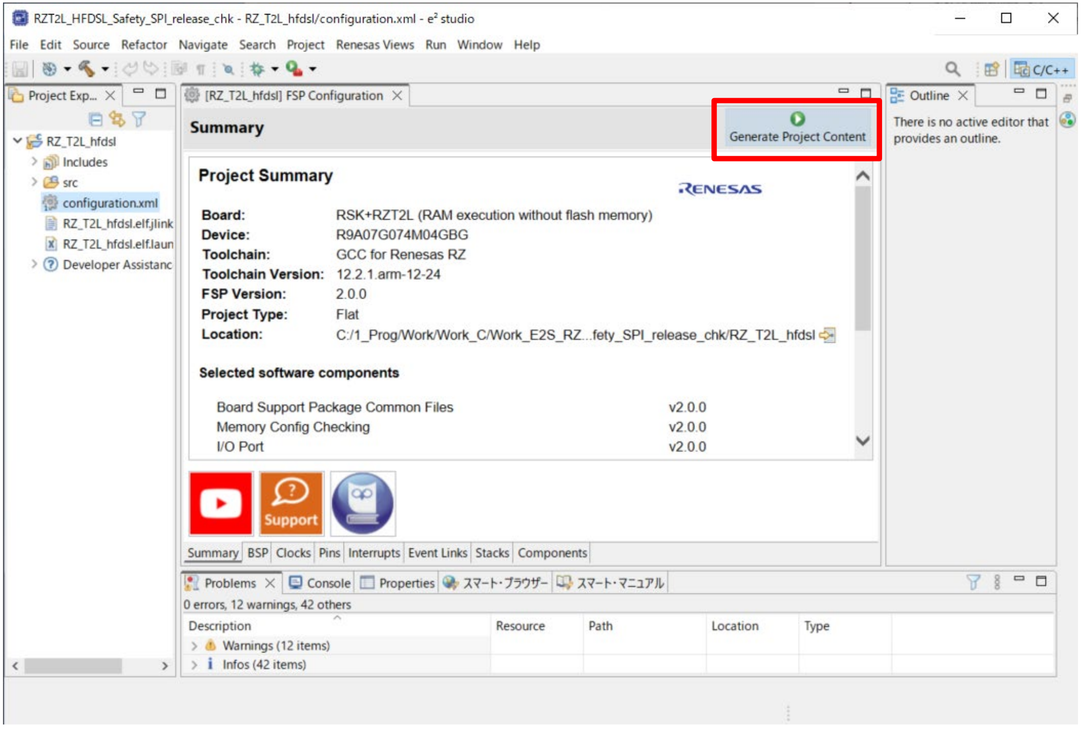
(3) Build Procedure of the Sample Program

The procedure for building the sample program is as follows.

1 Copy the expanded source file to any location.
2 After launching e^2 studio and moving to the workspace, click the [File] menu-> [Import] and select Existing project to workspace and click [Next].
3 On the project import screen, select the folder where the sample program was expanded as the root directory.
4 Select a project, check Copy Project to Workspace, and click [Finish].
5 Double-click the configuration.xml in the Project Explorer pane of e^2 studio to open it.



6 Click Generate Project Content in the FSP Configuration pane of e^2 studio.
The rzt, rzt_cfg, rzt_gen, script, .settings folders are generated.


Project Summary

Board: RSK+RZT2L (RAM execution without flash memory)
Device: R9A07G074M04GBG
Toolchain: GCC for Renesas RZ
Toolchain Version: 12.2.1.arm-12-24
FSP Version: 2.0.0
Project Type: Flat
Location: C:/1_Prog/Work/Work_C/Work_E2S_RZ...fety_SPI_release_chk/RZ_T2L_hfdsl

Selected software components

Board Support Package Common Files	v2.0.0
Memory Config Checking	v2.0.0
I/O Port	v2.0.0

RZT2L_HFDSL_Safety_SPI_release_chk - RZ_T2L_hfdsl/configuration.xml - e² studio
File Edit Source Refactor Navigate Search Project Renesas Views Run Window Help
C/C++
Project Exp...
RZ_T2L_hfdsl
Includes
src
configuration.xml
RZ_T2L_hfdsl.elf.jlink
RZ_T2L_hfdsl.elf.laun
Developer Assistanc
[RZ_T2L_hfdsl] FSP Configuration
Summary
Generate Project Content
RENESAS
Support
Summary BSP Clocks Pins Interrupts Event Links Stacks Components
Outline
There is no active editor that provides an outline.
Problems
Console
Properties
スマート・ブラウザー
スマート・マニュアル
0 errors, 12 warnings, 42 others
Description
Resource
Path
Location
Type
Warnings (12 items)
Infos (42 items)

7 Select [Project] menu -> [Build All].
The Debug\RZ_T2L_hfdsl.elf file is generated.

(4) Execution Procedure of the Sample Program

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

1 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging].
2 Click [Debug] to start downloading to internal RAM.
3 Click [Run] menu -> [Resume] to run the sample program.

(5) Execution Result of the Sample Program

Please refer “3.4.2, Execution Examples of the Sample Program” for the execution results.

3.4 Description of the Sample Program

3.4.1 Modification Summary of the SPI Interface Usage Sample Program

There is no modification on the HFDSL driver and only SPI interface related operation is added in this SPI interface usage sample program from the HIPERFACE DSL Safety sample program.

In the FSP configuration data (configuration.xml), the result of adding SPI driver (green-shaded) with its initial setting and I/O port assignment is reflected. Additionally, SPI interfaces of the HIPERFACE DSL Safety are assigned to the I/O ports shown in “3.2.2(3), Used Pins of the Target Board”.

Indication of the safe position and the raw data acquired by the SPI interfaces, are implemented by adding SPI driver control part to the sample program and modifying results indication part (red-shaded).

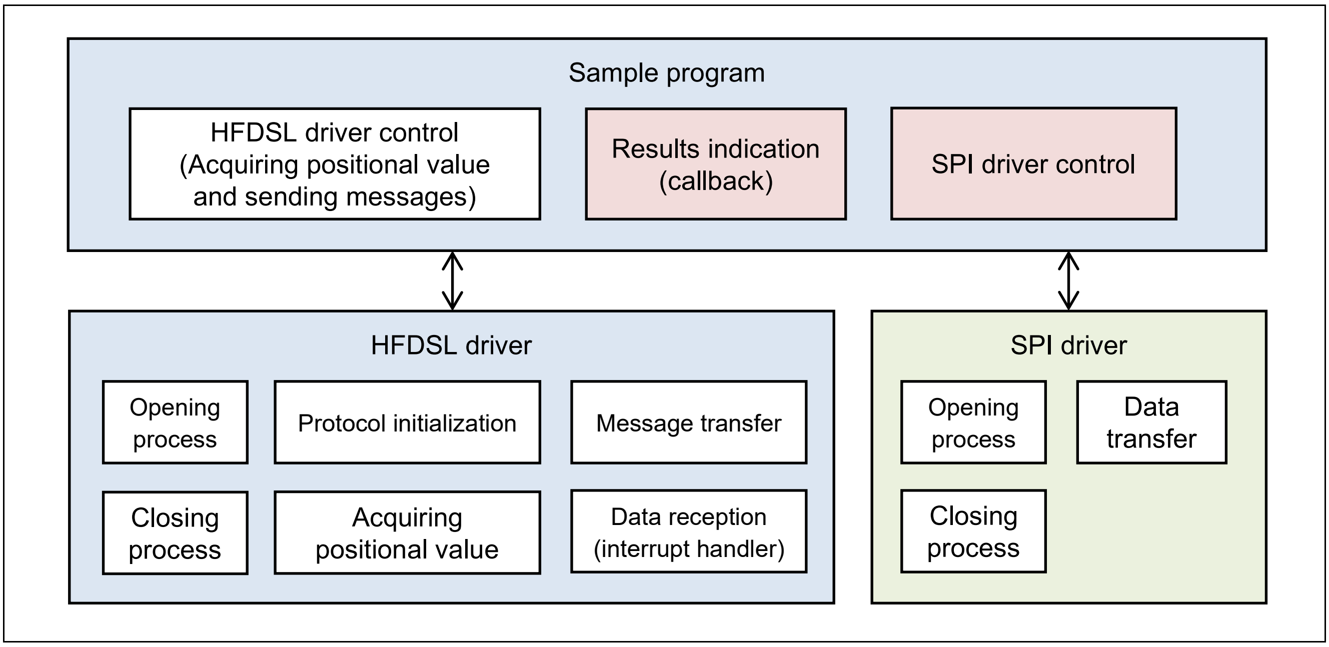


Figure 3.1 Software Configuration

3.4.2 Execution Examples of the Sample Program

In this sample program, results of the SPI interface access are indicated by a part of console commands (pos, safety) in addition to the original indication by the HIPERFACE DSL Safety sample program. Items read by the SPI interface are indicated with “(SPI)”. Other command responses are the same as that of the HIPERFACE DSL Safety sample program. See RZ/T2L Group HIPERFACE DSL Safety sample program application note for details.

The HFDSL0 channel is used by the default settings. Please execute program with connecting pins shown in the “3.2.2(4), Pin Connection on the Target Board”. In case of using the HFDSL1 channel or in case of using other HIPERFACE DSL SPI interface settings, refer “3.4.3, Build Option of the Sample Program”.

(1) Result of running

After running, it will display the command prompt following the version. Enter the command after “hfdsl >”.

```
HFDSL Safety sample program start
R_HFDSL_GetVersion = 2.0


hfdsl >
```

(2) pos command

Fast position: The result of R_HFDSL_CMD_POS in the hfdsl_int_nml_callback function is displayed.

Safe position: The result of R_HFDSL_CMD_VPOS in the hfdsl_int_nml_callback function is displayed. *1

Safe position 1 (SPI): The result of Safe channel 1 positional data read by SPI interface is displayed. *2

Error information: The result of the hfdsl_int_err_callback function is displayed.

```
hfdsl >pos
Fast position
   Rotations   : 0x00000F94
   Angle      : 0x00061DCA
Safe position
   Rotations   : --
   Angle      : --
Safe position 1 (SPI)
   Rotations   : 0x00000F94
   Angle      : 0x00061DC8
Error information
   EVENT_ERR   : 0x00000000
```

Note: 1. The safe channel 1 interface mode is SPI mode in default, and access to the safety channel 1 interface registers is disabled. Values for the safe position are shown as “--".

2. If the safe channel 1 interface mode is SPI mode, information read by SPI interface is displayed. If the safe channel 1 interface mode is switched to internal bus mode, the access by the SPI interface is disabled. Safe position 1 (SPI) shows invalid value.

(3) safety command

SAFETY POSITION 1 data: The result of the hfdsl_int_safety_callback function is displayed. *[1]

“data” are register data, “Rotations” and “Angle” are the values after conversion.

SAFETY POSITION 1 data (SPI): The result of Safe channel 1 positional data and raw data (Safe summary 1 Byte, Safe position 5 Bytes, CRC 2 Bytes in order) read by SPI interface are displayed. *[2]

“data” are register data, “Rotations” and “Angle” are the values after conversion.

SAFETY POSITION 2 data: Safety position 2 is not accessible from the internal bus. Values are displayed as “--".

SAFETY POSITION 2 data (SPI): The result of Safe channel 2 positional data and raw data (Safe channel 2 status 1 Byte, Safe position 5 Bytes, CRC 2 Bytes in order) read by SPI interface are displayed.

“data” are register data, “Rotations” and “Angle” are the values after conversion.

```
hfdsl >safety
SAFETY POSITION 1 data
   Rotations   : --
   Angle      : --
   data : -- -- -- -- -- -- -- --
SAFETY POSITION 1 data (SPI)
   Rotations   : 0x00000F94
   Angle      : 0x00063A53
   data : 0x05 0x00 0xF9 0x46 0x3A 0x53 0xBA 0xED
SAFETY POSITION 2 data
   Rotations   : --
   Angle      : --
   data : -- -- -- -- -- -- -- --
SAFETY POSITION 2 data (SPI)
   Rotations   : 0x00000F94
   Angle      : 0x000644C0
   data : 0x9C 0xFF 0x06 0xB9 0xBB 0x3F 0xD8 0xDD
```

Note:
1. The safe channel 1 interface mode is SPI mode in default, and access to the safety channel 1 interface registers is disabled. Values for the SAFETY POSITION 1 are shown as “--".
2. If the safe channel 1 interface mode is SPI mode, information read by SPI interface is displayed. If the safe channel 1 interface mode is switched to internal bus mode, the access by the SPI interface is disabled. SAFETY POSITION 1 data (SPI) shows invalid value.

3.4.3 Build Option of the Sample Program

SPI interface usage sample program is selectable its check function by setting define-statements in the source code.

Settings of the SPI interface check function in the hfdsl_main.c

With SPI interface check, safe channel 1 interface is SPI mode (Default setting)

```
#define HFDSL_ADD_SPI_CODE (1)
#define HFDSL_SPI_CHECK (1)
#define HFDSL_SAFE1_IF_MODE (R_HFDSL_SP_SPI_MODE)
```

With SPI interface check, safe channel 1 interface is internal bus mode

```
#define HFDSL_ADD_SPI_CODE (1)
#define HFDSL_SPI_CHECK (1)
#define HFDSL_SAFE1_IF_MODE (R_HFDSL_SP_INTERNAL_BUS_MODE)
```

Add SPI interface checking code without SPI interface access, safe channel 1 is SPI mode

```
#define HFDSL_ADD_SPI_CODE (1)
#define HFDSL_SPI_CHECK (0)
#define HFDSL_SAFE1_IF_MODE (R_HFDSL_SP_SPI_MODE)
```

Without SPI interface checking code, safe channel 1 is internal bus mode
(Settings equivalent to the HIPERFACE DSL Safety Sample Program)

```
#define HFDSL_ADD_SPI_CODE (0)
#define HFDSL_SAFE1_IF_MODE (R_HFDSL_SP_INTERNAL_BUS_MODE)
```

Settings of the using HIPERFACE DSL channel in the hal_entry.c

Use HFDSL0 channel (Default setting)

```
#define HFDSL_CH (0)
```

Use HFDSL1 channel

```
#define HFDSL_CH (1)
```

Revision History

Rev.	Date	Description	
		Page	Summary
2.00	Feb 21.25	-	First edition is issued.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/.