

# RZ/N2H Group

## ENCOUT sample program

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### Summary

This document describes the RZ/N2H encoder divided-output (ENCOUT) module sample program package.

### Functionality Checked Device

RZ/N2H Evaluation Board (RTK9RZN2Hxxxxxxxx)

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## 1. Package Contents

This package contains the following contents.

The RZ/N2H has one unit of ENCOUT module. The number of output channels supported by this sample program is one.

### 1.1 Software

- Source code

No.	Name	Version number
1	RZ/N2H ENCOUT sample program (CR52 ver.*)	2.0
2	RZ/N2H ENCOUT sample program (CA55 ver.*)	2.0

Note This sample program has a CR52 version that runs on the CPU core Cortex-R52 and a CA55 version that runs on the CPU core Cortex-A55. CR52 ver. and CA55 ver. are descriptions of the respective version.

### 1.2 Documents

No.	Document name	Version	File name
1	RZ/N2H Group ENCOUT sample program Release Note	2.00	(j) r11an0966jj0200-rzn2h.pdf (e) r11an0966ej0200-rzn2h.pdf (this document)
2	RZ/N2H Group ENCOUT sample program Application Note	2.00	(j) r11an0965jj0200-rzn2h-encout.pdf (e) r11an0965ej0200-rzn2h-encout.pdf

## 2. File Structure

The file structure and contents of this package are detailed below.

Top

```

├─ r11an0966jj0200-rzn2h.pdf
├─ r11an0966ej0200-rzn2h.pdf
└─ workspace
    └─ Software
        ├── iccarm
        │   ├── RZ_N2H_CR52_encout.zip      : RZ/N2H ENCOUT sample program set
        │   │                                   CR52 ver. (IAR)
        │   └─ RZ_N2H_CA55_encout.zip
        │       ├── RZ_N2H_CA55_0_encout    : RZ/N2H ENCOUT sample program set
        │       │                                   CA55 ver. (IAR)
        │       └─ RZ_N2H_CR52_0_primary    : CPU CTRL register setting program (IAR)
        └─ gcc
            ├── RZ_N2H_CR52_encout.zip      : RZ/N2H ENCOUT sample program set
            │                                   CR52 ver. (e2 studio)
            └─ RZ_N2H_CA55_encout.zip
                ├── RZ_N2H_CA55_0_encout    : RZ/N2H ENCOUT sample program set
                │                                   CA55 ver. (e2 studio)
                └─ RZ_N2H_CR52_0_primary    : CPU_CTRL register setting program (e2 studio)
└─ Documents
    ├── r11an0965jj0200-rzn2h-encout.pdf
    └─ r11an0965ej0200-rzn2h-encout.pdf

```

The file structure of the RZ\_N2H\_CR52\_encout.zip and the RZ\_N2H\_CA55\_0\_encout folder is shown below.

Top folder

```

├─ configuration.xml      : FSP Configuration data
├─ ( Build Tool Dependent Environment Files )
└─ src
    ├── hal_entry.c      : ENCOUT sample program
    ├── encout_main.c    : ENCOUT sample program
    ├── siochar.c        : SCI_UART sample program
    ├── siorw.c          : SCI_UART sample program
    ├── sio_char.h       : SCI_UART sample program
    ├── sci_uart
    └─ drv
        ├── src
        │   └─ r_encout_rzt2.c      : ENCOUT driver file
        └─ inc
            ├── iodefinc_encout.h   : ENCOUT register definition file
            ├── r_encout_rzt2_config.h : ENCOUT driver file
            └─ r_encout_rzt2_if.h    : ENCOUT driver file

```

The file structure of the RZ\_N2H\_CR52\_0\_primary folder is shown below.

Top folder

- |— configuration.xml : FSP Configuration data
- |— ( Build Tool Dependent Environment Files )
- |— src
  - |— hal\_entry.c : CA55 start-up program

### 3. About ENCOUT Sample Program

This section contains information necessary to use the complete set of ENCOUT sample program.

#### 3.1 Software Information

##### 3.1.1 Base OS

This sample program is OS-independent.

##### 3.1.2 Memory Size

Memory size used by this sample program and ENCOUT driver is shown in following table. This table does not include memory size used by Flexible Software Package or C language libraries of the compiler.

###### (1) CR52 ver.

Items		Memory Size	
		EWARM [kBytes]	e <sup>2</sup> studio [kBytes]
ENCOUT driver	Code	0.7	0.7
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.0	0.0
	Constant Data	0.0	0.0
Sample program	Code	0.7	1.1
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.0	0.0
	Constant Data	0.2	0.2

###### (2) CA55 ver.

Items		Memory Size	
		EWARM [kBytes]	e <sup>2</sup> studio [kBytes]
ENCOUT driver	Code	1.3	1.1
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.0	0.0
	Constant Data	0.1	0.0
Sample program	Code	1.2	2.0
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.0	0.0
	Constant Data	0.2	0.2

## 3.2 Hardware Information

### 3.2.1 Device

RZ/N2H

### 3.2.2 Target Board

#### (1) Board Name

RZ/N2H Evaluation Board (RTK9RZN2Hxxxxxxxx)

#### (2) Setting of the Target Board

Target board configuration is as follows.

DSW17-3: ON, DSW17-4: OFF

DSW17-5: ON, DSW17-6: OFF

DSW17-7: ON, DSW17-8: OFF

DSW3-1: ON, DSW3-2: OFF, DSW3-3: ON, DSW3-6: OFF (Set xSPI1 boot mode)

#### (3) Used Pins for the Target Board

The correspondence between the pin used by the ENCOUT and the pin header of the target board is as follows. Only channel 0 is available.

Channel	Pin name	Pin header	Input/Output	Voltage domain	Description
Channel 0	POUTA	CN43 #13	output	VDD33	Phase A output pin
	POUTB	CN43 #15	output	VDD33	Phase B output pin
	POUTZ	CN43 #17	output	VDD33	Phase Z output pin

### 3.3 Procedures on Development Environments: CR52 ver.

#### 3.3.1 Preparation before Executing the Sample Program

This sample program communicates with a PC. The USB connection terminal on the target board is CN27. Select higher-numbered port from COM ports that appear at connecting the board with the host PC.

The terminal software of the host PC is set as shown in the following table.

Function	Setting
Communication method	Asynchronous serial transmission/reception
Order of transmission / reception	LSB first
Transfer rate	19200 bps
Character length	8 bits
Stop bit length	1 bit
Parity function	None
Hardware flow control	None

#### 3.3.2 EWARM from IAR Systems

##### (1) Build Environment

IAR Embedded Workbench for Arm (EWARM)

Version 9.60.2 + patch (EWARM\_Patch\_for\_RZT2H\_N2H\_rev1.0)

RENESAS FSP Smart Configurator (FSP SC) 2024-10

RENESAS Flexible Software Package (FSP) for RZ/N2 v2.1.0

##### (2) Execution Environment ICE

IAR I-jet

##### (3) Build Procedure for Sample Programs

The build procedure for the sample program is as follows.

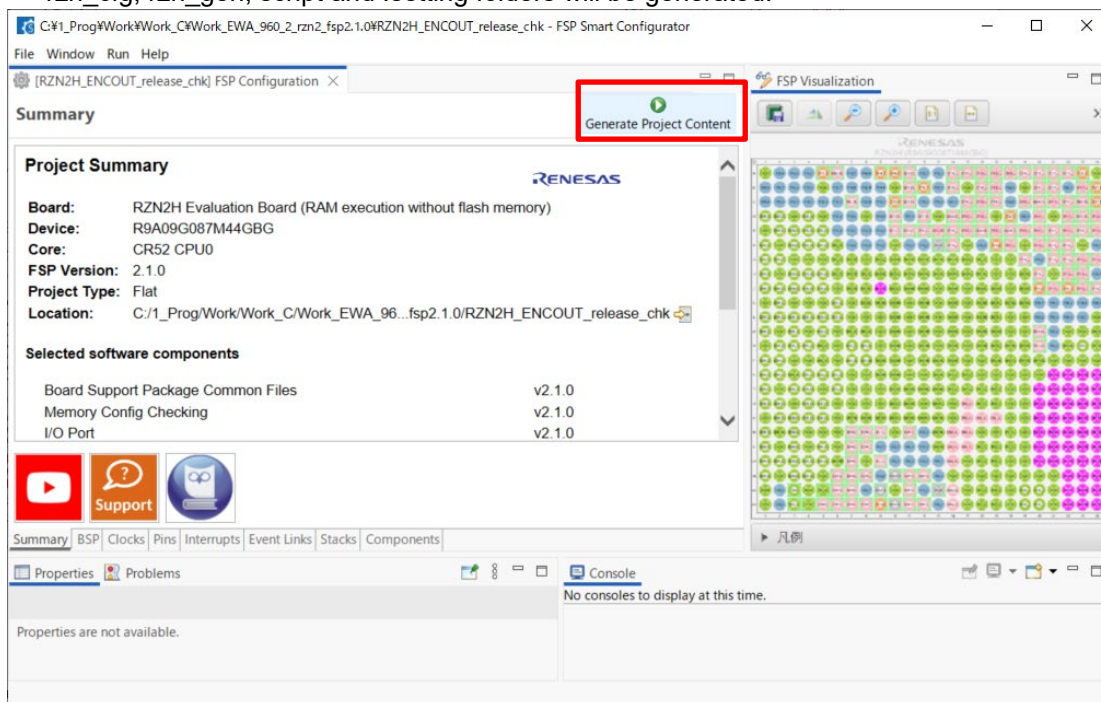
- 1 Extract RZ\_N2H\_CR52\_encout.zip and copy the extracted source files to the desired location.
- 2 Activate EWARM.
- 3 Select [File] menu -> [Open Workspace].
- 4 Open the extracted source file RZ\_N2H\_encout.eww.
- 5 Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE. \*

Note: The following procedure adds the activation of the FSP Smart Configurator to the [Tools] menu of the EWARM IDE. Select [Tools] menu -> [Tool Configuration] in the EWARM IDE. Select the [New] button, specify a table string in each field, and press [OK].

Field	String
Menu text	FSP Smart Configurator
Command	\$RASC_EXE_PATH\$
Argument	--compiler IAR configuration.xml
Initial directory	\$PROJ_DIR\$

String for the command is variable holding the path of the Smart Configurator execution file, rasc.exe. You can also start the FSP Smart Configurator directly from the command prompt by specifying the folder where it is installed.

- 6 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rzn, rzn\_cfg, rzn\_gen, script and .setting folders will be generated.



- 7 When project generation is complete, close the Smart Configurator.  
 8 Select [Rebuild ALL] from the [Project] menu of EWARM.  
 The file Debug\Exe\RZ\_N2H\_encout.out is generated.

#### (4) Sample Program Execution Procedure

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 Select [Project] menu -> [Download and Debug].
- 2 Select [Debug] menu -> [Execute].

#### (5) Execution Result of the Sample Program

The ENCOUT driver version is displayed in the terminal software window by executing this sample program. Additionally, Phase ABZ signals shown in the RZ/N2H Group ENCOUT Sample Program Application Note "4.8.9 Execution Result of the Sample Program" are outputted to the pin headers shown in "3.2.2(3) Used Pins for the Target Board".

### 3.3.3 e<sup>2</sup> studio from RENESAS

#### (1) Build Environment

RENESAS e<sup>2</sup> studio 2024-10

Toolchain version: GNU ARM Embedded 12.2.1.arm-12-24

RENESAS Flexible Software Package (FSP) for RZ/N2 v2.1.0

#### (2) Execution Environment ICE

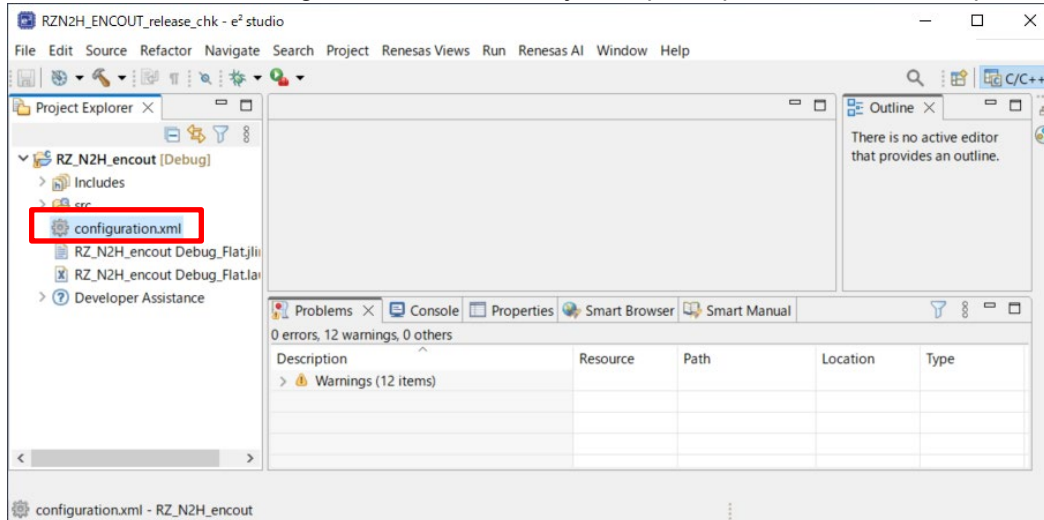
SEGGER J-Link v7.98c



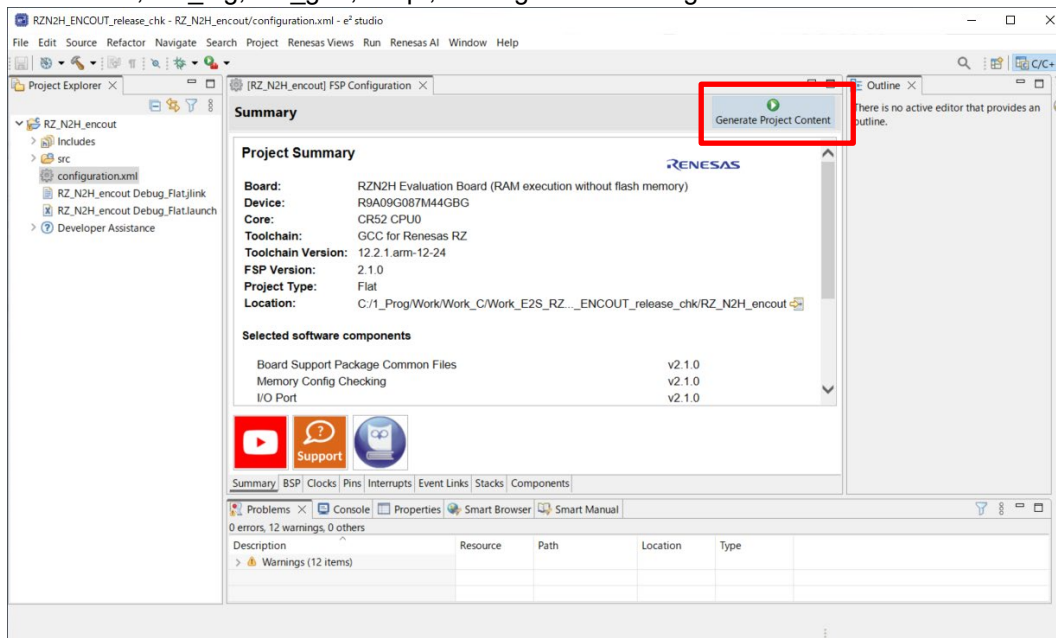
## (3) Build Procedure of the Sample Program

The procedure for building the sample program is as follows.

- 1 Extract RZ\_N2H\_CR52\_encout.zip and copy the extracted source files to the desired location.
- 2 After launching e<sup>2</sup> studio and moving to the workspace, click the [File] menu -> [Import] and select Existing project to workspace and click [Next].
- 3 On the project import screen, select the folder where the sample program was expanded as the root directory.
- 4 Select a project, check Copy Project to Workspace, and click [Finish].
- 5 Double-click the configuration.xml in the Project Explorer pane of e<sup>2</sup> studio to open it.



- 6 Click Generate Project Content in the FSP Configuration pane of e<sup>2</sup> studio.  
The rzn, rzn\_cfg, rzn\_gen, script, .settings folders are generated.



- 7 Select [Project] menu -> [Build All]  
The Debug/RZ\_N2H\_encout.elf file is generated.

#### (4) Execution Procedure of the Sample Program

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging].
- 2 Click [Debug] to start downloading to internal RAM.
- 3 Click [Run] menu -> [Resume] to run the sample program.

#### (5) Execution Result of the Sample Program

The ENCOUT driver version is displayed in the terminal software window by executing this sample program. Additionally, Phase ABZ signals shown in the RZ/N2H Group ENCOUT Sample Program Application Note "4.8.9 Execution Result of the Sample Program" are outputted to the pin headers shown in "3.2.2(3) Used Pins for the Target Board".

### 3.4 Procedures on Development Environments: CA55 ver.

#### 3.4.1 Preparation before Executing the Sample Program

This sample program communicates with a PC. The USB connection terminal on the target board is CN34. Select lower-numbered port from COM ports that appear at connecting the board with the host PC.

The terminal software of the host PC is set as shown in the following table.

Function	Setting
Communication method	Asynchronous serial transmission/reception
Order of transmission / reception	LSB first
Transfer rate	19200 bps
Character length	8 bits
Stop bit length	1 bit
Parity function	None
Hardware flow control	None

#### 3.4.2 EWARM from IAR Systems

##### (1) Build Environment

IAR Embedded Workbench for Arm

Version 9.60.2 + patch (EWARM\_Patch\_for\_RZT2H\_N2H\_rev1.0)

RENESAS FSP Smart Configurator (FSP SC) 2024-10

RENESAS Flexible Software Package (FSP) for RZ/N2 v2.1.0

##### (2) Execution Environment ICE

IAR I-jet

##### (3) Build Procedure for Sample Programs

The build procedure for the sample program is as follows.

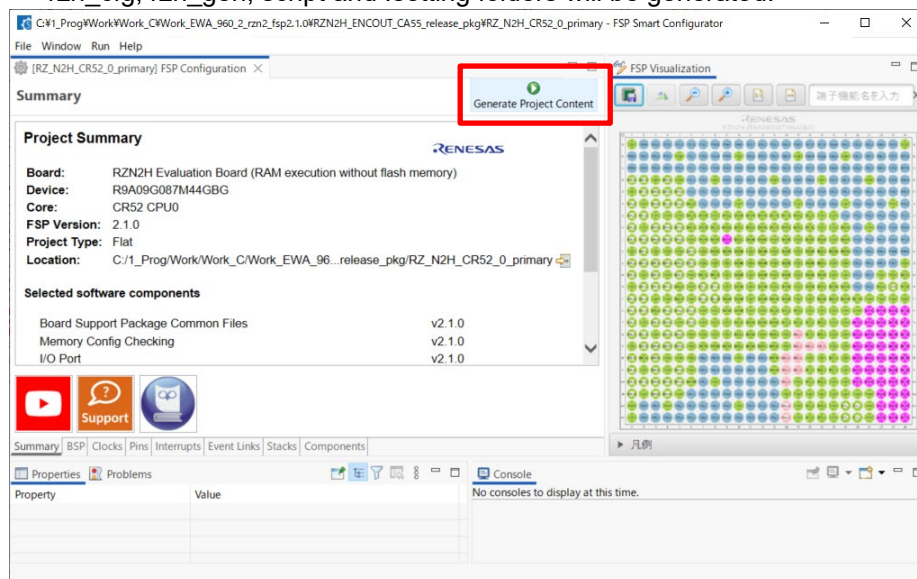
- 1 Extract RZ\_N2H\_CA55\_encout.zip and copy the extracted source files to the desired location.
- 2 Activate EWARM.
- 3 Select [File] menu -> [Open Workspace].
- 4 Open the extracted source file RZ\_N2H\_CR52\_0\_primary -> RZ\_N2H\_CR52\_0\_primary.eww.
- 5 Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE. \*

Note: The following procedure adds the activation of the FSP Smart Configurator to the [Tools] menu of the EWARM IDE. Select [Tools] menu -> [Tool Configuration] in the EWARM IDE. Select the [New] button, specify a table string in each field, and press [OK].

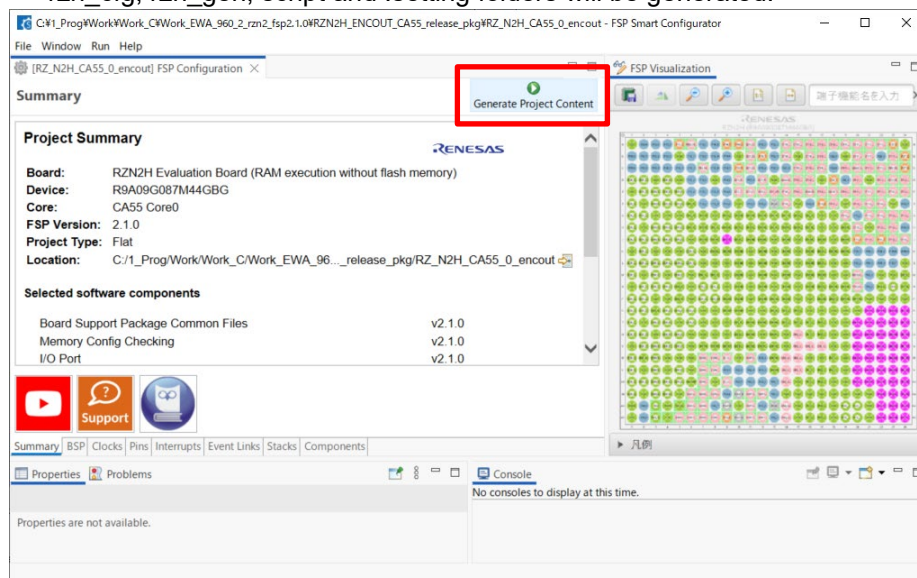
Field	String
Menu text	FSP Smart Configurator
Command	\$RASC_EXE_PATH\$
Argument	--compiler IAR configuration.xml
Initial directory	\$PROJ_DIR\$

String for the command is variable holding the path of the Smart Configurator execution file, rasc.exe. You can also start the FSP Smart Configurator directly from the command prompt by specifying the folder where it is installed.

- 6 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rzn, rzn\_cfg, rzn\_gen, script and .setting folders will be generated.



- 7 When project generation is complete, close the Smart Configurator.
- 8 Select [Rebuild ALL] from the [Project] menu of EWARM.  
The file Debug\Exe\RZ\_N2H\_CR52\_0\_primary.sbd is generated.
- 9 Select [File] menu -> [Open Workspace].
- 10 Open the extracted source file RZ\_N2H\_CA55\_0\_encout → RZ\_N2H\_CA55\_0\_encout.eww.  
(RZ\_N2H\_CR52\_0\_primary.sbd of the primary project is referenced to open this workspace file.  
Please build the primary project in advance.)
- 11 Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE.
- 12 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rzn, rzn\_cfg, rzn\_gen, script and .setting folders will be generated.



- 13 When project generation is complete, close the Smart Configurator.
- 14 Select [Rebuild ALL] from the [Project] menu of EWARM.  
The file Debug\Exe\RZ\_N2H\_CA55\_0\_encout.out is generated.

#### (4) Sample Program Execution Procedure

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 In the workspace of RZ\_N2H\_CR52\_0\_primary, select [Project] menu -> [Download and Debug]. RZ\_N2H\_CA55\_0\_encout project is launched.
- 2 In the workspace of RZ\_N2H\_CR52\_0\_primary, select [Debug] menu -> [Execute]. CA55 start-up program is executed.
- 3 In the workspace of RZ\_N2H\_CA55\_0\_encout, select [Debug] menu -> [Execute]. Sample program is executed.

#### (5) Execution Result of the Sample Program

The ENCOUT driver version is displayed in the terminal software window by executing this sample program. Additionally, Phase ABZ signals shown in the RZ/N2H Group ENCOUT Sample Program Application Note “4.8.9 Execution Result of the Sample Program” are outputted to the pin headers shown in “3.2.2(3) Used Pins for the Target Board”.

### 3.4.3 e<sup>2</sup> studio from RENESAS

#### (1) Build Environment

RENESAS e<sup>2</sup> studio 2024-10

Toolchain version:

GNU ARM Embedded 12.2.1.arm-12-24 (Used by RZ\_N2H\_CR52\_0\_primary)

GCC ARM A-Profile (Aarch64 bare-metal) 10.3.1.20210621 (Used by RZ\_N2H\_CA55\_0\_encout)

RENESAS Flexible Software Package (FSP) for RZ/N2 v2.1.0

#### (2) Execution Environment ICE

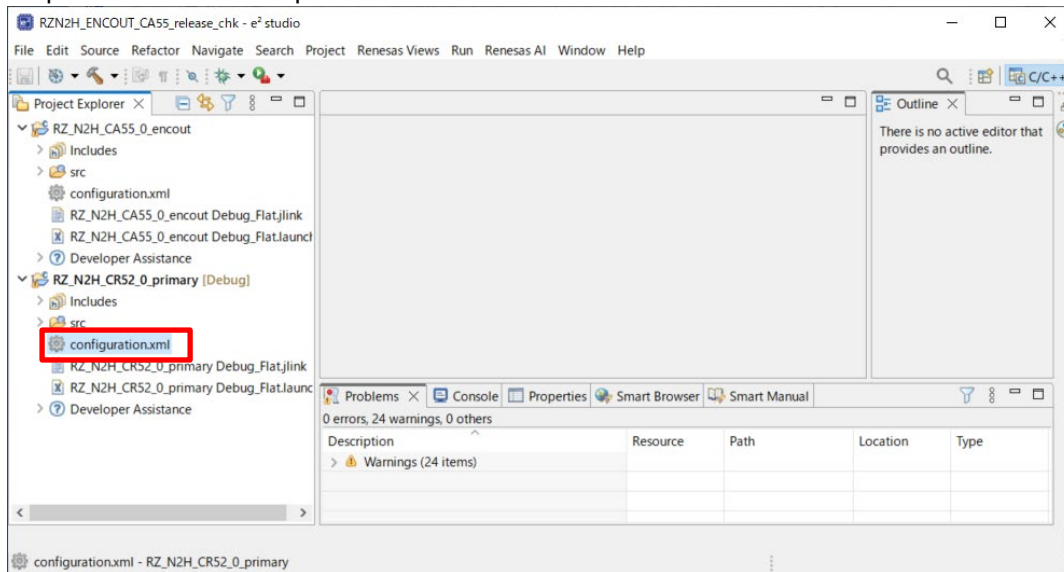
SEGGER J-Link v7.98c

#### (3) Build Procedure of the Sample Program

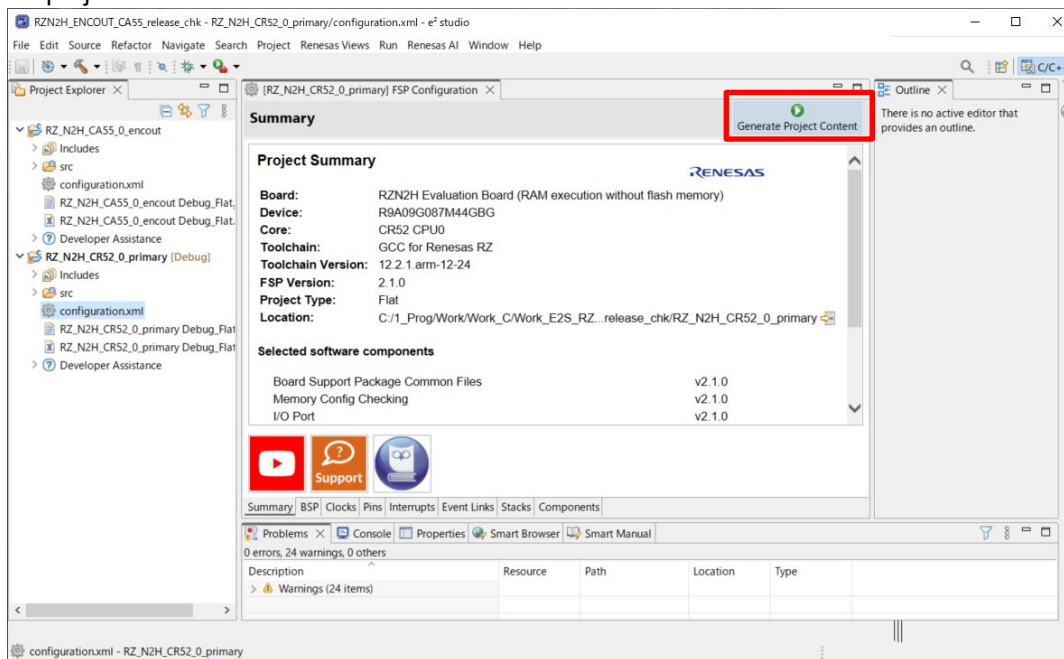
The procedure for building the sample program is as follows.

- 1 Extract RZ\_N2H\_CA55\_encout.zip and copy the extracted source files to the desired location.
- 2 After launching e<sup>2</sup> studio and moving to the workspace, click the [File] menu -> [Import] and select Existing project to workspace and click [Next].
- 3 On the project import screen, select the folder where the sample program was expanded as the root directory.
- 4 Select a project, check Copy Project to Workspace, and click [Finish].

- 5 Double-click the configuration.xml of the RZ\_N2H\_CR52\_0\_primary project in the Project Explorer pane of e<sup>2</sup> studio to open it.

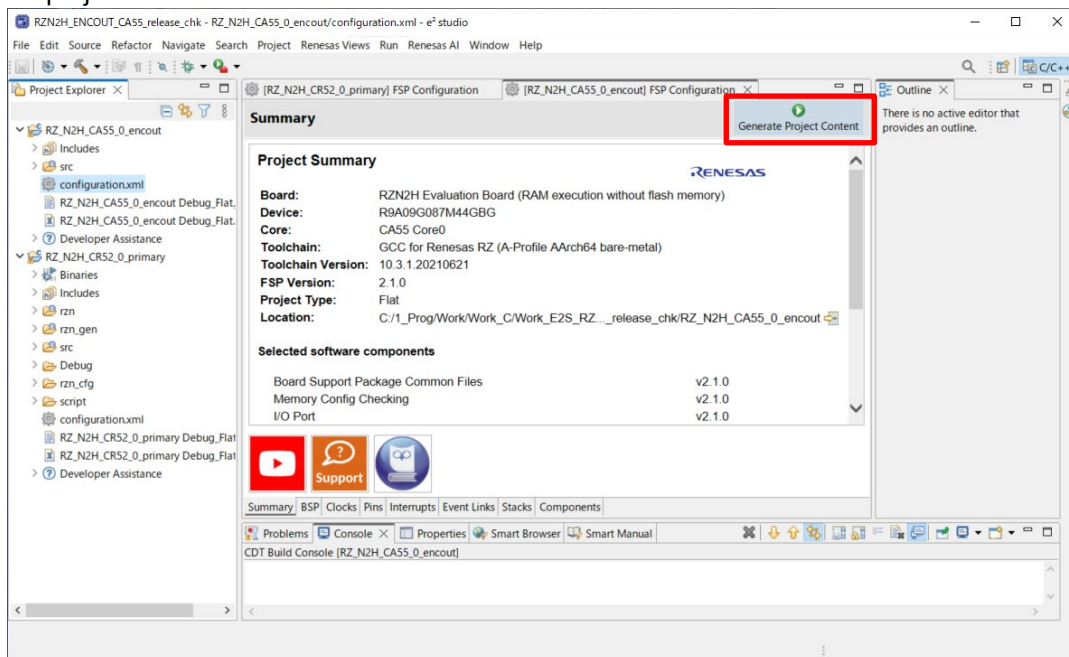


- 6 Click Generate Project Content in the FSP Configuration pane of e<sup>2</sup> studio. The rzn, rzn\_cfg, rzn\_gen, script, .settings folders are generated in the RZ\_N2H\_CR52\_0\_primary project.



- 7 Select RZ\_N2H\_CR52\_primary project in the Project Explorer pane and execute [Run] menu -> [Build Project].  
The file Debug\RZ\_N2H\_CR52\_0\_primary.sbd is generated.
- 8 Double-click the configuration.xml of the RZ\_N2H\_CA55\_0\_encout project in the Project Explorer pane of e<sup>2</sup> studio to open it.

- Click Generate Project Content in the FSP Configuration pane of e<sup>2</sup> studio.  
The rzn, rzn\_cfg, rzn\_gen, script, .settings folders are generated in the RZ\_N2H\_CA55\_0\_encout project.

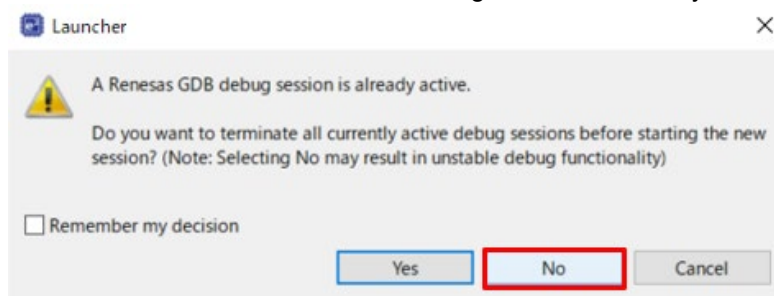


- Select [Project] menu -> [Build All]  
The Debug\RZ\_N2H\_CA55\_0\_encout.elf file is generated.

#### (4) Execution Procedure of the Sample Program

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging] for the RZ\_N2H\_CR52\_0\_primary project.  
Click [Debug] to start downloading to internal RAM.
- Click [Run] menu -> [Resume] to run the CA55 start-up program.
- Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging] for the RZ\_N2H\_CA55\_0\_encout project.
- Select 'No' when 'A Renesas GDB debug session is already active' is displayed.



- If 'Proceed with launch' is displayed, select 'Yes'.
- Click [Debug] to start downloading to internal RAM.
- Click [Run] menu -> [Resume] to run the sample program.

(5) Execution Result of the Sample Program

The ENCOUT driver version is displayed in the terminal software window by executing this sample program. Additionally, Phase ABZ signals shown in the RZ/N2H Group ENCOUT Sample Program Application Note “4.8.9 Execution Result of the Sample Program” are outputted to the pin headers shown in “3.2.2(3) Used Pins for the Target Board”.



## Revision History

Rev.	Date	Description	
		Page	Summary
2.00	Dec 23.24	-	First Edition issued

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
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