RZ/N2H Group

Encoder I/F HIPERFACE DSL sample program

Summary

This document describes the RZ/N2H Encoder I/F HIPERFACE DSL® sample program package.

For HIPERFACE DSL® communication protocol specifications and encoder specifications, contact SICK AG.

Functionality Checked Device

RZ/N2H Evaluation Board (RTK9RZN2Hxxxxxxxxx)

Contents

HIPEFACE DSL is a registered trademark of SICK AG.

1. Package Contents

This package contains the following contents.

The RZ/N2H encoder interface supports up to 13 axes, but the sample program uses only 1 axis of them. If you use it with 2 axes or more simultaneously, modify the sample program to support required axes.

1.1 Software

- Source Code

No.	Name	Version number
1	RZ/N2H HIPERFACE DSL sample program (CR52 ver. *)	2.0
2	RZ/N2H HIPERFACE DSL sample program (CA55 ver. *)	2.0

Note: This sample program has a CR52 version that runs on the CPU core Cortex-R52 and a CA55 version that runs on the CPU core Cortex-A55. CR52 ver. and CA55 ver. are descriptions of the respective version.

1.2 Documents

No.	Document name	Version	File name
1	RZ/N2H Group Encoder I/F HIPERFACE DSL sample program Release Note	2.00	(j) r11an0926jj0200-rzn2h.pdf (e) r11an0926ej0200-rzn2h.pdf (this document)
2	RZ/N2H Group HIPERFACE DSL Sample Program Application Note	2.00	(j) r11an0925jj0200-rzn2h-hfdsl.pdf (e) r11an0925ej0200-rzn2h-hfdsl.pdf

2. File Structure

The file structure and contents of this package are detailed below.

```
Top
├── r11an0926jj0200-rzn2h.pdf
├── r11an0926ej0200-rzn2h.pdf
└── workspace
    ├── Software
    │   ├── iccarm
    │   │   ├── RZ_N2H_CR52_hfdsl.zip        : RZ/N2H HIPERFACE DSL sample program
    │   │   │                                   CR52 ver. (IAR) set
    │   │   └── RZ_N2H_CA55_hfdsl.zip
    │   │       ├── RZ_N2H_CA55_0_hfdsl      : RZ/N2H HIPERFACE DSL sample program
    │   │       │                               CA55 ver. (IAR) set
    │   │       └── RZ_N2H_CR52_0_primary
    │   │                                     : CPU_CTRL register setting program (IAR)
    │   └── gcc
    │       ├── RZ_N2H_CR52_hfdsl.zip        : RZ/N2H HIPERFACE DSL sample program
    │       │                                   CR52 ver. (e2 studio) set
    │       └── RZ_N2H_CA55_hfdsl.zip
    │           ├── RZ_N2H_CA55_0_hfdsl      : RZ/N2H HIPERFACE DSL sample program
    │           │                               CA55 ver. (e2 studio) set
    │           └── RZ_N2H_CR52_0_primary
    │                                         : CPU_CTRL register setting program (e2 studio)
    └── Documents
        ├── r11an0925jj0200-rzn2h-hfdsl.pdf
        └── r11an0925ej0200-rzn2h-hfdsl.pdf
```

The file structure of the RZ_N2H_CR52_hfdsl.zip and RZ_N2H_CA55_0_hfdsl folder are shown below.

```
Top folder
├── configuration.xml                 : FSP Configuration data
├── ( Environment File Depending on Build Tool )
└── src
    ├── hal_entry.c                   : HIPERFACE DSL sample program
    ├── hfdsl_main.c                  : HIPERFACE DSL sample program
    ├── siochar.c                     : SCI_UART sample program
    ├── siorw.c                       : SCI_UART sample program
    ├── sio_char.h                    : SCI_UART sample program
    └── drv
        └── hfdsl
            ├── iodefine_hfdsl.h      : HFDSL register definition file
            ├── r_hfdsl_rzt2.c        : HFDSL driver file
            ├── r_hfdsl_rzt2_config.h : HFDSL driver file
            ├── r_hfdsl_rzt2_dat.h    : HFDSL driver file
            └── r_hfdsl_rzt2_if.h     : HFDSL driver file
```

The file structure of the RZ_N2H_CR52_0_primary folder is shown below.

```
Top folder
 ├── configuration.xml                    : FSP Configuration data
 ├── ( Environment File Depending on Build Tool )
 └── src
      └── hal_entry.c                     : CA55 start-up program
```

3. About HIPERFACE DSL Sample Program

This section contains information necessary to use the complete set of HIPERFACE DSL

3.1 Software Information

3.1.1 Base OS

This sample program is OS-independent.

3.1.2 Memory Size

Memory size used by this sample program and HFDSL driver is shown in the following table. This table does not include the memory size used by Flexible Software Package or C language libraries of the compiler.

(1) CR52 ver.

Items		Memory Size	
		EWARM [kBytes]	e² studio [kBytes]
HFDSL driver	Code	3.4	2.5
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.4	0.4
	Constant Data	0.3	0.3
Sample program	Code	1.8	2.1
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.3	0.3
	Constant Data	0.9	0.9

(2) CA55 ver.

Items		Memory Size	
		EWARM [kBytes]	e² studio [kBytes]
HFDSL driver	Code	4.9	4.0
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.6	0.6
	Constant Data	0.5	0.6
Sample program	Code	3.1	3.8
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.3	0.3
	Constant Data	0.9	0.9

3.2 Hardware Information

3.2.1 Device

RZ/N2H

3.2.2 Target Board

(1) Board Name

RZ/N2H Evaluation Board (RTK9RZN2Hxxxxxxxxx)

(2) Setting of the Target Board

The target board configuration is as follows. Do not push SW4 while you are using channel HFDSL14.

DSW2-4: ON, DSW2-6: OFF

DSW5-1: OFF, DSW5-2: OFF, DSW5-7: OFF, DSW5-8: OFF

DSW7-3: OFF, DSW7-4: ON

DSW12-5: ON, DSW12-6: OFF, DSW12-7: ON, DSW12-8: OFF

DSW13-1: OFF, DSW13-2: ON, DSW13-3: OFF, DSW13-4: ON, DSW13-7: ON, DSW13-8: OFF

DSW18-5: OFF, DSW18-6: ON

DSW19-3: OFF, DSW19-4: ON

DSW20-1: OFF, DSW20-3: OFF, DSW20-5: OFF

DSW21-2: OFF, DSW21-3: ON, DSW21-4: OFF, DSW21-5: ON, DSW21-6: OFF

DSW3-1: ON, DSW3-2: OFF, DSW3-3: ON, DSW3-6: OFF (Set xSPI1 boot mode)

JP8: Short between 2-3 pins (Set VDD1833_2 to 3.3 V)

JP9: Short between 2-3 pins (Set VDD1833_3 to 3.3 V)

JP23: Short between 1-2 pins, Open between 3-4 pins, and between 5-6 pins (Set VDD1833_6 to 3.3 V)

(3) Used pins of the Target Board

The correspondence between the pin used as the encoder I/F and the pin header of the target board is as follows. Channels HFDSL8, HFDSL12 and HFDSL15 are not available.

Channel	Port Name	Pin Header	Input/Output	Voltage Domain	Description
HFDSL0	ENCIFDI00 (dsl_in)	CN44 #9	Input	VDD33	Data input
	ENCIFDO00 (dsl_out)	CN44 #7	Output	VDD33	Data output
	ENCIFOE00 (dsl_en)	CN44 #5	Output	VDD33	Drive/receive control
HFDSL1	ENCIFDI01 (dsl_in)	CN44 #8	Input	VDD33	Data input
	ENCIFDO01 (dsl_out)	CN44 #6	Output	VDD33	Data output
	ENCIFOE01 (dsl_en)	CN44 #4	Output	VDD1833_5	Drive/receive control
HFDSL2	ENCIFDI02 (dsl_in)	CN43 #23	Input	VDD33	Data input
	ENCIFDO02 (dsl_out)	CN43 #21	Output	VDD33	Data output
	ENCIFOE02 (dsl_en)	CN43 #27	Output	VDD33	Drive/receive control
HFDSL3	ENCIFDI03 (dsl_in)	CN43 #24	Input	VDD1833_6	Data input
	ENCIFDO03 (dsl_out)	CN43 #22	Output	VDD1833_6	Data output
	ENCIFOE03 (dsl_en)	CN43 #18	Output	VDD1833_6	Drive/receive control
HFDSL4	ENCIFDI04(dsl_in)	CN44 #27	Input	VDD33	Data input
	ENCIFDO04 (dsl_out)	CN44 #25	Output	VDD33	Data output
	ENCIFOE04 (dsl_en)	CN44 #23	Output	VDD33	Drive/receive control
HFDSL5	ENCIFDI05 (dsl_in)	CN43 #14	Input	VDD1833_6	Data input

Channel	Port Name	Pin Header	Input/Output	Voltage Domain	Description
	ENCIFDO05 (dsl_out)	CN43 #12	Output	VDD1833_6	Data output
	ENCIFOE05 (dsl_en)	CN43 #10	Output	VDD1833_6	Drive/receive control
HFDSL6	ENCIFDI06 (dsl_in)	CN42 #18	Input	VDD1833_3	Data input
	ENCIFDO06 (dsl_out)	CN42 #16	Output	VDD1833_3	Data output
	ENCIFOE06 (dsl_en)	CN42 #14	Output	VDD1833_3	Drive/receive control
HFDSL7	ENCIFDI07 (dsl_in)	CN42 #36	Input	VDD1833_3	Data input
	ENCIFDO07 (dsl_out)	CN42 #34	Output	VDD1833_3	Data output
	ENCIFOE07 (dsl_en)	CN42 #24	Output	VDD1833_3	Drive/receive control
HFDSL9	ENCIFDI09 (dsl_in)	CN51 #18	Input	VDD1833_2	Data input
	ENCIFDO09 (dsl_out)	CN51 #16	Output	VDD1833_2	Data output
	ENCIFOE09 (dsl_en)	CN51 #14	Output	VDD1833_2	Drive/receive control
HFDSL10	ENCIFDI10 (dsl_in)	CN51 #27	Input	VDD1833_2	Data input
	ENCIFDO10 (dsl_out)	CN51 #25	Output	VDD1833_2	Data output
	ENCIFOE10 (dsl_en)	CN51 #23	Output	VDD1833_2	Drive/receive control
HFDSL11	ENCIFDI11 (dsl_in)	CN51 #26	Input	VDD1833_2	Data input
	ENCIFDO11 (dsl_out)	CN51 #24	Output	VDD1833_2	Data output
	ENCIFOE11 (dsl_en)	CN51 #22	Output	VDD1833_2	Drive/receive control
HFDSL13	ENCIFDI13 (dsl_in)	CN43 #32	Input	VDD1833_6	Data input
	ENCIFDO13 (dsl_out)	CN43 #30	Output	VDD1833_6	Data output
	ENCIFOE13 (dsl_en)	CN43 #28	Output	VDD1833_6	Drive/receive control
HFDSL14	ENCIFDI14 (dsl_in)	CN42 #35	Input	VDD33	Data input
	ENCIFDO14 (dsl_out)	CN42 #33	Output	VDD33	Data output
	ENCIFOE14 (dsl_en)	CN42 #31	Output	VDD33	Drive/receive control

3.3 Procedures on Development Environments: CR52 ver.

3.3.1 Preparation before Executing the Sample Program

This sample program communicates with a PC. The USB connection terminal on the target board is CN27.
Select higher-numbered port from COM ports that appear at connecting the board with the host PC.
The terminal software of the host PC is set as shown in the following table.

Function	Setting
Communication method	Asynchronous serial transmission/reception
Sending / receiving order	LSB first
Transfer rate	19200 bps
Character length	8 bits
Stop bit length	1 bit
Parity function	None
Hardware flow control	None

3.3.2 EWARM from IAR Systems

(1) Build Environment

IAR Embedded Workbench for Arm (EWARM)

Version 9.60.2 + patch (EWARM_Patch_for_RZT2H_N2H_rev1.0)

RENESAS FSP Smart Configurator (FSP SC) 2024-10

RENESAS Flexible Software Package (FSP) for RZ/N2 v2.1.0

(2) Execution Environment ICE

IAR I-jet

(3) Build Procedure for Sample Programs

The build procedure for the sample program is as follows.

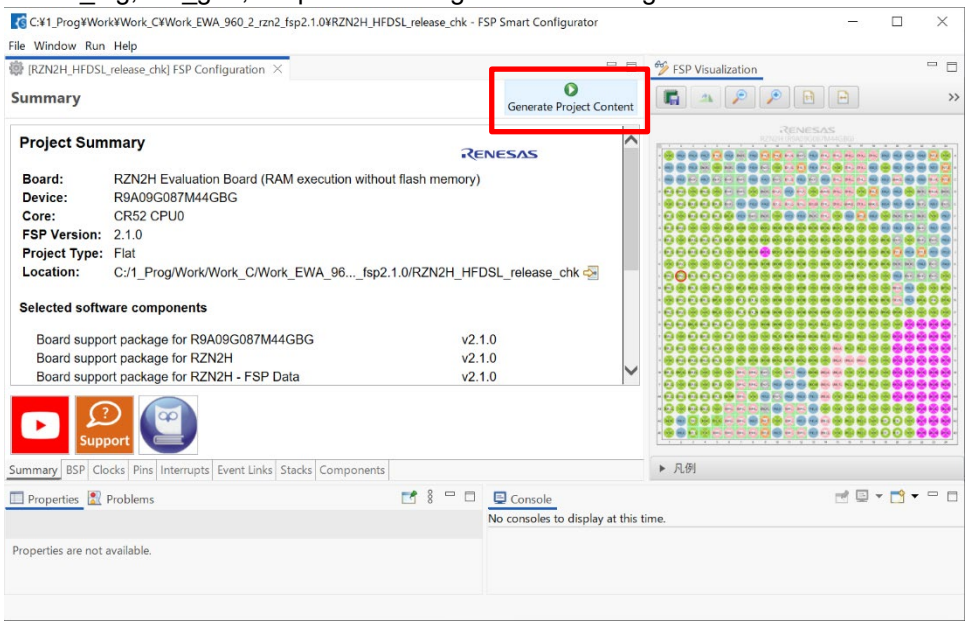
1. Extract RZ_N2H_CR52_hfdsl.zip and copy the extracted source files to the desired location.
2. Activate EWARM.
3. Select [File] menu -> [Open Workspace].
4. Open the extracted source file RZ_N2H_hfdsl.eww.
5. Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE. *

Note: The following procedure adds the activation of the FSP Smart Configurator to the [Tools] menu of the EWARM IDE. Select [Tools] menu -> [Tool Configuration] in the EWARM IDE. Select the [New] button, specify a table string in each field, and press [OK].

Field	String
Menu text	FSP Smart Configurator
Command	$RASC_EXE_PATH$
Argument	--compiler IAR configuration.xml
Initial directory	$PROJ_DIR$

String for the command is variable holding the path of the Smart Configurator execution file, rasc.exe. You can also start the FSP Smart Configurator directly from the command prompt by specifying the folder where it is installed.

6 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rzn, rzn_cfg, rzn_gen, script and .setting folders will be generated.



7 When project generation is complete, close the Smart Configurator.
8 Select [Rebuild All] from the [Project] menu of EWARM.
The file Debug\Exe\RZ_N2H_hfdsl.out is generated.

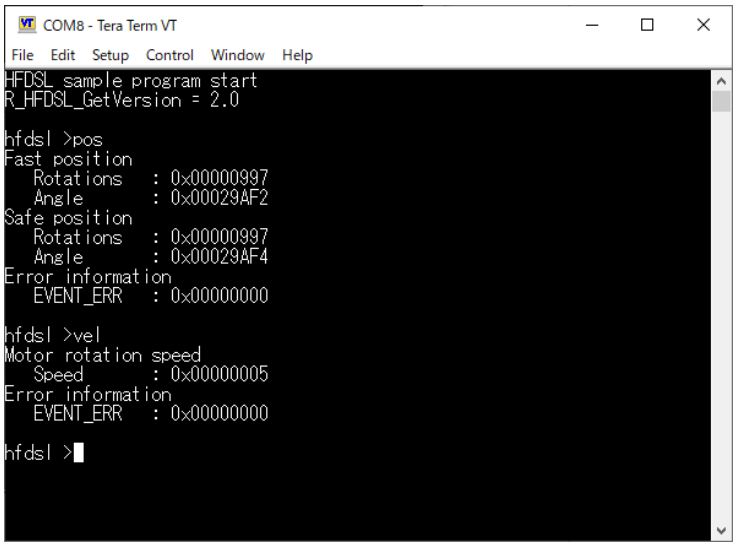
(4) Sample Program Execution Procedure

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

1 Select [Project] menu -> [Download and Debug].
2 Select [Debug] menu -> [Execute].

(5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.6 console commands in the RZ/N2H Group HIPERFACE DSL Sample Program Application Note.



3.3.3 e² studio from RENESAS

(1) Build Environment

RENESAS e² studio 2024-10

Toolchain version: GNU ARM Embedded 12.2.1.arm-12-24

RENESAS Flexible Software Package (FSP) for RZ/N2 v2.1.0

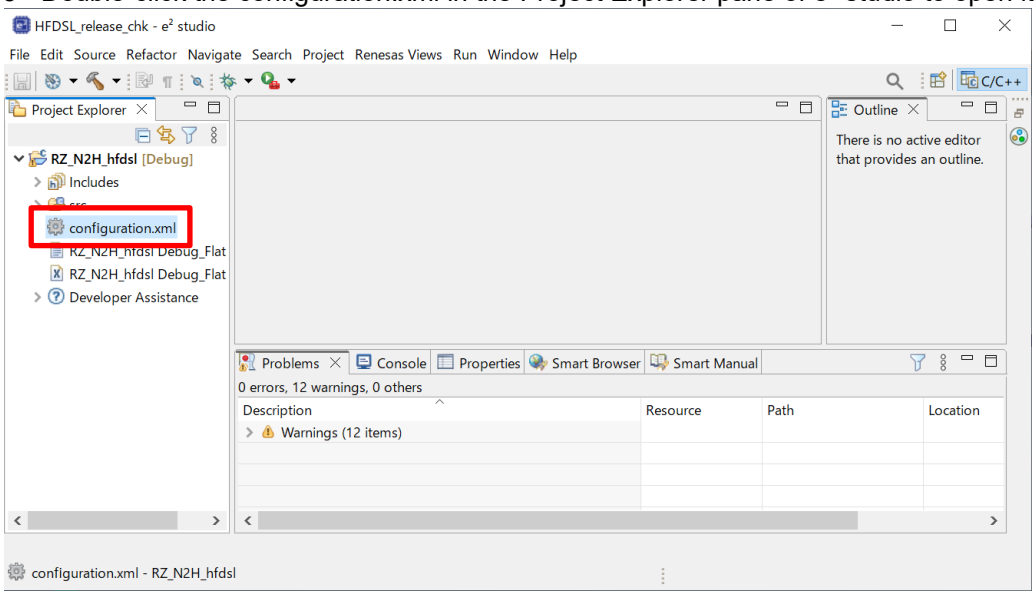
(2) Execution Environment ICE

SEGGER J-Link v7.98c

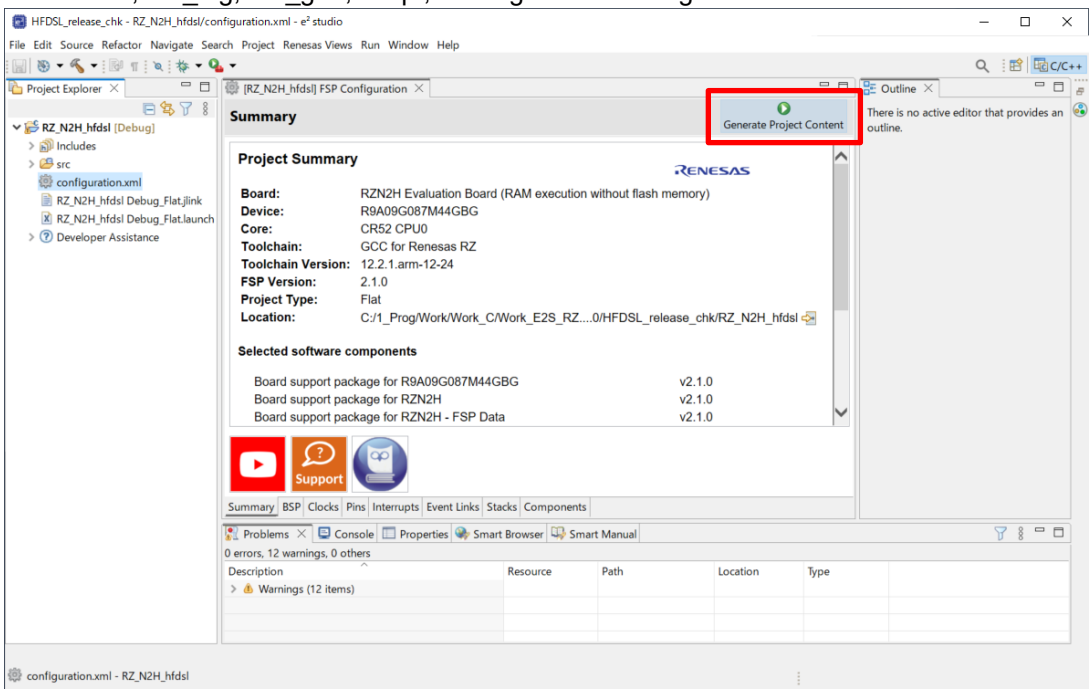
(3) Build Procedure of the Sample Program

The procedure for building the sample program is as follows.

1. Extract RZ_N2H_CR52_hfdsl.zip and copy the extracted source files to the desired location.
2. After launching e² studio and moving to the workspace, click the [File] menu-> [Import] and select Existing project to workspace and click [Next].
3. On the project import screen, select the folder where the sample program was expanded as the root directory.
4. Select a project, check Copy Project to Workspace, and click [Finish].
5. Double-click the configuration.xml in the Project Explorer pane of e² studio to open it.



6 Click Generate Project Content in the FSP Configuration pane of e² studio.
The rzn, rzn_cfg, rzn_gen, script, .settings folders are generated.



7 Select [Project] menu -> [Build All].
The Debug\RZ_N2H_hfdsl.elf file is generated.

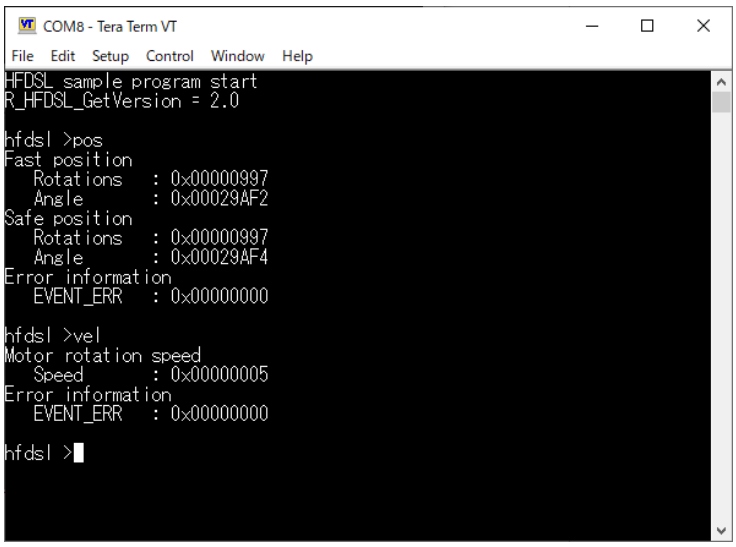
(4) Execution Procedure of the Sample Program

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

1 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging].
2 Click [Debug] to start downloading to internal RAM.
3 Click [Run] menu -> [Resume] to run the sample program.

(5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.6 console commands in the RZ/N2H Group HIPERFACE DSL Sample Program Application Note.



3.4 Procedures on Development Environments: CA55 ver.

3.4.1 Preparation before Executing the Sample Program

This sample program communicates with a PC. The USB connection terminal on the target board is CN27.
Select lower-numbered port from COM ports that appear at connecting the board with the host PC.
The terminal software of the host PC is set as shown in the following table.

Function	Setting
Communication method	Asynchronous serial transmission/reception
Sending / receiving order	LSB first
Transfer rate	19200 bps
Character length	8 bits
Stop bit length	1 bit
Parity function	None
Hardware flow control	None

3.4.2 EWARM from IAR Systems

(1) Build Environment

IAR Embedded Workbench for Arm (EWARM)

Version 9.60.2 + patch (EWARM Patch for RZT2H_N2H_rev1.0)

RENESAS FSP Smart Configurator (FSP SC) 2024-10

RENESAS Flexible Software Package (FSP) for RZ/N2 v2.1.0

(2) Execution Environment ICE

IAR I-jet

(3) Build Procedure for Sample Programs

The build procedure for the sample program is as follows.

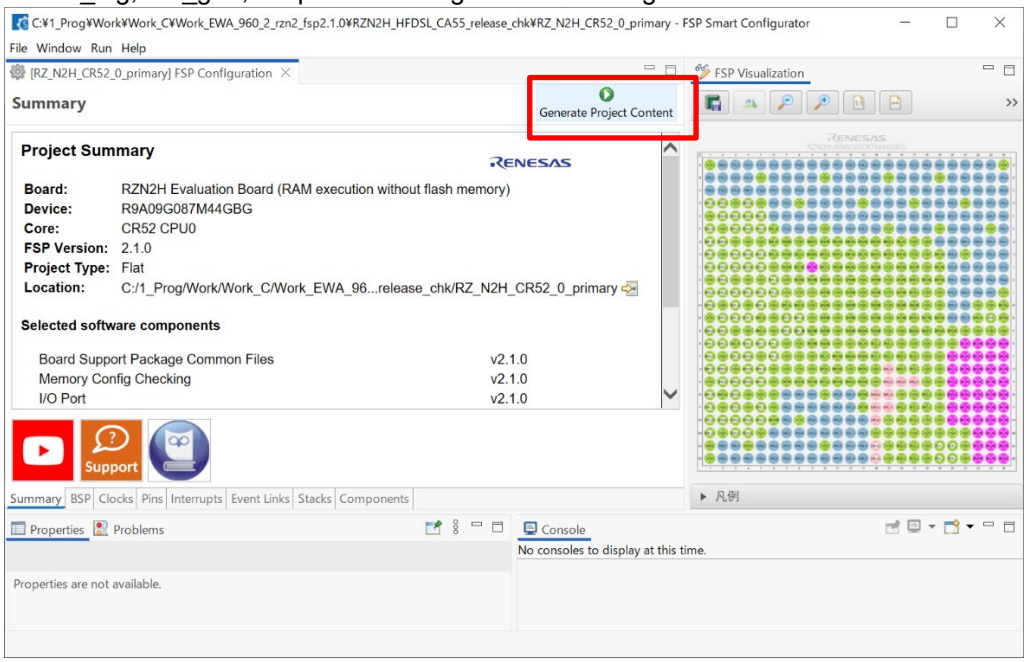
1. Extract RZ_N2H_CA55_hfdsl.zip and copy the extracted source files to the desired location.
2. Activate EWARM.
3. Select [File] menu -> [Open Workspace].
4. Open the extracted source file RZ_N2H_CR52_0_primary -> RZ_N2H_CR52_0_primary.eww.
5. Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE. *

Note: The following procedure adds the activation of the FSP Smart Configurator to the [Tools] menu of the EWARM IDE. Select [Tools] menu -> [Tool Configuration] in the EWARM IDE. Select the [New] button, specify a table string in each field, and press [OK].

Field	String
Menu text	FSP Smart Configurator
Command	$RASC_EXE_PATH$
Argument	--compiler IAR configuration.xml
Initial directory	$PROJ_DIR$

String for the command is variable holding the path of the Smart Configurator execution file, rasc.exe. You can also start the FSP Smart Configurator directly from the command prompt by specifying the folder where it is installed.

6 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rzn, rzn_cfg, rzn_gen, script and .setting folders will be generated.



7 When project generation is complete, close the Smart Configurator.

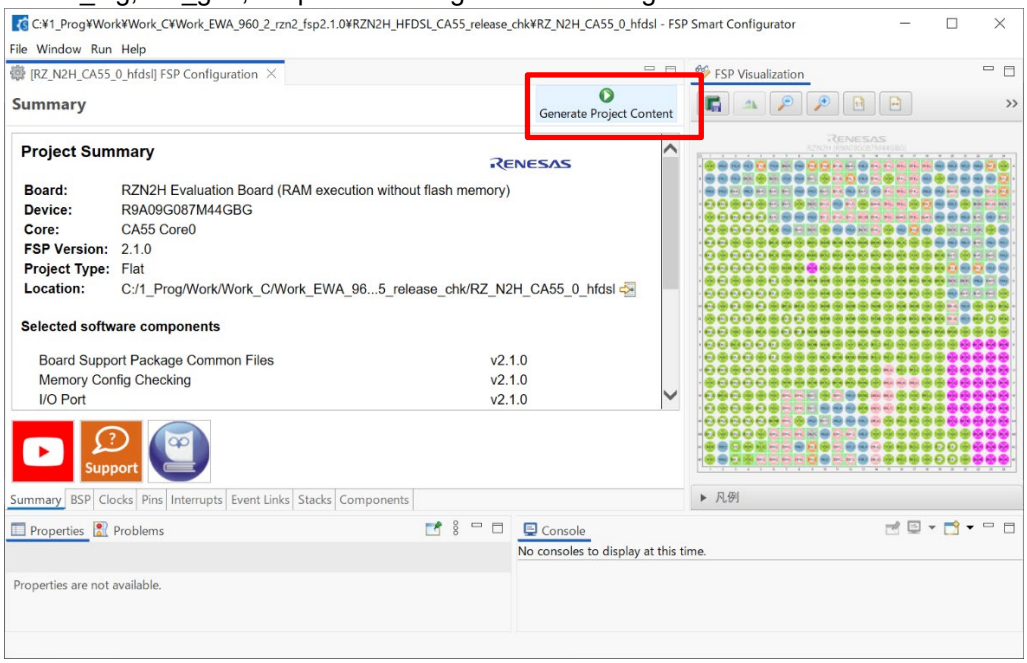
8 Select [Rebuild All] from the [Project] menu of EWARM.
The file Debug\Exe\RZ_N2H_CR52_0_primary.sbd is generated.

9 Select [File] menu -> [Open Workspace].

10 Open the extracted source file RZ_N2H_CA55_0_hfdsl → RZ_N2H_CA55_0_hfdsl.eww.
(RZ_N2H_CR52_0_primary.sbd of the primary project is referenced to open this workspace file.
Please build the primary project in advance.)

11 Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE.

12 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rzn, rzn_cfg, rzn_gen, script and .setting folders will be generated.



13 When project generation is complete, close the Smart Configurator.

14 Select [Rebuild ALL] from the [Project] menu of EWARM.
The file Debug\Exe\ RZ_N2H_CA55_0_hfdsl.out is generated.

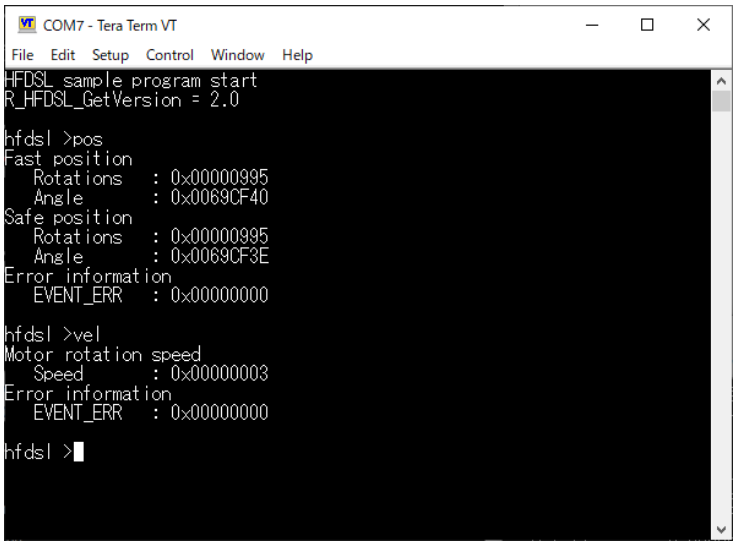
(4) Sample Program Execution Procedure

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

1 In the workspace of RZ_N2H_CR52_0_primary, select [Project] menu -> [Download and Debug]. RZ_N2H_CA55_0_hfdsl project is launched.
2 In the workspace of RZ_N2H_CR52_0_primary, select [Debug] menu -> [Execute]. CA55 start-up program is executed.
3 In the workspace of RZ_N2H_CA55_0_hfdsl, select [Debug] menu -> [Execute]. Sample program is executed.

(5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.6 console commands in the RZ/N2H Group HIPERFACE DSL Sample Program Application Note.



3.4.3 e² studio from RENESAS

(1) Build Environment

RENESAS e² studio 2024-10

Toolchain version:

GNU ARM Embedded 12.2.1.arm-12-24 (Used by RZ_N2H_CR52_0_primary.)

GCC ARM A-Profile (AArch64 bare-metal) 10.3.1.20210621 (Used by RZ_N2H_CA55_0_hfdsl)

RENESAS Flexible Software Package (FSP) for RZ/N2 v2.1.0

(2) Execution Environment ICE

SEGGER J-Link v7.98c

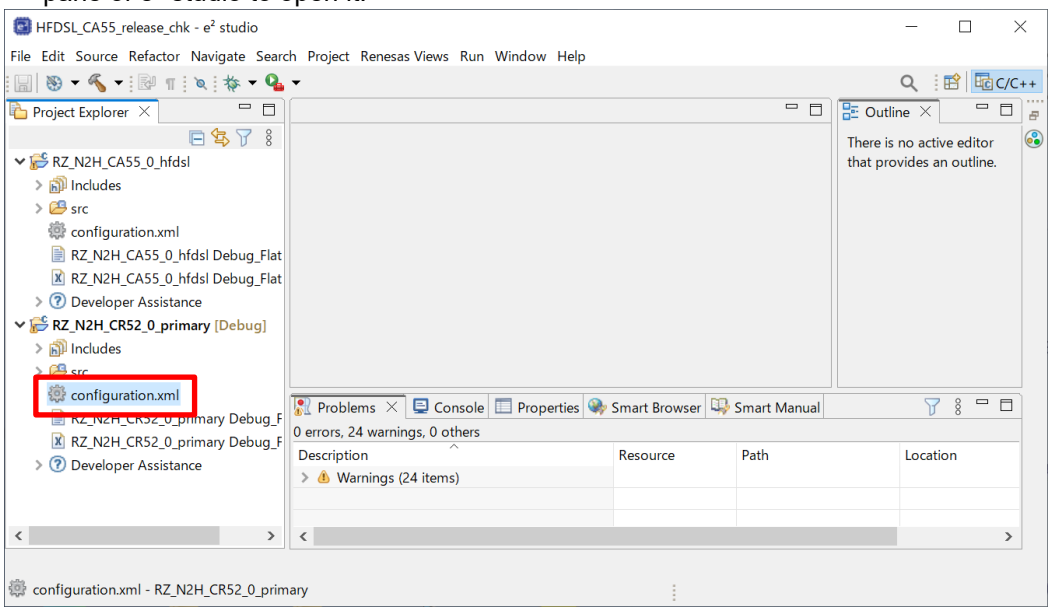
(3) Build Procedure of the Sample Program

The procedure for building the sample program is as follows.

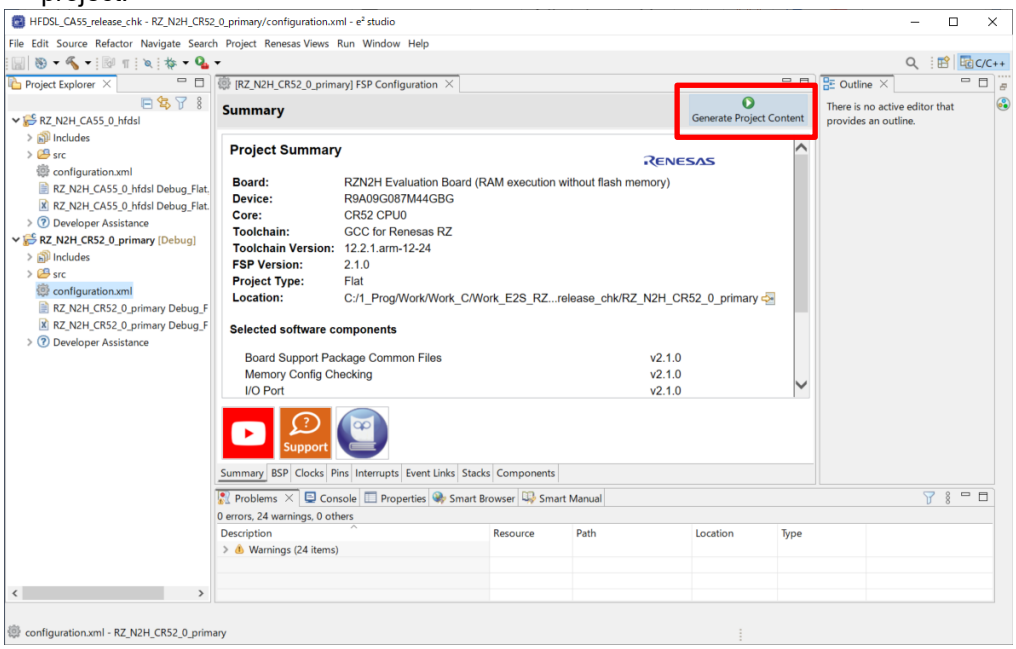
1 Extract RZ_N2H_CA55_hfdsl.zip and copy the expanded source file to any location.
2 After launching e² studio and moving to the workspace, click the [File] menu -> [Import] and select Existing project to workspace and click [Next].
3 On the project import screen, select the folder where the sample program was expanded as the root directory.

4 Select a project, check Copy Project to Workspace, and click [Finish].

5 Double-click the configuration.xml of the RZ_N2H_CR52_0_primary project in the Project Explorer pane of e² studio to open it.



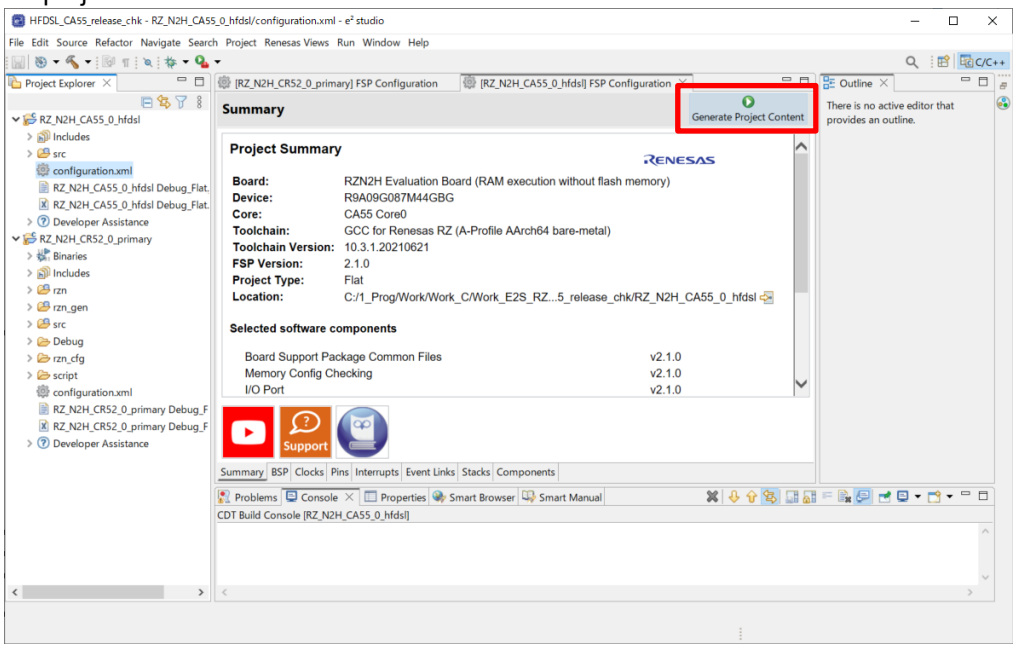
6 Click Generate Project Content in the FSP Configuration pane of e² studio.
The rzn, rzn_cfg, rzn_gen, script, .settings folders are generated in the RZ_N2H_CR52_0_primary project.



7 Select RZ_N2H_CR52_primary project in the Project Explorer pane and execute [Run] menu -> [Build Project].
The file Debug\RZ_N2H_CR52_0_primary.sbd is generated.

8 Double-click the configuration.xml of the RZ_N2H_CA55_0_hfdsl project in the Project Explorer pane of e² studio to open it. (RZ_N2H_CR52_0_primary.sbd of the primary project is referenced to open this configuration file. Please build the primary project in advance.)

9 Click Generate Project Content in the FSP Configuration pane of e² studio.
The rzn, rzn_cfg, rzn_gen, script, .settings folders are generated in the RZ_N2H_CA55_0_hfdsl project.

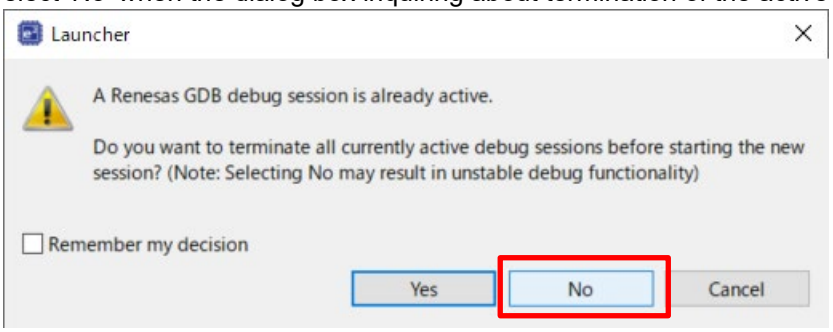


10 Select [Project] menu -> [Build All].
The Debug\RZ_N2H_CA55_0_hfdsl.elf file is generated.

(4) Execution Procedure of the Sample Program

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

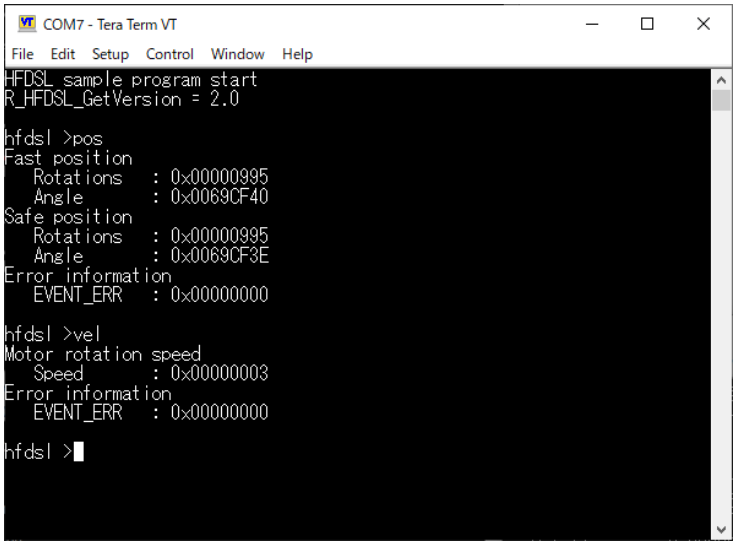
1 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging] for the RZ_N2H_CR52_0_primary project.
Click [Debug] to start downloading to internal RAM.
2 Click [Run] menu -> [Resume] to run the CA55 start-up program.
3 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging] for the RZ_N2H_CA55_0_hfdsl project.
4 Select 'No' when the dialog box inquiring about termination of the active debug session is displayed.



5 If 'Proceed with launch' is displayed, select 'Yes'.
6 Click [Debug] to start downloading to internal RAM.
7 Click [Run] menu -> [Resume] to run the sample program.

(5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.6 console commands in the RZ/N2H Group HIPERFACE DSL Sample Program Application Note.



Revision History

Rev.	Date	Description	
		Page	Summary
2.00	Dec 23.24	-	First Edition issued.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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