
RL78/G22 Simulator V1.08.00

Release Note

Thank you for using the RL78/G22 simulator.

This document describes restrictions on and points for caution regarding the simulator.

Read this document before using the product.

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Chapter 1. Target Devices and Supported Simulation Functions

The RL78/G22 simulator supports the following target devices.

Device	Part Number	
RL78/G22	16 pins	R7F102G4C, R7F102G4E
	20 pins	R7F102G6C, R7F102G6E
	24 pins	R7F102G7C, R7F102G7E
	25 pins	R7F102G8C, R7F102G8E
	30 pins	R7F102GAC, R7F102GAE
	32 pins	R7F102GBC, R7F102GBE
	36 pins	R7F102GCC, R7F102GCE
	40 pins	R7F102GEC, R7F102GEE
	44 pins	R7F102GFC, R7F102GFE
48 pins	R7F102GGC, R7F102GGE	

As well as CPU instructions, the RL78/G22 simulator is capable of simulating the following items in the target devices.

- Peripheral modules such as timers, the serial array unit, the serial interface, and SNOOZE mode sequencer
- Virtual target board (simulation via the [I/O panel] window)
- MCU pin signal waveforms (simulation via the [Timing chart] window)

Note that the RL78/G22 simulator does not support simulation of current drawn by this MCU.

Chapter 2. Changes

This chapter describes changes from V1.07.00 to V1.08.00 of the RL78/G22 simulator.

2.1 Improvements to the RL78/G22 simulator

2.1.1 Support for SMS debugging function

The simulator supports debugging of the SNOOZE Mode Sequencer (SMS) for RL78/G22 in this version.

- Function to break automatically when an SMS activating trigger occurs, before executing the processing specified by the SMSI0 register
- SMS step execution
- Function to forcibly start SMS debugging from the SMSI0 register

Note: SMS is executed in synchronization with the CPU.

For details, refer to the e² studio help.

Chapter 3. Points for Caution

This section lists points for caution on using the RL78/G22 simulator. These points for caution are in the following two categories.

- Differences in behavior between the target devices and the simulator due to simulator specifications
- Usage of simulation functions (operations in and configuration of the GUI windows)

CS+ for CC supports the [Virtual Board] panel which is described in those points for caution.

3.1 Differences in behavior between the target devices and the simulator

3.1.1 Peripheral functions not supported by the simulator

The simulator is not capable of simulating the following peripheral functions of the target devices.

- Regulator
- Power-on-reset circuit
- Voltage detector
- Operation state control
- Capacitive touch sensing unit (CTSU2La)
- Security function

3.1.2 Special function registers (SFRs) for controlling port functions

The following SFRs which control port functions are not simulated.

Although read/write access for each register can proceed normally, the operation does not change even though the value is changed.

- Port input mode registers (PIMxx)
- Port digital input disable registers (PDIDISxx)
- Port mode control T registers (PMCTxx)

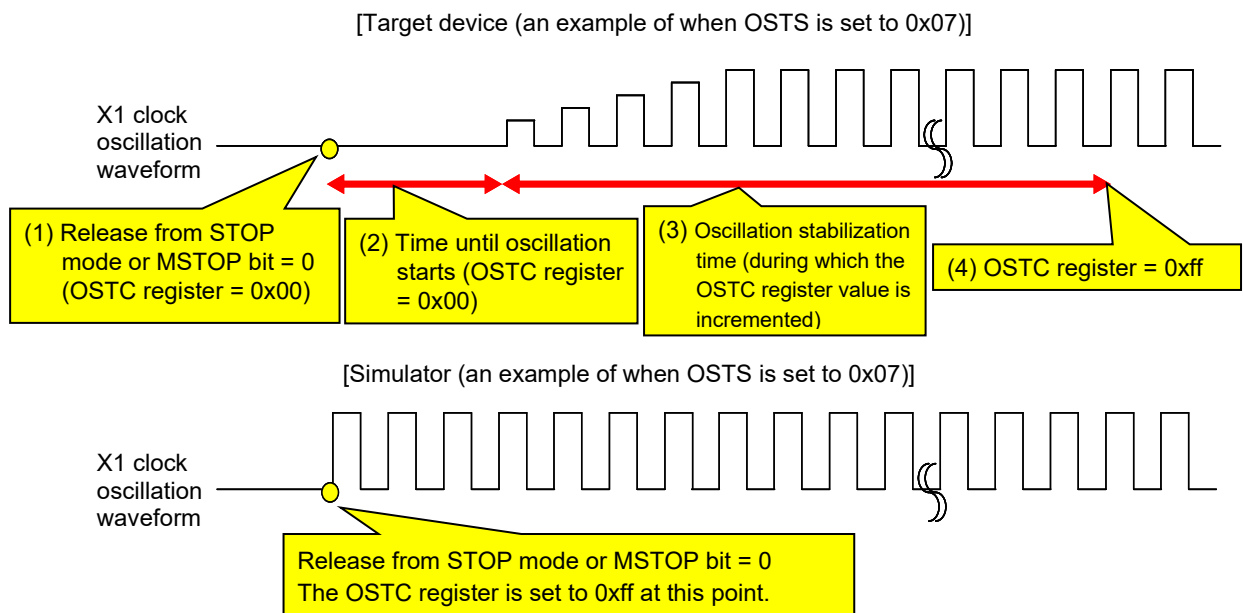
3.1.3 Oscillation stabilization time for the clock generator

Since the simulator does not simulate the clock oscillator oscillation stabilization time, stabilization always takes no time. When the oscillation is started, the OSTC register is set to one of the following values (i.e. not incremented).

OSTS Setting	OSTC Value
0x0 : $2^8/f_x$	0x80
0x1 : $2^9/f_x$	0xc0
0x2 : $2^{10}/f_x$	0xe0
0x3 : $2^{11}/f_x$	0xf0
0x4 : $2^{13}/f_x$	0xf8
0x5 : $2^{15}/f_x$	0xfc
0x6 : $2^{17}/f_x$	0xfe
0x7 : $2^{18}/f_x$	0xff

The following figure illustrates this operation.

In the target device, oscillation by the X1 clock starts after operation has passed through states (1) to (4). In the simulator, states (1) through (4) are skipped and oscillation instantly starts.



Therefore, pay attention to the code that waits for oscillation stabilization.

There is no problem if a program is created under the condition that execution proceeds after the oscillation stabilization wait period when the OSTC register value becomes the maximum value, or when the OSTC register value exceeds the specified value, but if a program is created under the condition that execution

proceeds after the oscillation stabilization wait period when the OSTC register value becomes a value other than the maximum value, execution will enter an endless loop.

The following shows examples of code that causes and does not cause problems.

The examples are when the OSTC is set to 0x07.

<u>Correct code example (1)</u>	<u>Correct code example (2)</u>	<u>Example of code that may cause problems</u>
<pre>while(OSTC != 0xff) { NOP();/* wait */ }</pre>	<pre>while(OSTC <= 0xf0) { NOP();/* wait */ }</pre>	<pre>while(OSTC != 0xf0) { NOP();/* wait */ }</pre>

3.1.4 SFRs (CMC, OSMC, HIOTRM, MIOTRM, LIOTRM, and CSC) in the clock generator

The following SFRs which belong to the clock generator are not simulated. Although read/write access for each register can proceed normally, the operation does not change even if the value is changed.

- Bits 0, 1, and 2 (AMPH, AMPHS0, and AMPHS1) of the clock operating mode control register (CMC)
- Bit 0 (HIPREC)^{Note} of the subsystem clock supply mode control register (OSMC)
- High-speed on-chip oscillator trimming register (HIOTRM)
- Middle-speed on-chip oscillator trimming register (MIOTRM)
- Low-speed on-chip oscillator trimming register (LIOTRM)

Note: In the simulator, the HIPREC bit is fixed to 0. However, if the STOP instruction is executed, the RL78/G22 will enter the STOP mode.

The operation in initialization of the EXCLKS, OSCSELS, XTSEL, AMPHS1, and AMPHS0 bits of the clock operation mode control register (CMC) and the XTSTOP bit of the clock operation status control register (CSC) differs between the target device and the simulator.

[Target device]

EXCLKS, OSCSELS, XTSEL, AMPHS1, AMPHS0, and XTSTOP bits are only initialized by a power-on reset and retain their values following resetting by other reset sources.

[Simulator]

Since the simulator does not support resetting by a power-on reset, the EXCLKS, OSCSELS, XTSEL, AMPHS1, AMPHS0, and XTSTOP bits are not initialized by the reset. The values of these bits are retained in response to resets from the following reset sources, which are those supported by the simulator.

- External reset input via the RESET pin
- Internal reset due to detection of a program malfunction by the watchdog timer
- CPU reset by the debugger

3.1.5 Operating clock of the timer array unit

Do not specify an operating clock that runs at or below 233 Hz. If the operating clock for the timer array unit runs at or below 233 Hz, then the timer array unit will not work properly (it will behave as if operating with a clock that is faster than the one selected).

3.1.6 Noise filter of the timer array unit

Although the target device's timer array unit has a function to turn the noise filters on and off in order to reduce noise from the timer input pins, the simulator does not simulate this function since there is no noise in the simulator's signals. That is, whether filtering is on or off makes no difference to the behavior.

3.1.7 SFRs (RTCC0, RTCC1, and SUBCUD) of the realtime clock (RTC)

The operation of realtime clock control register 0 (RTCC0), realtime clock control register 1 (RTCC1), and the time error correction register (SUBCUD) of the realtime clock (RTC) differs between the target device and the simulator.

[Target device]

The registers are cleared to 00H in response to an internal reset by the power-on reset circuit.

[Simulator]

The registers are not cleared to 00H in response to a reset because the simulator does not support the power-on reset circuit.

3.1.8 Clock output/buzzer output controller

When f_{MAIN} is selected as an output clock, the [Timing chart] window does not show the clock waveform of the PCLBUZn signal.

When $f_{\text{MAIN}}/2$ or a slower signal is selected as an output clock, the [Timing chart] window shows the clock waveform.

3.1.9 Interval interrupts generated by the watchdog timer

The timing of the generation of interval interrupts by the watchdog timer differs between the target device and the simulator.

[Target device]

When $75\% + 1/4f_{\text{IL}}$ of overflow time is reached

[Simulator]

When 75% of overflow time is reached

3.1.10 A/D converter

When no voltage is being applied to the VDD or AVREFP pin, the default reference voltage of the A/D converter is 5.0 V.

To change the reference voltage, input the desired voltage values for VDD and AVREFP via the [Signal Data Editor] window.

The temperature sensor output voltage is always 1.05 V.

3.1.11 Clock used in the serial array unit

Do not specify a clock that is 233 Hz or lower in the following cases. If the following clock of the serial array unit is 233 Hz or lower, then the serial array unit will not operate correctly (it will behave as if operating via a clock that is faster than the one selected).

- Operating clock(f_{MCK}) is 233Hz or lower.
- Transfer clock setting by dividing the operation clock ($f_{MCK} \div (SDRmn[15:9] + 1)$) is 233Hz or lower.

3.1.12 Noise filter of the serial array unit

Although the target device's serial array unit has a function to turn the noise filter on and off in order to reduce noise on the input pin, the simulator does not simulate this function since there is no noise in the simulator's signals. That is, whether filtering is on or off makes no difference to the behavior.

3.1.13 SDRmn registers of the serial array unit

The values read from the seven higher-order bits of the serial data registers (SDRmn) during serial operation differ between the target device and the simulator.

[Target device]

0 is read.

[Simulator]

The value read is that at the time serial operation starts.

3.1.14 SSm registers of the serial array unit

During serial communications, when the operation start trigger of channel n (SSmn) in the serial channel start register m (SSm) is set to 1, operation of the simulator differs from that of the actual target device in the way stated below.

[Target device]

The target device stops communications and enters the suspended state.

[Simulator]

The simulator does not stop communications. Accordingly, the TSFmn and BFFmn bits in the serial status register mn (SSRmn) are not cleared to 0.

3.1.15 Input switch control register (ISC) of the serial array unit

When (ISC3, ISC4) bits for the switch of the serial clock input source of CSI00 and (ISC6, ISC7) bits for the switch of the serial clock input source of CSI01 in the Input switch control register (ISC) are set to anything other than (0, 0) (normal operation), CSI communications are disabled in the [Serial] window. To enable CSI communications in the [Serial] window, set (ISC3, ISC4) bits and (ISC6, ISC7) bits to (0, 0).

3.1.16 IICA serial interface

IICA supports pin waveform generation and the communications through the [Serial] window. The following functions are not supported.

- Digital filter
- Arbitration
- Detection of transmission errors
- Communication reservation

3.1.17 SFR (ICCCTL01) for the IICA serial interface

The following SFR which controls the IICA serial interface is not simulated.

Although read/write access for the register can proceed normally, the operation does not change even if the value is changed.

- Bit 2 (DFC0) ^{Note} and bit 3 (SMC0) of the IICA control register 01 (IICCTL01)

Note: In the simulator, the DFC0 bit can be set to 1 only when the SMC0 bit is 1.

3.1.18 Times taken for data transfer by the data transfer controller (DTC)

The times taken for data transfer by the data transfer controller (DTC) differ between the target device and the simulator.

[Target device]

- A response time is required from detection of a DTC activation source until data transfer starts.
- A waiting time is required for access to extended special function registers (2nd SFRs).
- The DTC puts the data transfer on hold when the CPU executes any instruction that holds the DTC pending.
- Access to the data bus by the CPU is put on hold during DTC transfer.

[Simulator]

- Data transfer starts immediately after detection of a DTC activation source.
- No waiting time is required even for access to extended special function registers (2nd SFRs).
- The DTC does not put the data transfer on hold even when the CPU executes any instruction that should hold the DTC pending.
- Access to the data bus by the CPU is not put on hold even during DTC transfer.

3.1.19 Repeat mode of the data transfer controller (DTC)

If any of the conditions listed below is satisfied while the data transfer controller (DTC) is in repeat mode, the DTC ignores activation sources and will thus fail to transfer data.

- A DTC transfer count register j (DTCCTj) is set to 00H (number of transfers: 256 times).
- A DTC block size register j (DTBLSj) is set to 00H (block size: 256 or 512 bytes).
- A DTC control register j (DTCCRj) is used to set the transfer data size to 16 bits and the corresponding DTC block size register j (DTBLSj) is used to set the block size to 256 bytes or more.

3.1.20 Event link controller (ELC)

If any of the peripheral-module functions listed below is selected for linking by the event link controller (ELC), the simulator causes the peripheral-module function to operate immediately after reception of the event signal. The ELC in the actual device, on the other hand, causes the peripheral-module function to start operation several cycles after the ELC has received the event signal.

[Peripheral-module functions]

- Timer input channel 0 of timer array unit 0
- Timer input channel 1 of timer array unit 0
- A/D converter

3.1.21 SFR (WKUPMD) for the standby function

The following SFR which controls the standby function is not simulated.

Although read/write access for the register can proceed normally, the operation does not change even if the value is changed.

- Bit 0 (FWKUP) of the standby mode release setting register (WKUPMD)

3.1.22 Reset

Among the sources for generating reset signals, the following types of internal reset do not occur in the simulator.

- Internal reset by comparison of supply voltage and detection voltage of the power-on-reset circuit (POR)
- Internal reset by comparison of supply voltage and detection voltage of the voltage detectors (LVD0 and LVD1)
- Internal reset due to execution of an illegal instruction
- Internal reset due to a RAM parity error
- Internal reset due to illegal-memory access

In addition, the behavior differs as follows if a reset signal is input from the RESET pin.

[Target device]

The MCU is reset when the RESET pin goes low. Release from the reset state proceeds when the RESET pin goes high.

[Simulator]

The MCU is not reset when the RESET pin goes low. The simulator is reset momentarily and then released when the RESET pin goes high.

3.1.23 Reset control flag register (RESF)

The simulator only supports the WDTRF bit of the reset control flag register (RESF).

The simulator is not capable of simulating the operations of the other bits (TRAP, RPERF, IAWRF, and LVIRF). Only the default values of these bits are indicated.

The reset control flag register (RESF) of the target device is cleared by a reset input via the RESET pin, a reset by the power-on-reset circuit (POR), or reading the RESF register by using an 8-bit memory manipulation instruction. However, on the simulator, the RESF is only cleared by a reset input via the RESET pin.

3.1.24 Safety functions

The simulator does not support the following safety functions.

- Flash memory CRC operation function (high-speed CRC, general-purpose CRC)
- Flash memory guard function
- RAM parity error detection
- RAM guard function
- SFR guard function
- Illicit memory access detection
- Guard function of invalid memory access detection control register (IAWCTL)

3.1.25 Power supply for battery backup (VBAT)

The simulator does not simulate the power supply for battery backup (VBAT).

3.1.26 Executing illegal instructions

If an illegal instruction (instruction code: 0xFF) is executed, the target device will be reset, but the simulator will go into an endless loop (the illegal instruction will be executed repeatedly).

3.1.27 Conversion start time in the A/D converter

The simulator does not support the conversion start time but recognizes the time as 0 clock cycles in simulation.

3.1.28 Flash memory

The simulator does not support serial programming.

3.1.29 FSASTL register in flash memory

In the simulator, the WRER and ERER bits in the flash memory sequencer status register L (FSASTL) are always 0 because writing or erasure of flash memory will not fail.

3.1.30 Setting of the flash memory control mode

Setting each of the flash memory control modes requires writing the values to the flash protect command register (PFCMD) and flash programming mode control register (FLPMC) according to the procedure for executing the specific sequence.

In the target device, if writing to any other memory area or register is attempted during execution of the specific sequence, a protection error occurs, writing to the specified register does not proceed, and the FPRERR flag of the flash status register (PFS) is set to 1.

In the simulator, if writing to any other memory area is attempted during execution of the specific sequence, a protection error does not occur, writing to the specified register proceeds, and the FPRERR flag of the flash status register (PFS) is not set to 1. If writing to any other register is attempted during execution of the specific sequence, the operation will be the same as that of the target device.

3.1.31 Entry to the non-programmable mode in self-programming

In the target device, after executing the procedure for entry to the non-programmable mode from the code flash memory programming mode or data flash memory programming mode and waiting, reading from the target flash memory for the programming mode before the mode transition becomes possible.

In the simulator, reading from the target flash memory for the programming mode before the mode transition becomes possible without the wait.

3.1.32 Security settings of flash memory

The simulator supports neither control of connection to the programmer and on-chip debugger nor programmer connection ID authentication.

3.1.33 Access to the data flash memory

In the target device, the DFLEN bit in the data flash control register (DFLCTL) must be set to 1 to enable access to the data flash memory. However, the simulator can read the data flash memory with a CPU instruction even if the setting of the DFLEN bit is 0.

3.2 Usage of simulation functions

3.2.1 Simulation speed

The simulation speed of RL78/G22 simulator depends on the number of operating peripheral functions. If many peripheral functions are operating, the simulation speed becomes from several to ten times slower than the actual device. ^{Note}

With the use of only a few, or even no peripheral functions, the simulation speed may become faster than the actual device.

Note: The measurement environment for simulation speed is as follows.

CPU: 3.20 GHz (Quad-Core); memory: 8 Gbytes; OS: Windows11

3.2.2 Pin waveforms in the [Timing chart] window

The maximum length of a pin waveform is 4096 signal-level changing points. After reaching this maximum length, the data will be overwritten from the oldest value. If this length is not sufficient, use the following methods.

- Reduce the number of registered pins
- Stop the user program at the place where you want to confirm the waveform by using a breakpoint

3.2.3 Controlling windows


The following keyboard operations are not available in the simulator windows ([Signal Data Editor], [I/O panel], and [Serial]).


- Navigation via tab or arrow keys (←, ↑, →, ↓)
- Deletion via the Del or Backspace keys
- Cut & paste and other operations via the Ctrl + C, V, X, A, or Z keys.

Perform the above operations as follows.

- Navigation: Navigate by using the mouse.
- Deletion: Right-click and perform the action from the context menu.
- Cut & paste, etc.: Right-click and perform the action from the context menu.

3.2.4 Closing the [Simulator GUI] window

The [Simulator GUI] window can only be closed by disconnecting from the debugging tool, or by closing CS+ in proper manner. The  button cannot be used.

Additionally, although it appears that the  button can be pressed if Aero is enabled in Windows, pressing this button will not close the [Simulator GUI] window.

3.2.5 Disconnecting the debug tool

CS+ may be closed if the debugging tool is disconnected while any of the following dialog boxes is open from the [Simulator GUI] window. Be sure that the following dialog boxes have been closed before disconnecting the simulator.

- Save As
- Open
- New
- Color
- Font
- Customize
- Loop
- Select Pin
- Search Data
- Format (UART)
- Format (CSI)
- Format (IIC)
- Message (e.g. Error)
- Parts Button Properties
- Analog Button Properties
- Parts Key Properties
- Parts Level Gauge Properties
- Parts Led Properties
- Parts Segment LED Properties
- Parts Matrix Led Properties
- Parts Buzzer Properties
- Pull up / Pull down
- Entry Bitmap
- Object Properties

3.2.6 [Serial] window

When using the [Serial] window as the data receiver for the simplified I²C of the serial array unit or IICA, only ACK can be generated after receiving the data. NACK cannot be generated.

3.2.7 Setting the pins in the simulator GUI or the [Virtual Board] panel

The peripheral I/O redirection register (PIOR) can be manipulated by a program or debugger operations to re-assign specific multiplexed pin functions to alternative port pins in the same way as on the actual device. However, if the assignment of serial interface functions to port pins is changed to use the [Serial] window or the serial communication component of the [Virtual Board] panel, set the changed port pins when making settings of the [Format] dialog box in the [Serial] window or the serial communication component of the [Virtual Board] panel. This enables the use of the [Serial] window or the serial communication component of the [Virtual Board] panel when port pins to which multiplexed functions are assigned by the PIOR are changed.

After re-assigning a given pin function by using the PIOR, be sure to select the name of the pin you are currently using in the [Select Pin] dialog box of the simulator GUI or “Connected To” of the component in the [Virtual Board] panel.

3.2.8 Events for debugging during the use of boot swapping

When boot swapping of flash memory is to be used, if an event for debugging is set in a boot cluster before swapping, correct swapping cannot proceed with the data for the address of the event or the event may be invalid.

Delete all events before swapping and set any events again after swapping.

3.2.9 Events for debugging during copying of the code for rewrite processing to the RAM in self-programming

When the code flash area or extra area is to be rewritten through self-programming, if an event for debugging is set at a RAM address before copying of the code for rewrite processing to the RAM, the event may be invalid after copying to the RAM has proceeded.

3.2.10 SMS debugging function

The following notes apply to the SMS debugging function.

- During SMS step execution, if the clock required to execute a sequencer processing command stops, if SMS is reset (PRR1.SMSRES = 1), or if SMS is forcibly terminated (SMSC.SMSSTOP = 1), SMS step execution stops and the program breaks.
- When the SMS is in the "Activation pending state" or "Activating trigger waiting state", clearing the SMSTRGWAIT bit in the SMSC register to 0 or executing the function to forcibly start SMS debugging causes a break before the processing specified by the SMSI0 register is executed. Note that if the SMSI0 processing takes 1 cycle of fCLK, the break may occur after execution.

Revision History

Rev.	Date	Description	
		Page	Summary
Rev.1.00	Mar.01.26	-	First Edition

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