RL78/G1F Simulator V1.11.00

Release Note

Thank you for using the RL78/G1F simulator.

This document describes restrictions on and points for caution regarding the simulator.

Read this document before using the product.

Contents

Chapter 1. Target Devices and Supported Simulation Functions

The RL78/G1F simulator supports the following target devices.

Device group	Device name
RL78/G1F	R5F11B7C
	R5F11BBC
	R5F11BCC
	R5F11BGC
	R5F11BLC
	R5F11B7E
	R5F11BBE
	R5F11BCE
	R5F11BGE
	R5F11BLE

The RL78/G1F simulator is capable of simulating the following items as well as CPU instructions.

- Peripheral modules such as timers, the serial array unit, and the serial interface
- Virtual target board (simulation via the [I/O panel] window)
- MCU pin signal waveforms (simulation via the [Timing chart] window)

Note that the RL78/G1F simulator does not support simulation of current drawn by these MCUs.

Chapter 2. Changes

This chapter describes changes from V1.10.00 to V1.11.00 of the RL78/G1F simulator.

2.1 Improvements to the RL78/G1F simulator

2.1.1 Improvement to canceling clock stretching of the IICA serial interface

When all conditions listed below were satisfied, clock stretching of the eighth clock cycle during the reception of addresses could not be cancelled by setting bit 5 (WRELn) in IICA control register n0 (IICCTLn0). This problem has now been rectified so that setting the bit cancels clock stretching under those conditions.

- Operation is in slave mode.
- An extension code is received.
- Bit 3 (WTIMn) in IICA control register n0 (IICCTLn0) is 1.
- Bit 3 (TRCn) in IICA status register n (IICSn) is 1 (sending state).

Chapter 3. Points for Caution

This section lists points for caution on using the RL78/G1F simulator. These points for caution are in the following two categories.

• Differences in behavior between the target devices and the simulator due to simulator specifications

• Usage of simulation functions (operations in and configuration of the GUI windows)

CS+ for CC supports the [Virtual Board] panel which is described in those points for caution.

3.1 Differences in behavior between the target devices and the simulator

3.1.1 Peripheral functions not supported by the simulator

The simulator is not capable of simulating the following peripheral functions of the target devices.

- Regulator
- Power-on-reset circuit
- Voltage detector
- Flash self-programming

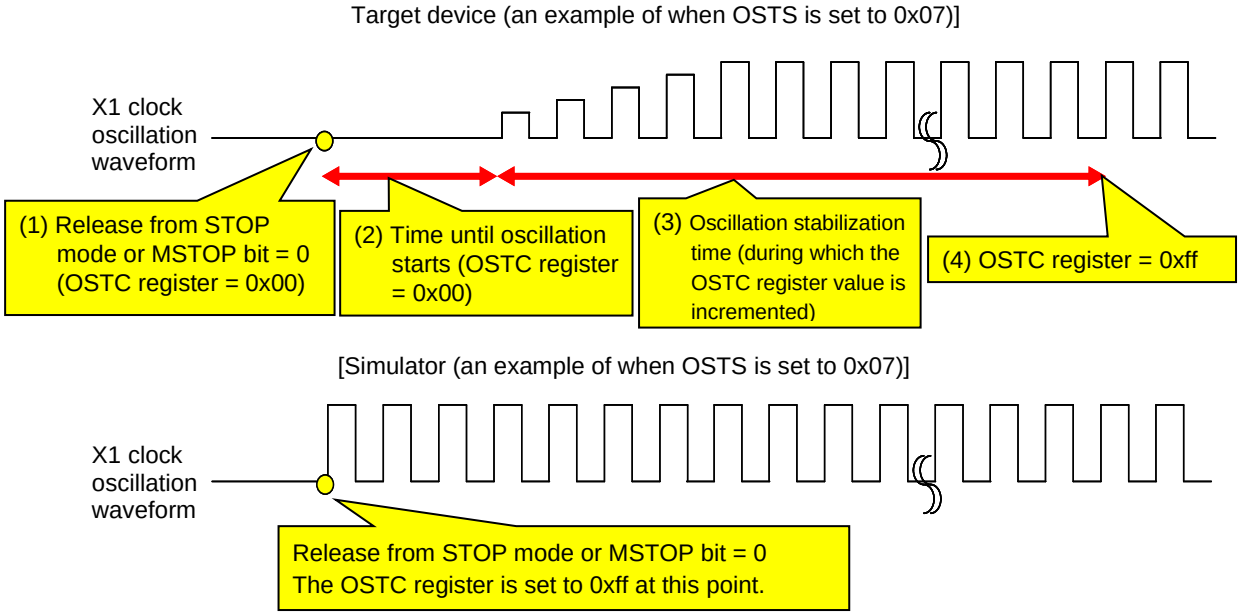
3.1.2 Oscillation stabilization time for the clock generator

Since the simulator does not simulate the clock oscillator oscillation stabilization time, stabilization always takes no time. When the oscillation is started, the OSTC register is set to one of the following values (i.e. not incremented).

OSTS Setting	OSTC Value
0x0 : 2^8/fx	0x80
0x1 : 2^9/fx	0xc0
0x2 : 2^{10}/fx	0xe0
0x3 : 2^{11}/fx	0xf0
0x4 : 2^{13}/fx	0xf8
0x5 : 2^{15}/fx	0xfc
0x6 : 2^{17}/fx	0xfe
0x7 : 2^{18}/fx	0xff

The following figure illustrates this operation.

In the target device, oscillation by the X1 clock starts after operation has passed through states (1) to (4). In the simulator, states (1) through (4) are skipped and oscillation instantly starts.



Therefore, pay attention to the code that waits for oscillation stabilization.

There is no problem if a program is created under the condition that execution proceeds after the oscillation stabilization wait period when the OSTC register value becomes the maximum value, or when the OSTC register value exceeds the specified value, but if a program is created under the condition that execution proceeds after the oscillation stabilization wait period when the OSTC register value becomes a value other than the maximum value, execution will enter an endless loop.

The following shows examples of code that causes and does not cause problems.

The examples are when the OSTS is set to 0x07.

Correct code example (1)

```
while(OSTC != 0xff)
{
NOP();/* wait */
}
```

Correct code example (2)

```
while(OSTC <= 0xf0)
{
NOP();/* wait */
}
```

Example of code that may cause problems

```
while(OSTC != 0xf0)
{
NOP();/* wait */
}
```

3.1.3 SFRs (AMPH, AMPHS0, AMPHS1, and HIOTRM) in the clock generator

The following SFRs which belong to the clock generator are not simulated. Although read/write access for each register can proceed normally, the operation does not change even if the value is changed.

- Bits 0, 1, and 2 (AMPH, AMPHS0, and AMPHS1) of the clock operating mode control register (CMC)
- High-speed internal oscillator trimming register (HIOTRM)

3.1.4 Operating clock of the timer array unit

Do not specify an operating clock that runs at or below 233 Hz. If the operating clock for the timer array unit runs at or below 233 Hz, then the timer array unit will not work properly (it will behave as if operating with a clock that is faster than the one selected).

3.1.5 Noise filter of the timer array unit

Although the target device's timer array unit has a function to turn the noise filters on and off in order to reduce noise from the timer input pins, the simulator does not simulate this function since there is no noise in the simulator's signals. That is, whether filtering is on or off makes no difference to the behavior.

3.1.6 Digital filters in timers RJ, RD, and RG

The simulator does not simulate the digital filters in timers RJ, RD, and RG.

3.1.7 Interval interrupts generated by the watchdog timer

The timing of the generation of interval interrupts by the watchdog timer differs between the target device and the simulator.

[Target device]

When 75% + 1/2f_{IL} of overflow time is reached

[Simulator]

When 75% of overflow time is reached

3.1.8 Clock used in the serial array unit

Do not specify a clock that is 233 Hz or lower in the following cases. If the following clock of the serial array unit is 233 Hz or lower, then the serial array unit will not operate correctly (it will behave as if operating via a clock that is faster than the one selected).

- Operating clock(f_{MCK}) is 233Hz or lower.
- Transfer clock setting by dividing the operation clock (f_{MCK} ÷ (SDRmn[15:9] + 1)) is 233Hz or lower.

3.1.9 Noise filter of the serial array unit

Although the target device's serial array unit has a function to turn the noise filter on and off in order to reduce noise on the input pin, the simulator does not simulate this function since there is no noise in the simulator's signals. That is, whether filtering is on or off makes no difference to the behavior.

3.1.10 SDRmn registers of the serial array unit

The values read from the seven higher-order bits of the serial data registers (SDRmn) during serial operation differ between the target device and the simulator.

[Target device]

0 is read.

[Simulator]

The value read is that at the time serial operation starts.

3.1.11 IICA serial interface

IICA supports pin waveform generation and the communications through the [Serial] window. The following functions are not supported.

- Digital filter
- Arbitration
- Detection of transmission errors
- Communication reservation

3.1.12 SFR (IICCTLn1) for the IICA serial interface

The following SFR which controls the IICA serial interface is not simulated.

Although read/write access for the register can proceed normally, the operation does not change even if the value is changed.

- Bit 2 (DFCn) [Note] and bit 3 (SMCn) of the IICA control register n1 (IICCTLn1)

Note: In the simulator, the DFCn bit can be set to 1 only when the SMCn bit is 1.

3.1.13 Reset

The behavior differs as follows if a reset signal is input from the RESET pin.

[Target device]

The MCU is reset when the RESET pin goes low. Release from the reset state proceeds when the RESET pin goes high.

[Simulator]

The MCU is not reset when the RESET pin goes low. The simulator is reset momentarily and then released when the RESET pin goes high.

3.1.14 Reset control flag register (RESF)

The simulator only supports the WDTRF bit of the reset control flag register (RESF).

The simulator is not capable of simulating the operations of the other bits (TRAP, RPERF, IAWRF, and LVIRF). Only the default values of these bits are indicated.

The reset control flag register (RESF) of the target device is automatically cleared if it is read by an 8-bit memory manipulation instruction; however, this does not clear the register in the case of the simulator.

3.1.15 A/D converter

When no voltage is being applied to the VDD or AVREFP pin, the default reference voltage of the A/D converter is 5.0 V.

To change the reference voltage, input the desired voltage values for VDD and AVREFP via the [Signal Data Editor] window.

The temperature sensor output voltage is always 1.05 V.

3.1.16 Conversion start time in the A/D converter

The simulator does not support the conversion start time but recognizes the time as 0 clock cycles in simulation.

3.1.17 Clock output/buzzer output controller

When f_{MAIN} is selected as an output clock, the [Timing chart] window does not show the clock waveform of the PCLBUZn signal.

When $f_{MAIN}/2$ or a slower signal is selected as an output clock, the [Timing chart] window shows the clock waveform.

3.1.18 Executing illegal instructions

If an illegal instruction (instruction code: 0xFF) is executed, the target device will be reset, but the simulator will go into an endless loop (the illegal instruction will be executed repeatedly).

3.1.19 Times taken for data transfer by the data transfer controller (DTC)

The times taken for data transfer by the data transfer controller (DTC) differ between the target device and the simulator.

[Target device]

- A response time is required from detection of a DTC activation source until data transfer starts.
- A waiting time is required for access to extended special function registers (2nd SFRs).
- The DTC puts the data transfer on hold when the CPU executes any instruction that holds the DTC pending.
- Access to the data bus by the CPU is put on hold during DTC transfer.

[Simulator]

- Data transfer starts immediately after detection of a DTC activation source.
- No waiting time is required even for access to extended special function registers (2nd SFRs).
- The DTC does not put the data transfer on hold even when the CPU executes any instruction that should hold the DTC pending.
- Access to the data bus by the CPU is not put on hold even during DTC transfer.

3.1.20 Repeat mode of the data transfer controller (DTC)

If any of the conditions listed below is satisfied while the data transfer controller (DTC) is in repeat mode, the DTC ignores activation sources and will thus fail to transfer data.

- A DTC transfer count register j (DTCCTj) is set to 00H (number of transfers: 256 times).
- A DTC block size register j (DTBLSj) is set to 00H (block size: 256 or 512 bytes).
- A DTC control register j (DTCCRj) is used to set the transfer data size to 16 bits and the corresponding DTC block size register j (DTBLSj) is used to set the block size to 256 bytes or more.

3.1.21 Event link controller (ELC)

If any of the peripheral-module functions listed below is selected for linking by the event link controller (ELC), the simulator causes the peripheral-module function to operate immediately after reception of the event signal. The ELC in the actual device, on the other hand, causes the peripheral-module function to start operation several cycles after the ELC has received the event signal.

[Peripheral-module functions]

- Timer input channel 0 of timer array unit 0
- Timer input channel 1 of timer array unit 0
- Timers RG, RD0, and RD1, and PWM option unit A (PWMOPA)
- Channels 0 and 1 of the D/A converter

3.1.22 D/A converter

When no voltage value is set for the VDD pin, the default reference voltage of the D/A converter is 5.0 V. To change the reference voltage, specify the desired voltage value for the VDD pin via the [Signal Data Editor] window or some other means.

3.1.23 Reference voltage of the comparators (CMP)

When no voltage value is set for the VDD pin, the simulator generates the reference voltage on the assumption that 5 V is being input to the VDD pin.

To change the reference voltage, specify the desired voltage value for the VDD pin via the [Signal Data Editor] window or some other means.

3.1.24 Internal reference voltage of the comparators (CMP)

In the target device, bits CVRVS0 and CVRVS1 of the comparator internal reference voltage control register (CVRCTL) are used to select the power supply and GND, respectively, of the internal reference voltage to be input to the D/A converter as the comparator reference voltage (VREF0 or VREF1).

In the simulator, on the other hand, the voltages of VREF0 and VREF1 only depend on the power supply (i.e. not on GND) of the internal reference voltage. While you can use the CVRVS0 bit to select VDD or AVREFP as the power supply, GND is fixed to 0 V regardless of the setting of the CVRVS1 bit.

3.1.25 Digital filters in the comparators (CMP)

The simulator does not simulate the digital filters in the comparators (CMP).

3.1.26 Voltages amplified by the programmable gain amplifier (PGA)

In the hardware configuration of the target device, the voltages amplified by the programmable gain amplifier (PGA) depend on the voltages on the PGAGND and VSS pins. The voltages amplified by the simulated PGA, on the other hand, only depend on the voltage on the PGAI pin (i.e. not on those on the PGAGND and VSS pins).

3.1.27 Widths of pulses received by the IrDA interface

In the target device, the IrDA interface does not recognize pulses shorter than 1.41 μs (which is the minimum pulse width). In the simulator, on the other hand, pulses shorter than 1.41 μs are recognized.

3.1.28 Safety functions

The simulator does not support the following safety functions.

- Flash memory CRC operation function (high-speed CRC, general-purpose CRC)
- RAM parity error detection
- RAM guard function
- SFR guard function
- Invalid memory access detection

3.1.29 SSm registers in the serial array unit

During serial communications, when the operation start trigger of channel n (SSmn) in the serial channel start register m (SSm) is set to 1, operation of the simulator differs from that of the actual target device in the way stated below.

[Target device]

The target device stops communications and enters the suspended state.

[Simulator]

The simulator does not stop communications. Accordingly, the TSFmn and BFFmn bits in the serial status register mn (SSRmn) are not cleared to 0.

3.2 Usage of simulation functions

3.2.1 Simulation speed

The simulation speed of RL78/G1F simulator depends on the number of operating peripheral functions.

If many peripheral functions are operating, the simulation speed becomes from several to ten times slower than the actual device. Note

With the use of only a few, or even no peripheral functions, the simulation speed may become faster than the actual device.

Note: The measurement environment for simulation speed is as follows.

CPU: 3.20 GHz (Quad-Core); memory: 8 Gbytes; OS: Windows10 64-bit edition

3.2.2 Pin waveforms in the [Timing chart] window

The maximum length of a pin waveform is 4096 signal-level changing points. After reaching this maximum length, the data will be overwritten from the oldest value. If this length is not sufficient, use the following methods.

- Reduce the number of registered pins
- Stop the user program at the place where you want to confirm the waveform by using a breakpoint

3.2.3 Controlling windows

The following keyboard operations are not available in the simulator windows ([Signal Data Editor], [I/O panel], and [Serial]).

- Navigation via tab or arrow keys (←, ↑, →, ↓)
- Deletion via the Del or Backspace keys
- Cut & paste and other operations via the Ctrl + C, V, X, A, or Z keys.

Perform the above operations as follows.

- Navigation: Navigate by using the mouse.
- Deletion: Right-click and perform the action from the context menu.
- Cut & paste, etc.: Right-click and perform the action from the context menu.

3.2.4 Closing the [Simulator GUI] window

The [Simulator GUI] window can only be closed by disconnecting from the debugging tool, or by closing CS+ in proper manner. The [X] button cannot be used.

Additionally, although it appears that the [X] button can be pressed if Aero is enabled in Windows, pressing this button will not close the [Simulator GUI] window.

3.2.5 Disconnecting the debug tool

CS+ may be closed if the debugging tool is disconnected while any of the following dialog boxes is open from the [Simulator GUI] window. Be sure that the following dialog boxes have been closed before disconnecting the simulator.

- •Save As
- •Open
- •New
- •Color
- •Font
- •Customize
- •Loop
- •Select Pin
- •Search Data
- •Format (UART)
- •Format (CSI)
- •Format (IIC)
- •Message (e.g. Error)
- •Parts Button Properties
- •Analog Button Properties
- •Parts Key Properties
- •Parts Level Gauge Properties
- •Parts Led Properties
- •Parts Segment LED Properties
- •Parts Matrix Led Properties
- •Parts Buzzer Properties
- •Pull up / Pull down
- •Entry Bitmap
- •Object Properties

3.2.6 [Serial] window

When using the [Serial] window as the data receiver for the simplified I^2C of the serial array unit or IICA, only ACK can be generated after receiving the data. NACK cannot be generated.

3.2.7 Setting the pins in the simulator GUI or the [Virtual Board] panel

The peripheral I/O redirection register (PIOR) can be manipulated by a program or debugger operations to re-assign specific multiplexed pin functions to alternative port pins in the same way as on the actual device. However, if the assignment of serial interface functions to port pins is changed to use the [Serial] window or the serial communication component of the [Virtual Board] panel, set the changed port pins when making settings of the [Format] dialog box in the [Serial] window or the serial communication component of the [Virtual Board] panel. This enables the use of the [Serial] window or the serial communication component of the [Virtual Board] panel when port pins to which multiplexed functions are assigned by the PIOR are changed.

After re-assigning a given pin function by using the PIOR, be sure to select the name of the pin you are currently using in the [Select Pin] dialog box of the simulator GUI or “Connected To” of the component in the [Virtual Board] panel.

Revision History

Rev.	Date	Description	
		Page	Summary
Rev.1.00	Jun.01.25	-	First Edition

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