

Peripheral Driver Generator V.2.08

R20UT2843EJ0100

Release Note

Rev.1.00

Dec 01, 2013

1. Description of Revision

Refer to the RENESAS TOOL NEWS Document No.131216/tnx at:

<http://tool-support.renesas.com/eng/toolnews/131216/tnx.htm>

2. Precautions

Some known problems reside in Peripheral Driver Generator V.2.08. You can refer to the details of them that have not been fixed yet on the following Web page.

http://tool-support.renesas.com/eng/toolnews/p_tool_3.htm

The following problems also reside in Peripheral Driver Generator V.2.08.

2.1 A Note on Selecting Address/Data Multiplexed Bus for CS0 area (RX630)

(1) Description

When address/data multiplexed bus is selected only for CS0 area in the bus setting window, ALE pin is enabled by calling generated function `R_PG_ExtBus_SetBus`. However, ALE is not displayed as used pin function in the pin function pane ([Pin function] sheet and [Peripheral pin usage] sheet). Even if other pin function is assigned to the ALP pin, the warning indicating confliction is not displayed.

(2) Conditions

When address/data multiplexed bus is selected only for CS0 area in the bus setting window

(3) Workaround

Do not assign other pin functions to ALE pin when selecting address/data multiplexed bus for any of CS areas.

2.2 A Note on Setting Single Write Strobe Mode for External Bus (RX630)

(1) Description

When single write strobe mode is selected as write access mode for any of CS areas, `BC0#` is displayed as used pin function in the pin function pane ([Pin function] sheet and [Peripheral pin usage] sheet) even when `[A7-A0(BC0#)]` in `[Address output pins]` is not checked. However, `BC0#` is not enabled when calling generated function `R_PG_ExtBus_SetBus`.

(2) Conditions

When single write strobe mode is selected as write access mode for any of CS areas

(3) Workaround

If you use the `BC0#`, check `[A7-A0(BC0#)]` in `[Address output pins]`.

2.3 A Note on Selecting TMR Clock for SCI Transfer Clock (RX62N,RX210,RX630,RX63N,RX631,RX220)

(1) Description

When TMR clock is selected as the SCI transfer clock in SCI setting window, error arises if [Bit rate] edit box is empty.

(2) Conditions

When TMR clock is selected as the SCI transfer clock in SCI setting window.

(3) Workaround

When TMR clock is selected as the SCI transfer clock, the value of [Bit rate] is not used for settings. Input 0 into the edit box to avoid an error.

2.4 A Note on Setting Peripheral Module Clock (PCLK) (RX62T)

In the setup window of the clock generation circuit, [EXTAL*8] is included in the selection menu of [Peripheral module clock (PCLK)]. However, EXTAL*8 cannot be selected as the clock source of PCLK in the RX62T. Do not select this item. When this item is selected, an error occurs and the source generation cannot be executed.

2.5 A Note on Disabling Sub-clock Oscillation (RX630,RX63N,RX631,RX220)

The sub-clock oscillator is enabled after reset. If the sub-clock oscillator is not required, disable it as follows:

- Check the [Use sub-clock] check box in the setup window of the clock generation circuit.
(For RX210 and RX220, check [Use RTC-dedicated clock (supplied by the sub-clock oscillator)])
- Call R_PG_Clock_Stop_SUB after calling PG_Clock_Set or R_PG_Clock_WaitSet.

2.6 A Note on Setting Pinfunctions of MTU2a, TMR and SC1c (RX210)

The following pin functions of 145pin or 144pin package of RX210 cannot be set up.

MTU2a	TMR	SC1c
MTIOC3B (P80)	TMC10 (P01)	RXD6/SMISO6/SSCL6 (P01)
MTIOC3C (P56)	TMR10 (P00)	TXD6/SMOSI6/SSDA6 (P01)
MTUIC3D (P81)	TMC11 (P02)	SCK6 (P02)
MTUIC4A (P82)		
MTUIC4C (P83)		

If these pins are selected in [Peripheral pin usage] window, the generated source files cannot be built. Do not select these pins in [Peripheral pin usage] window.

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